1/4 VGA Cholesteric Display Module with SPI™-Compatible Interface

Product Features

Display Module:

- 320 Columns × 240 Rows
- Active Frame: 2 Rows and 2 Columns
- 72 dpi (pixels per inch)
- Approximate Size: 155 x 108 x 14 mm
- Four Standard Colors
- Integrated LCD Bias Supply
- "No Power" Image Retention
- 3.3V Logic Supply
- 4.0V – 9.0V Power Supply
- Viewing Cone Comparable to Paper
- Low Profile Modular Design
- Available with Optional Bezel

Embedded Controller:

- Serial Peripheral Interface (SPI) Compatible
- 250 kbps Image Download
- 32 KB of Image Memory
- 10 µA Sleep Current
- Full or Partial Screen Update Ability

Typical Applications

- **Battery Powered Portable Devices**
- **Machine Interface**
- **Inventory Tracking Displays**
- **Instrumentation Displays**
- **Remote Control Display Applications**
- **Point of Sale Displays**

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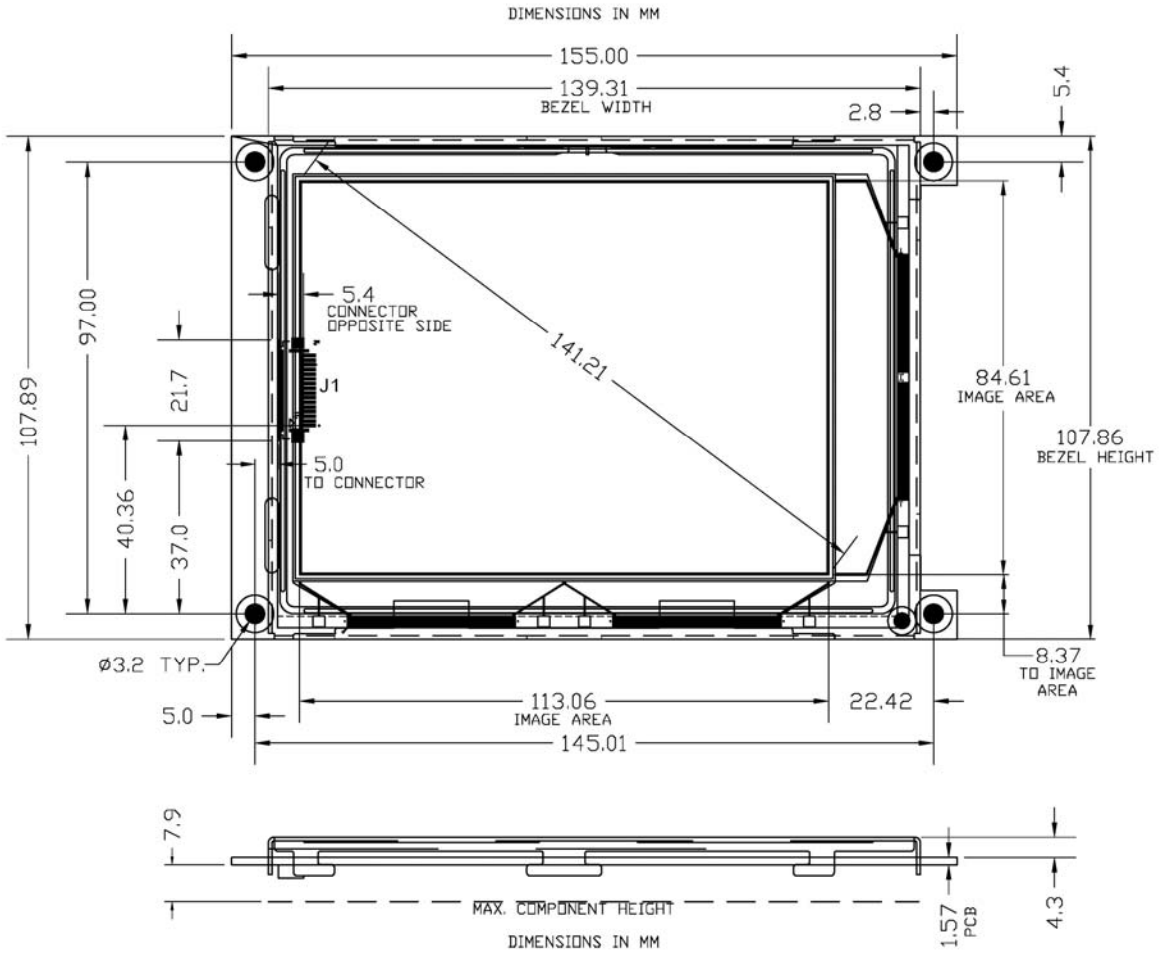
Specification Summary

Parameter	Description
Display Type	Reflective Cholesteric LCD
Format	320 Columns × 240 Rows (318 x 238 Minus the Active Frame)
Resolution	72 dots per inch, 0.36 mm between pixel centerlines (both horizontal and vertical)
Image Area	113.06 mm × 84.61 mm (Dimensions do not include active frame.)
Display Module Weight	105 grams (Weight is 150 grams with optional bezel.)
Operating Temperature Range	0°C to +60°C
Storage Temperature Range	-30°C to +80°C
Full Image Update Rate	1.85 sec @ 25°C

(Shown with Optional Bezel)

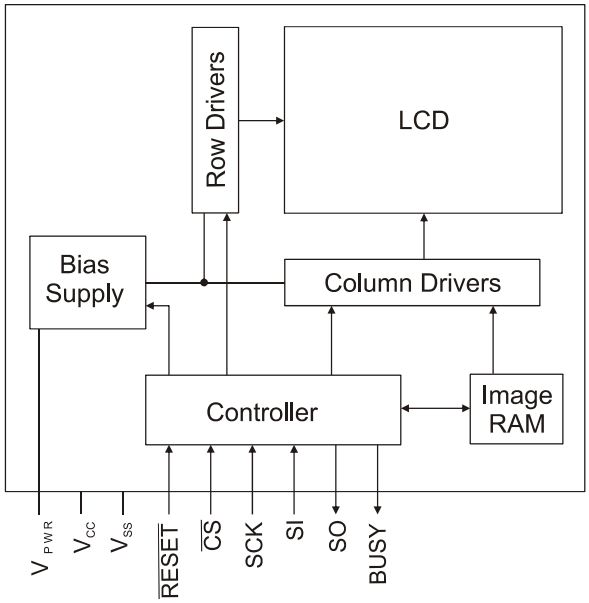


Contents

1 Overview

The 320x240 (1/4 VGA) ChLCD is a general-purpose graphic display module ideally suited for battery powered portable devices and display applications that require superior optical performance including wide viewing angle and sunlight readability. The display is a reflective cholesteric liquid crystal display (ChLCD) that takes full advantage of the technology's unique "No Power" image retention attribute. The embedded display controller generates the unique ChLCD drive waveforms and provides automatic temperature compensation. The SPI-compatible interface to the embedded controller simplifies system integration using a minimal number of I/O resources and controls all display operations, from downloading image data to triggering display updates. Bistable, sunlight readable, and easy to integrate, the 320x240 (1/4 VGA) is truly a unique LCD display solution.

2 Block Diagram



3 Electrical Interface

3.1 Header

Electrical connection to the display module is made through the 16-contacts located at J1 (see section 5.4). Connection options include a 1mm pitch ZIF flat flex connector (FFC – with top or bottom contacts) soldered to the printed circuit board at J1, or a 50mm flat flexible cable soldered at J1 (with the cable contacts at the opposite end facing up – toward the component side of the display module, or down – toward the viewing side of the display module). Custom cable lengths are available upon request. Minimum quantities may apply for custom configurations.

3.2 Pin Summary

Name	Number	Type	Description
$\overline{\text{RESET}}$	1	Input	Reset (Optional Use).
BUSY	2	Output	Display Busy Status Indicator (Optional Use).
V_{SS}	3,8,12,14	Supply	Ground.
SCK	4	Input	Serial Data Clock.
SO	5	Output	Serial Data Output.
SI	6	Input	Serial Data Input.
$\overline{\text{CS}}$	7	Input	Chip Select.
V_{CC}	9	Supply	Logic Supply (3.3V).
V_{PWR}	10,11,13	Supply	Power Supply (4.0V – 9.0V).
NC	15,16	--	No Connection.

3.3 Pin Functions

3.3.1 Logic Interface

SERIAL INPUT (SI): The SI pin is used to shift commands and image data into the display module. Input is only accepted when the display is selected ($\overline{\text{CS}}$ is low).

SERIAL OUTPUT (SO): The SO pin is used to shift data out of the display module. This pin is in a high-impedance state when the display is not selected ($\overline{\text{CS}}$ is high).

SERIAL CLOCK (SCK): The SCK pin is used to clock data in and out of the display module. Input data is latched from SI on the falling edge of SCK and new data is output on SO on the rising edge of SCK.

CHIP SELECT ($\overline{\text{CS}}$): The display module is selected when $\overline{\text{CS}}$ is low. A high-to-low transition on $\overline{\text{CS}}$ signifies the start of a new command packet. A low-to-high transition on $\overline{\text{CS}}$ is required to end the commanded operation.

RESET ($\overline{\text{RESET}}$): A low level on the $\overline{\text{RESET}}$ pin terminates any operation in progress and holds the controller in the reset state. The reset sequence executes when this pin is released to the high state. The display module enters the sleep mode upon termination of the reset sequence. There is no restriction on the $\overline{\text{RESET}}$ pin when powering on the display module. The $\overline{\text{RESET}}$ pin is internally pulled high, so this pin may be left unconnected.

BUSY (BUSY): The BUSY pin is high while the display module is processing a command and also during execution of the reset sequence. The BUSY pin must be low before the display may be selected ($\overline{\text{CS}}$ set low). After receiving a command packet, the display module requires $\overline{\text{CS}}$ to return high before the operation can complete and BUSY returns low. The display module is immediately ready for a new command packet when BUSY returns low. Module status may also be polled using the serial interface, which makes use of this pin optional.

3.3.2 Power Supply

LOGIC SUPPLY (V_{CC}): The V_{CC} pin provides regulated 3.3V power to the display module control logic, memory, and drivers.

POWER SUPPLY (V_{PWR}): The V_{PWR} pin provides DC power to the bias supply used to drive the ChLCD. For maximum efficiency, this supply may be unregulated. This pin draws zero current in sleep mode.

GROUND (V_{SS}): The V_{SS} pin provides the return path for both V_{CC} and V_{PWR}.

4 Operating Principles

4.1 Bistability

The unique bistable property of ChLCD products means that an image placed on the display will remain indefinitely without the need for refreshing. This bistability has implications both for managing power consumption and for managing screen image content.

Display modules contain an onboard RAM into which image data is loaded using the SPI-compatible interface. Due to the bistability of the display, there is no continuous refresh and changes to the image data in the RAM do not automatically appear on the display. The displayed image only changes in response to the display update commands (see Section 6.3). The DISP_FULLSCRN and DISP_PARTSCRN commands are used, respectively, to update the entire display or a section of the display using image data stored in the RAM. The entire 32 KB RAM space is available to the application. The RAM is larger than required to hold a single full screen image and may be partitioned in any manner suitable to the application. Both update commands accept the starting address for the image data as an argument.

The display module contains the LCD bias supply that generates the 30 to 40 volts necessary to drive the display. This supply is normally on and drawing current from V_{PWR} when the display is idle. By leaving the bias supply on, the display can begin an update in a relatively short time (t_{HVCCHG}). A longer time is required (t_{HVCON}) to begin an update when the bias supply requires initialization. However, considerable power can be saved for infrequent display updates by using the sleep mode (see SLEEP, Section 6.4.1). The bias supply is disabled in sleep mode, with the result that the current drawn from V_{PWR} goes to zero. Note that the contents of the image RAM are preserved in sleep mode.

4.2 Serial Interface

The display module functions as a SPI slave device. The master selects the display for communication using the $\overline{CS}$ line and provides the clock signal (SCK) used to clock data in and out of the display module. All new command packets to the display begin with a high-to-low transition on $\overline{CS}$. The $\overline{CS}$ line must remain low until the command and all arguments are clocked into the display, at which time it is to return high. New data (commands or arguments) for the display are placed on SI on rising edges of SCK, and the display latches the data on the falling edge of SCK. The display places new output data on SO on rising edges of SCK for reading by the master on the falling edge. Thus, the display will output a byte of data on SO for every byte of data clocked in on SI. Transmission of each byte begins with the most significant bit (MSB) and ends with the least significant bit (LSB).

Figure 1 illustrates the basic interface timing for sending a command packet to the display module. The command is always the first byte clocked in following the high-to-low transition on $\overline{CS}$. The command arguments, numbered 1 to N, are clocked in next. Some commands have no arguments while others have many. The first byte output by the slave, numbered 0, clocks synchronously with the command byte. Slave output bytes 1 through N are clocked synchronously with the respective argument numbered 1 to N. See Section 5.5 for detailed timing information.

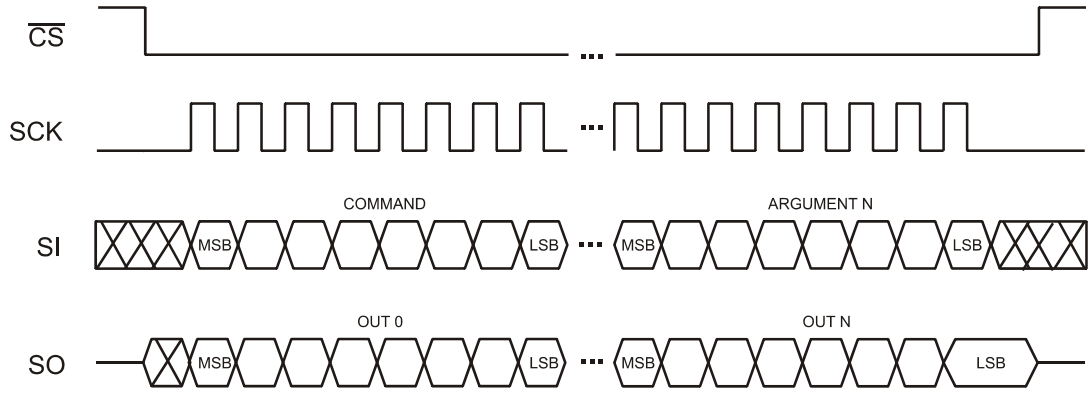


Figure 1: Basic Serial Interface Timing

Two alternative methods exist for determining the display module's readiness to accept new commands. The first method requires monitoring the BUSY signal (pin 2), while the second method requires using the serial interface to poll the display module's status register.

BUSY Signal:

Display modules output a BUSY signal (pin 2) that indicates the readiness of the display to accept new commands. A high on the BUSY pin indicates that the display is currently processing a previous command (or executing the reset sequence) and no new commands will be accepted. The master device must wait for the BUSY line to return low before asserting $\overline{CS}$ low to send a new command packet. Once $\overline{CS}$ is asserted low, the command and all of its arguments may be clocked in without regard to the BUSY line. Note that the $\overline{CS}$ line must return high after the entire command is clocked in. The BUSY line will not return low again, freeing up the display to execute additional commands, until after $\overline{CS}$ returns high.

Serial Polling:

The display status may alternatively be determined using the serial interface. This approach has the advantage of saving the I/O resource required by the BUSY line. However, the interface is more complex and the SPI port will be in use for longer durations. First, the commands are partitioned into those with fixed execution times and those with variable execution times. The variable execution time commands require special monitoring for completion. The fixed execution time commands require no special monitoring and permit the display module to be deselected ($\overline{CS}$ high) immediately after the command packet is transmitted.

The procedure for variable execution time commands with serial polling is detailed as follows. The $\overline{CS}$ line to the display module is asserted low and the command and arguments are clocked in. Following the command and arguments, additional dummy bytes are clocked in (with $\overline{CS}$ remaining low). The display module's status register is output (on SO) with every byte. The high order bit of the status register indicates the busy status of the display module. This bit is a '1' while the display is busy, and a '0' when the operation is complete and the display is not busy. Note that the output pipeline of the display module requires three output bytes after the operation is complete for the not busy status to appear. The display may be deselected ($\overline{CS}$ high) once the status byte containing the '0' busy bit is received.

Two additional signal timing constraints, t_{CS} and t_{SCK2CS}, are required for the serial polling method. These constraints are automatically satisfied when the BUSY signal is used. The first parameter, t_{CS}, is the minimum time that $\overline{CS}$ must be high between any two command packets. The second parameter, t_{SCK2CS}, is the minimum time from the falling edge of SCK on the last bit in a command packet until the high-to-low transition on $\overline{CS}$ that begins a new command packet. These two constraints must be satisfied for all command packets (both fixed and variable execution time commands).

4.3 Power On and Reset

The display module executes an internal reset sequence in response to hardware and software resets and also at power on. A hardware reset is triggered when the $\overline{\text{RESET}}$ pin returns high after being held low for a minimum of t_{RST}. Software resets are triggered by the RESET command (see Section 6.4.2). The BUSY pin may be monitored to determine when the reset sequence has completed and the display module is ready to accept new command packets. For applications where the BUSY line is not connected (serial polling of display module status is implemented), it is necessary to wait for a period of t_{RESET} after triggering the reset sequence before issuing new command packets to the display module. The display module is in the sleep mode upon completion of the reset sequence.

4.4 Electronic Erase (Pressure Point Removal)

Application of external pressure to the display module glass or PCB may produce visual non-uniformities as a result of liquid crystal flow. These non-uniformities, called pressure points, typically appear as bright spots. Some pressure points can be removed by updating the display using the Display Update Commands (see Section 6.3), but some pressure points that result from higher pressures cannot. In particular, the interpixel area cannot be driven to the dark state using the Display Update Commands.

The electronic erase command (see ELEC_ERASE, Section 6.4.5) may be used to completely remove pressure points from the active area of the display. This command leaves all pixels in the bright state with the interpixel area in the dark state. This command is provided to assist OEM customers in assembling the display modules into their devices. An electronic erase command may be issued after final product assembly in order to clear any pressure points created in handling and mounting the displays. This command should only be used for the infrequent removal of pressure points, not for erasing the display during normal operation, as extensive use of this command may shorten the operating lifetime of the display.

4.5 Active Frame

The active (drivable) area of the display is slightly smaller than the glass substrates that form the display. The inactive portion of the glass should generally not be visible in the final product assembly as the electronic erase is unable to remove pressure points in this area. Display modules include an active frame that enables creation of a pressure-point free border around the image content area of the display. The active frame consists of a five-pixel wide border, which is controlled in the same manner as normal image data. Suitable framing should be used to partially overlap the active frame and mask off the inactive area. The optional bezel may be used for this purpose.

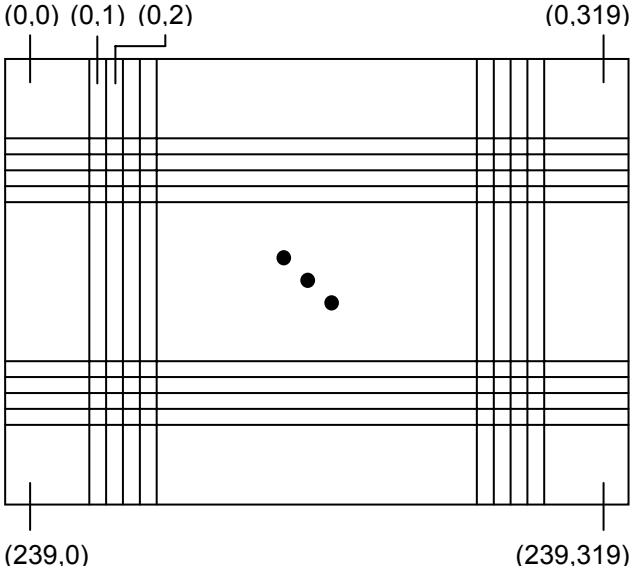


Figure 2: Active Area of the 320x240 Display.

Figure 2 illustrates the row and column numbering as well as the active frame for the 320x240 display module. These modules have 320 columns, numbered 0 to 319, and 240 rows, numbered 0 to 239. Note that the first (0) and last (319) columns appear five pixels wide, while the first (0) and last (239) rows appear five pixels tall. Thus, image data destined for these locations is stretched in order to produce the active frame. Typically, image data is selected the same for all active frame locations in order to produce a solid border for the image. Once the active frame is taken into account, 318 columns and 238 rows are available for general image content.

4.6 Image Data

A full screen update of the 320x240 display module requires 9600 bytes (= 240 x 320 pixels x 1 bit/pixel x 1 byte / 8 bits) of image data. The first byte of data defines the leftmost 8 pixels in the top row. Successive bytes map to the next 8 pixels to the right. When the end of a row is reached, the next byte maps to the leftmost 8 pixels of the following row. A bright (on) pixel is a binary one, while a dark (off) pixel is a binary zero. The leftmost pixel encoded in a given byte corresponds to the most significant bit in the byte while the rightmost pixel corresponds to the least significant bit.

Figure 3 illustrates how the byte data maps to the display. The bytes are labeled D0 through D9599, with D0 being the first byte in the image buffer and D9599 the last. Note again that the active frame will cause the data encoded in the first (D0 – D39) and last (D9570 – D9599) rows to appear five pixels high on the display. Also, the single bit that encodes a column 0 pixel will appear five pixels wide as will the single bit that encodes a column 319 pixel.

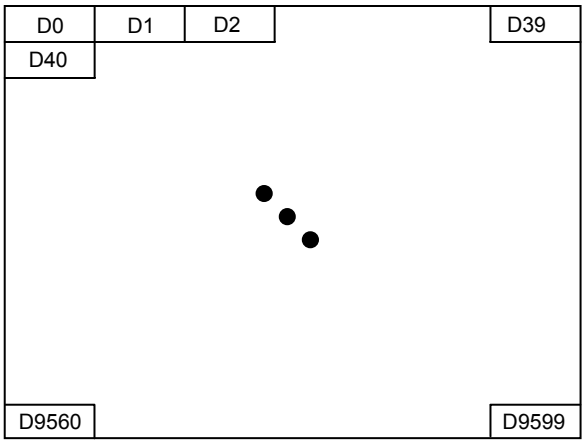


Figure 3: 320x240 Display Screen Location to Image Data Mapping.

Partial screen updates (update a limited number of whole rows; all columns in the row), are also available. The mapping for partial screen updates is similar. However, less data is required (40 bytes times the number of rows to update). For partial screen updates, D0 maps to the upper left corner of the region to be updated rather than the upper left corner of the display.

5 Specifications

5.1 General

Parameter	Description
Display Type	Reflective Cholesteric LCD
Format	320 Columns × 240 Rows (318 x 238 Minus the Active Frame)
Resolution	72 dots per inch, 0.36 mm between pixel centerlines (both horizontal and vertical)
Image Area	113.06 mm × 84.61 mm (Dimensions do not include active frame.)
Display Module Weight	105 grams (Weight is 150 grams with optional bezel.)
Operating Temperature Range	0°C to +60°C
Storage Temperature Range	-30°C to +80°C
Full Image Update Rate	1.85 sec @ 25°C (Ref. graph, 5.2.2)

5.2 Electrical

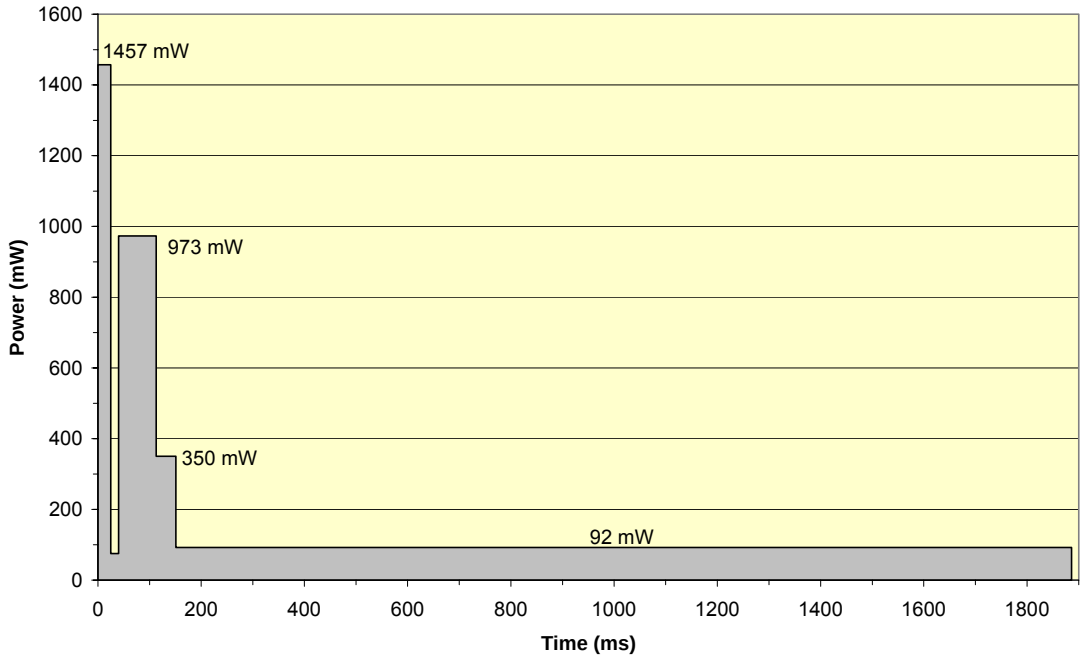
Parameter		Minimum	Typical	Maximum	Units
Logic Supply (V_{CC})[1]		3.0	3.3	3.6	VDC
Power Supply (V_{PWR})		4.0	-	9.0	VDC
High Level Logic Output Voltage (V_{OH})		V_{CC}-0.6	-	V_{CC}	VDC
Low Level Logic Output Voltage (V_{OL})		V_{SS}	-	V_{SS}+0.6	VDC
High Level Logic Input Voltage (V_{IH})		0.8xV_{CC}	-	V_{CC}	VDC
Low Level Logic Input Voltage (V_{IL})		V_{SS}	-	V_{SS}+0.6	VDC
Average Operating Power @25°C (while driving image) [2]	V_{CC}	-	7	-	mW
	V_{PWR}	-	150	-	mW
Average Operating Power @60°C (while driving image) [2]	V_{CC}	-	7	-	mW
	V_{PWR}	-	234	-	mW
Standby Current [2]	V_{CC}	-	156	-	µA
	V_{PWR}	-	13	-	mA
Sleep Current [2]	V_{CC}	-	10	-	µA
	V_{PWR}	-	0	1	µA

[1] V_{CC} must rise/fall with a slope ≥ 1V/ms. If this requirement can not be satisfied, the $\overline{\text{RESET}}$ pin must be asserted low while $V_{CC} \leq 2.7V$.

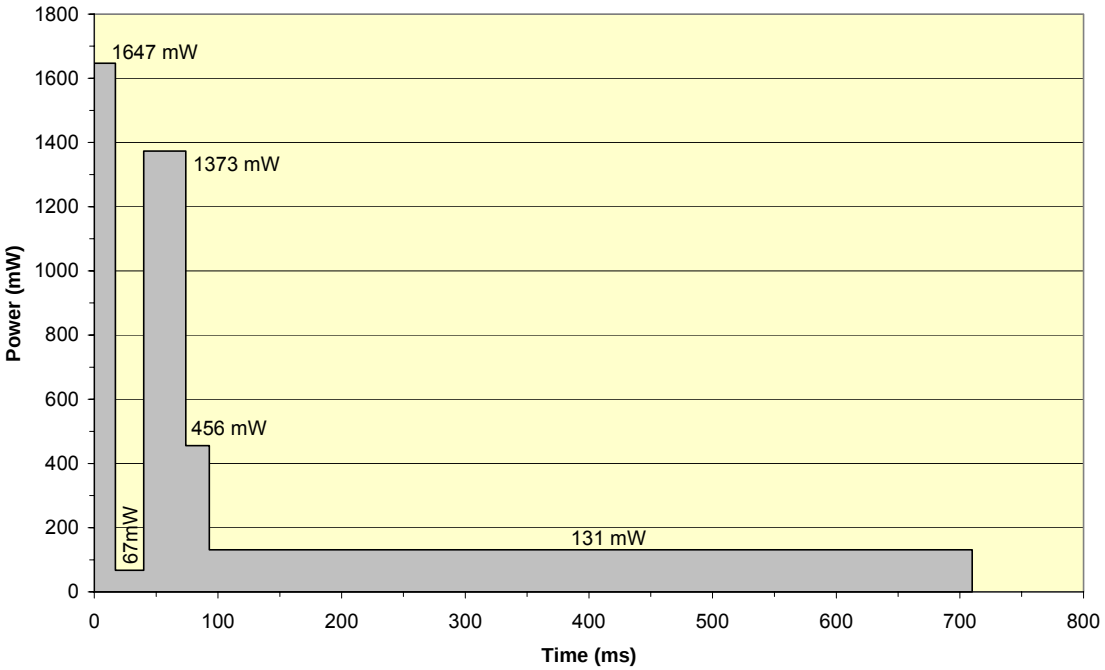
[2] Test Conditions: V_{CC} = 3.3V and V_{PWR} = 5.0V.

5.2.1 Update Cycle Power Profiles

320x240 SPI Display Module Update Cycle Power @25°C

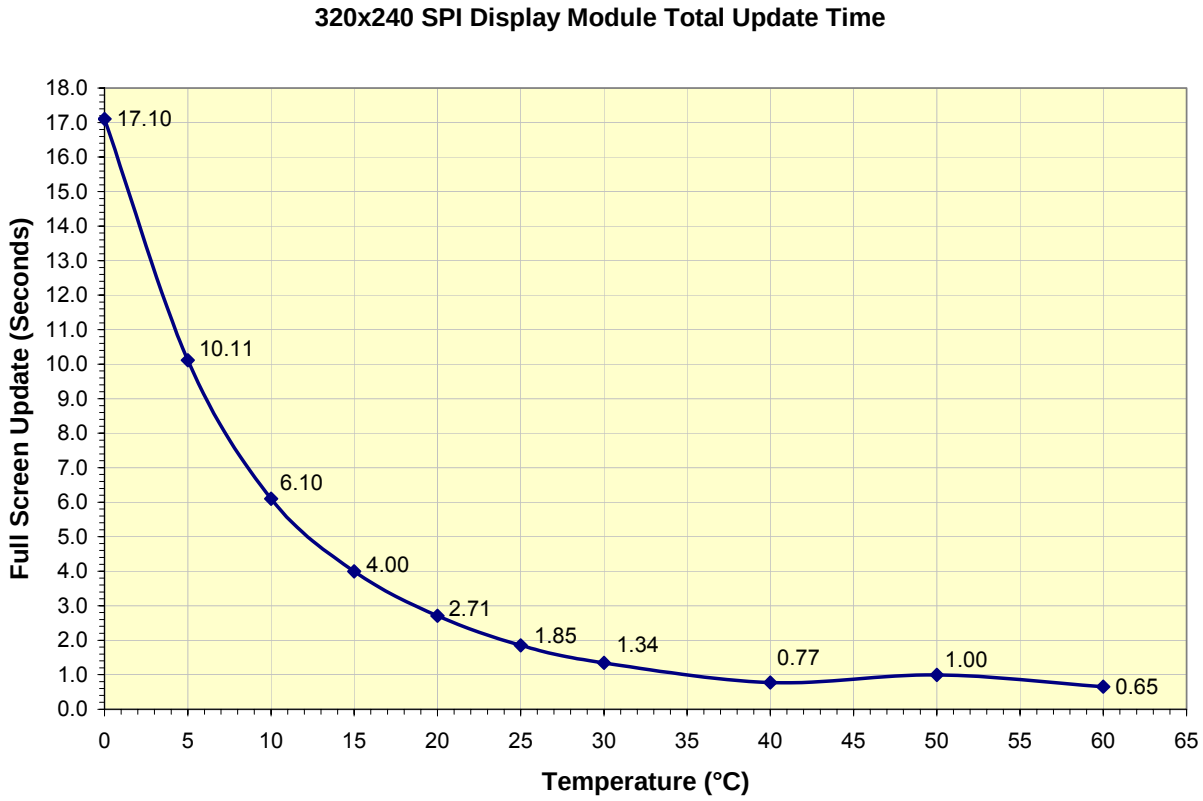


320x240 SPI Display Module Update Cycle Power @60°C



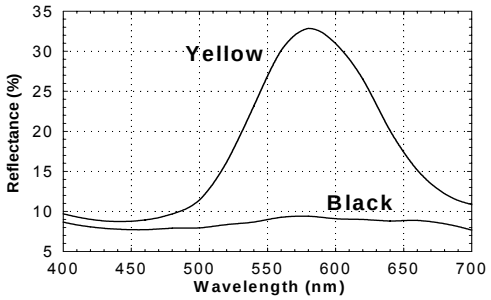
Note: Graphs above represent power required for a single full screen update. Initial power surge corresponds to capacitive loading in power supply circuit. Average power consumed during display update is 150 mW at 25°C and 234 mW at 60°C. Test Conditions: V_{CC} = 3.3V and V_{PWR} = 5.0V.

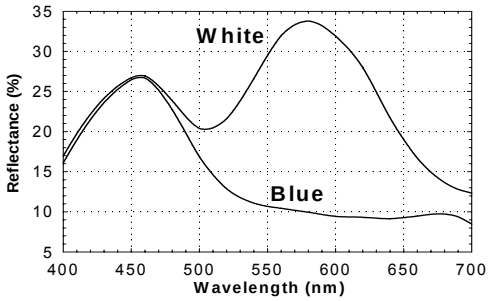
5.2.2 Update Cycle Temperature Performance

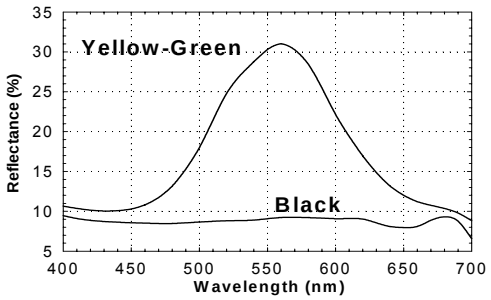


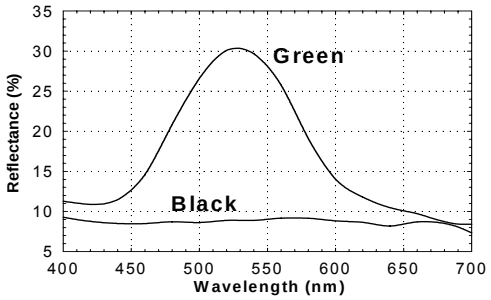
The chart above illustrates average computed full screen update times with respect to temperature for the 320×240 SPI display module (Blue/White). The update time is approximately 1.85 seconds at room temperature (25°C).

5.3 Optical



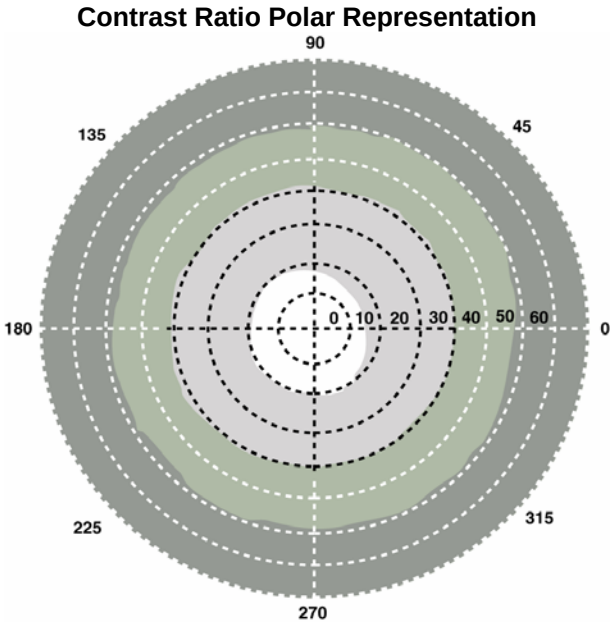






The above reflectance curves are from a single pixel. Actual reflectance will vary depending on display resolution, aperture ratio, and other factors.

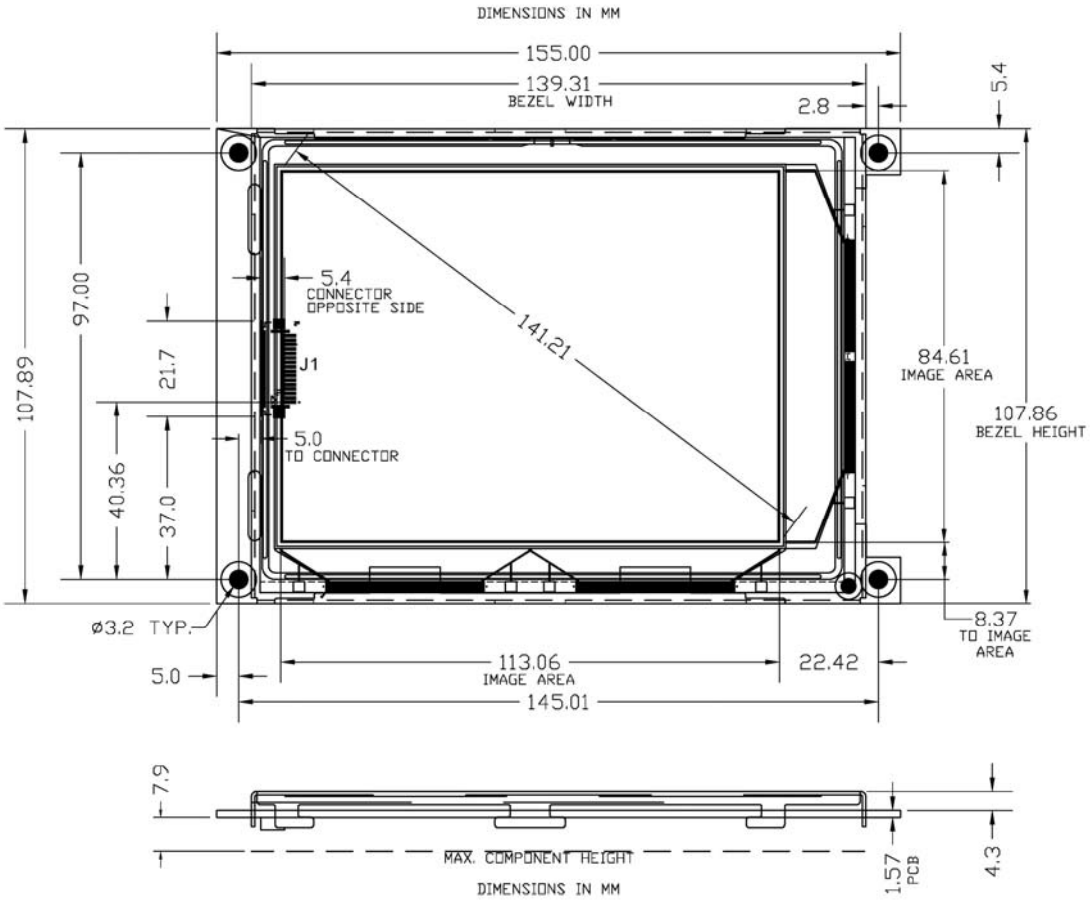
The graphs to the left outline the spectral reflectance characteristics for a given display pixel when switched to either of the two possible stable states: reflective planar or transparent focal conic. The top line in each chart outlines the reflective characteristic of the planar state. The bottom line outlines the reflective characteristic of the transparent focal conic state. Graphs for the 4 standard color combinations are illustrated.



As illustrated in the polar graph above, all Kent Displays' ChLCD products have a 360-degree viewing cone. When measured normal to the plane of the display, the monochromatic contrast ratio is as high as 25:1 with a peak reflectivity approaching 35% of the incident light. The contrast ratio reduces as the viewing angle approaches the plane of the display but is still excellent at 11:1. Since no polarizers are used, display contrast reduces uniformly in all azimuthal directions when the viewing angle is increased.

5.4 Mechanical

(Shown with Optional Bezel)



FRONT COVER REQUIREMENTS:

The following front cover requirements are necessary to insure image quality during the life of the 320×240 display module:

1. Cholesteric Liquid Crystal materials require protection from UV light. A UV blocking material with a minimum 98% cutoff at 380nm and lower spectral components is required.

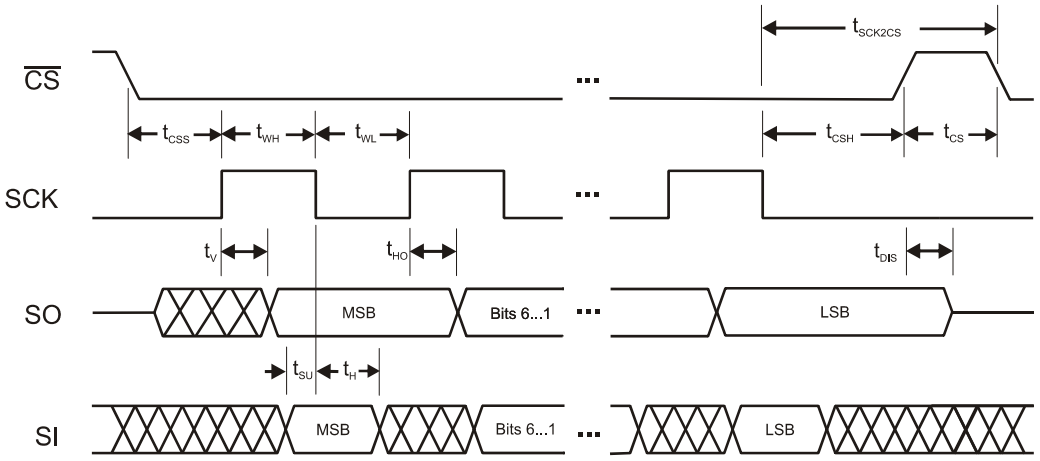
2. The finished product design should incorporate a transparent cover such as acrylic, polycarbonate, etc., to protect the viewing area of the display. Place the protective cover as close to the display module as possible. The protective cover should be of sufficient thickness to resist flexing, or if flexed should not touch the surface of the display. Acrylite® OP-3 P-99 matte finish and Acrylite® OP-3 material without matte finish are examples of a recommended protective cover material.

Adding an anti-glare and/or anti-reflective surface film or finish (e.g. Acrylite® OP-3 P-99) to the viewing side of the protective cover may improve the optical performance in certain display applications and lighting conditions.

5.5 Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	SCK Frequency	-	250	kHz
t_{WH}	SCK High Time	tbd[1]	-	ns
t_{WL}	SCK Low Time	tbd[1]	-	ns
t_{CS}	$\overline{CS}$ High Time	40	-	µs
t_{SCK2CS}	Last Data SCK to $\overline{CS}$ Low Time	60	-	µs
t_{CSS}	$\overline{CS}$ Setup Time	tbd[1]	-	ns
t_{CSH}	$\overline{CS}$ Hold time	tbd[1]	-	ns
t_{SU}	Data In Setup Time	tbd[1]	-	ns
t_H	Data In Hold Time	tbd[1]	-	ns
t_{HO}	Output Hold Time	-	tbd[1]	ns
t_{DIS}	Output Disable Time	-	tbd[1]	ns
t_V	Output Valid	-	tbd[1]	ns
t_{RST}	$\overline{RESET}$ Pulse Width	2	-	µs
t_{RESET}	Duration of Reset Sequence	-	1	S
t_{HVCON}	Bias Supply Initialization Time	-	60	ms
t_{HVCCHG}	Bias Supply Change Time	-	17	ms

[1] - Texas Instruments micro-controller (MSP430-F135) data pending.



6 Instruction Set

6.1 Overview

Function	Command	Hex	Description	Details	
				# of Bytes	Section
Memory	WRITE	00	Write byte data to RAM.	4+	6.2.1
	FILL[1]	01	Fill RAM with single byte.	6	6.2.2
	READ	04	Read byte data from RAM.	6+	6.2.3
	CLEAR_BITS	08	Clear bits in RAM.	4	6.2.4
	SET_BITS	09	Set bits in RAM.	4	6.2.5
	XOR_BITS	0A	Exclusive-Or bits in RAM.	4	6.2.6
Display	CLR_DISP_BRT[1]	10	Clear display bright.	1	6.3.1
	CLR_DISP_BRT_IB[1]	11	Clear display bright with inverted border.	1	6.3.2
	CLR_DISP_DRK[1]	12	Clear display dark.	1	6.3.3
	CLR_DISP_DRK_IB[1]	13	Clear display dark with inverted border.	1	6.3.4
	CLR_SECT_BRT[1]	14	Clear display section bright.	5	6.3.5
	CLR_SECT_BRT_IB [1]	15	Clear display section bright with inverted border.	5	6.3.6
	CLR_SECT_DRK[1]	16	Clear display section dark.	5	6.3.7
	CLR_SECT_DRK_IB[1]	17	Clear display section dark with inverted border.	5	6.3.8
	DISP_FULLSCRN[1]	18	Update entire display.	3	6.3.9
	DISP_PARTSCRN[1]	19	Update display section.	7	6.3.10
System	SLEEP	20	Enter low-power sleep mode.	1	6.4.1
	RESET[2]	24	Software reset.	1	6.4.2
	GET_FW_VERSION	26	Get firmware version.	36	6.4.3
	SET_CONTRAST	27	Set display contrast.	2	6.4.4
	ELEC_ERASE[1]	2A	Electronic erase (Clear pressure points).	1	6.4.5

[1] – Variable Execution Time Command
[2] – The RESET command requires an additional delay (t_{RESET}) after being issued if the serial status polling method is used.

6.2 Memory Access Commands

The display module contains onboard image RAM that may be read from or written to using the memory access commands.

6.2.1 WRITE

This command provides byte-level write access to the display module's onboard image RAM. The command requires a minimum of 3 arguments.

(CMD)	0x00:	The command.
(ARG1)	ADDRESSH:	High byte of the target memory address.
(ARG2)	ADDRESSL:	Low byte of the target memory address.
(ARG3)	DATA:	The value to be written.

Data can be written to successive addresses by including more arguments. For instance, the optional argument ARG4 would contain the value to write to address <ARG1:ARG2> + 1. This feature permits the efficient transfer of an entire image to the display RAM. The low-to-high transition on $\overline{CS}$ signals to the controller that the last byte of data has been written.

6.2.2 FILL

This command fills an entire region of the display module's onboard image RAM with a given value. The use of this command with a fill value of 0x00 or 0xFF is the recommended method of clearing an image buffer. The command has 5 arguments.

(CMD)	0x01:	The command.
(ARG1)	STARTH:	High byte of the first address in the fill region.
(ARG2)	STARTL:	Low byte of the first address in the fill region.
(ARG3)	ENDH:	High byte of the last address in the fill region.
(ARG4)	ENDL:	Low byte of the last address in the fill region.
(ARG5)	FILL_VALUE:	Value to write to all memory locations in the region.

This is a variable execution time command.

6.2.3 READ

This command provides byte-level read access to the display module's onboard image RAM. The command requires a minimum of 5 arguments.

(CMD)	0x04:	The command.
(ARG1)	ADDRESSH	High byte of the memory address to read.
(ARG2)	ADDRESSL:	Low byte of the memory address to read.
(ARG3)	DUMMY1:	Don't care.
(ARG4)	DUMMY2:	Don't care.
(ARG5)	DUMMY3:	Don't care.

The display module will output (on SO) the contents of the memory location encoded in ARG1 and ARG2 (mem(<ARG1:ARG2>)) during receipt of ARG5. Additional dummy arguments may be used to obtain the contents of successive memory locations. For example, during optional dummy argument ARG6, the display module outputs mem(<ARG1:ARG2>+1). The low-to-high transition on $\overline{CS}$ signals to the controller that the last byte of data has been read.

6.2.4 CLEAR_BITS

This command provides the ability to clear (set to 0) individual bits in the display module's onboard image RAM. A bit mask is used to specify which bits at a given memory address should be cleared. A one in the mask indicates that the corresponding bit should be cleared, while a zero indicates that the corresponding bit should be left unaffected. The command has 3 arguments.

(CMD)	0x08:	The command.
(ARG1)	ADDRESSH:	High byte of the memory address to modify.
(ARG2)	ADDRESSL:	Low byte of the memory address to modify.
(ARG3)	MASK:	The bit mask.

This command is useful for generating dark text or drawing with a dark pen directly to image RAM.

6.2.5 SET_BITS

This command provides the ability to set (set to 1) individual bits in the display module's onboard image RAM. A bit mask is used to specify which bits at a given memory address should be set. A one in the mask indicates that the corresponding bit should be set, while a zero indicates that the corresponding bit should be left unaffected. The command has 3 arguments.

(CMD)	0x09:	The command.
(ARG1)	ADDRESSH:	High byte of the memory address to modify.
(ARG2)	ADDRESSL:	Low byte of the memory address to modify.
(ARG3)	MASK:	The bit mask.

This command is useful for generating bright text or drawing with a bright pen directly to image RAM.

6.2.6 XOR_BITS

This command provides the ability to toggle (exclusive-or) individual bits in the display module's onboard image RAM. A bit mask is used to specify which bits at a given memory address should be toggled. A one in the mask indicates that the corresponding bit should be toggled, while a zero indicates that the corresponding bit should be left unaffected. The command has 3 arguments.

(CMD)	0x0A:	The command.
(ARG1)	ADDRESSH:	High byte of the memory address to modify.
(ARG2)	ADDRESSL:	Low byte of the memory address to modify.
(ARG3)	MASK:	The bit mask.

This command is useful for generating text or drawing directly to image RAM without regard to the background color.

6.3 Display Update Commands

The display update commands drive new image data to the display.

6.3.1 CLR_DISP_BRT

This command clears the entire display, including the active frame, to the bright state. There are no arguments.

(CMD)	0x10:	The command.

This is a variable execution time command.

6.3.2 CLR_DISP_BRT_IB

This command clears the entire display, less the active frame, to the bright state. The active frame is set to the dark state, i.e. the border is inverted. There are no arguments.

(CMD)	0x11:	The command.

This is a variable execution time command.

6.3.3 CLR_DISP_DRK

This command clears the entire display, including the active frame, to the dark state. There are no arguments.

(CMD)	0x12:	The command.

This is a variable execution time command.

6.3.4 CLR_DISP_DRK_IB

This command clears the entire display, less the active frame, to the dark state. The active frame is set to the bright state, i.e. the border is inverted. There are no arguments.

(CMD)	0x13:	The command.

This is a variable execution time command.

6.3.5 CLR_SECT_BRT

This command clears a given section of the display to the bright state. The section is defined by the first and last rows (numbered 0 to 239). Any part of the active frame (left/right and top/bottom) in the defined section is also set to the bright state. The maximum number of rows that may be cleared using this command is 120. The command has 4 arguments.

(CMD)	0x14:	The command.
(ARG1)	FIRSTH:	High byte of the first row to clear.
(ARG2)	FIRSTL:	Low byte of the first row to clear
(ARG3)	LASTH:	High byte of the last row to clear.
(ARG4)	LASTL:	Low byte of the last row to clear.

This is a variable execution time command.

6.3.6 CLR_SECT_BRT_IB

This command clears a given section of the display, less the active frame, to the bright state. The section is defined by the first and last rows (numbered 0 to 239). Any part of the active frame (left/right and top/bottom) in the defined section is set to the dark state, i.e. the border is inverted. The maximum number of rows that may be cleared using this command is 120. The command has 4 arguments.

(CMD)	0x15:	The command.
(ARG1)	FIRSTH:	High byte of the first row to clear.
(ARG2)	FIRSTL:	Low byte of the first row to clear
(ARG3)	LASTH:	High byte of the last row to clear.
(ARG4)	LASTL:	Low byte of the last row to clear.

This is a variable execution time command.

6.3.7 CLR_SECT_DRK

This command clears a given section of the display to the dark state. The section is defined by the first and last rows (numbered 0 to 239). Any part of the active frame (left/right and top/bottom) in the defined section is also set to the dark state. The maximum number of rows that may be cleared using this command is 120. The command has 4 arguments.

(CMD)	0x16:	The command.
(ARG1)	FIRSTH:	High byte of the first row to clear.
(ARG2)	FIRSTL:	Low byte of the first row to clear
(ARG3)	LASTH:	High byte of the last row to clear.
(ARG4)	LASTL:	Low byte of the last row to clear.

This is a variable execution time command.

6.3.8 CLR_SECT_DRK_IB

This command clears a given section of the display, less the active frame, to the dark state. The section is defined by the first and last rows (numbered 0 to 239). Any part of the active frame (left/right and top/bottom) in the defined section is set to the bright state, i.e. the border is inverted. The maximum number of rows that may be cleared using this command is 120. The command has 4 arguments.

(CMD)	0x17:	The command.
(ARG1)	FIRSTH:	High byte of the first row to clear.
(ARG2)	FIRSTL:	Low byte of the first row to clear
(ARG3)	LASTH:	High byte of the last row to clear.
(ARG4)	LASTL:	Low byte of the last row to clear.

This is a variable execution time command.

6.3.9 DISP_FULLSCRN

This command triggers a full screen update from a specified image buffer in the onboard image RAM. The command has 2 arguments.

(CMD)	0x18:	The command.
(ARG1)	ADDRESSH:	High byte of the image buffer starting address.
(ARG2)	ADDRESSL:	Low byte of the image buffer starting address.

This is a variable execution time command.

6.3.10 DISP_PARTSCRN

This command triggers a partial screen update from a specified image buffer in the onboard image RAM to a specified group of rows (numbered 0 to 239). The maximum number of rows permitted in a single partial screen update is 120. The command has 6 arguments.

(CMD)	0x19:	The command.
(ARG1)	ADDRESSH:	High byte of the image buffer starting address.
(ARG2)	ADDRESSL:	Low byte of the image buffer starting address.
(ARG3)	FIRSTH:	High byte of the first row to update.
(ARG4)	FIRSTL:	Low byte of the first row to update.
(ARG5)	LASTH:	High byte of the last row to update.
(ARG6)	LASTL:	Low byte of the last row to update.

This is a variable execution time command.

6.4 System Control Commands

The system control commands are used to configure display module operation and obtain display module information and status.

6.4.1 SLEEP

This command puts the display module in the low power sleep mode. There are no arguments.

(CMD)	0x20:	The command.

6.4.2 RESET

This command triggers a software reset of the display module. There are no arguments.

(CMD)	0x24:	The command.

See Section 4.3 for details of the reset sequence.

6.4.3 GET_FW_VERSION

This command retrieves the firmware version of the display module. The firmware version is returned as a fixed-length, NULL terminated ASCII string. The command requires 35 dummy arguments to clock out the version string.

(CMD)	0x26:	The command.
(ARG1)	DUMMY1:	Don't Care
	•	
	•	
	•	
(ARG35)	DUMMY35:	Don't Care

The bytes returned while clocking in the command, ARG1, and ARG2 are to be ignored. The first byte of the version string is returned with ARG3 and continues with subsequent bytes. The version string has the following format:

"FFFFFR-LCID/MMM DD YYYY/HH:MM:SS"

FFFFF:	Firmware identifier.
R:	Revision letter.
LCID:	Liquid crystal material identifier.
MMM:	Compile date month identifier.
DD:	Compile date day identifier.
YYYY:	Compile date year identifier.
HH:	Compile time hour identifier.
MM:	Compile time minute identifier.
SS:	Compile time second identifier.
NULL:	'0'

6.4.4 SET_CONTRAST

This command permits the contrast of the display module to be adjusted. The command has one argument.

(CMD)	0x27:	The command.
(ARG1)	CONTRAST:	The contrast setting.

The contrast setting is a signed 2's complement value. Thus, it can range from –128 to +127. A setting of zero produces the default contrast. This should generally be suitable as the display modules have integrated temperature compensation and are calibrated at the factory. Positive contrast values brighten the display, while negative values darken the display. The magnitude of the contrast value determines the amount of contrast adjustment, with higher magnitudes producing the larger effect.

The contrast setting is stored in RAM and resets to zero when power is cycled or the RESET command is issued.

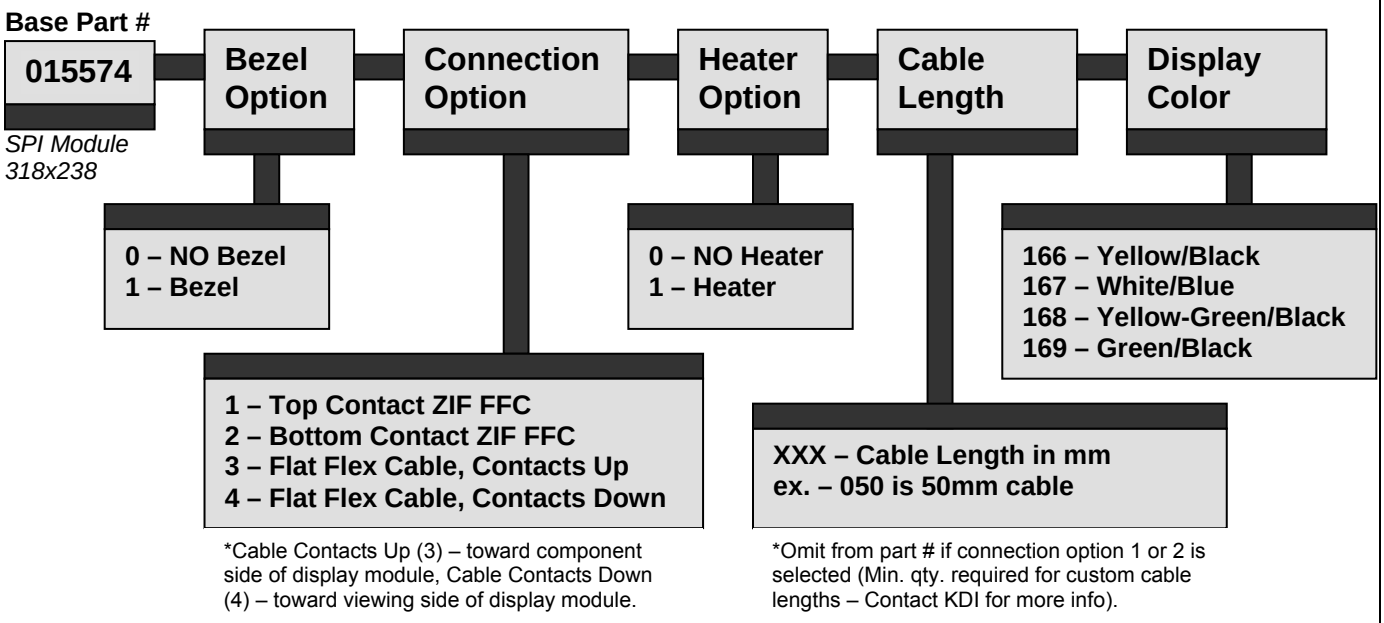
6.4.5 ELEC_ERASE

The electronic erase command removes pressure points from the display (see Section 4.4). There are no arguments. **See the warning in Section 4.4 about the proper use of this command.**

(CMD) 0x2A: The command.

This is a variable execution time command.

7 Ordering Information



*Cable Contacts Up (3) – toward component side of display module, Cable Contacts Down (4) – toward viewing side of display module.

*Omit from part # if connection option 1 or 2 is selected (Min. qty. required for custom cable lengths – Contact KDI for more info).

Sample Part Numbers: **015574110167 –** [SPI Module, 318x238, w/Bezel, Top Contact ZIF FFC, NO Heater, White/Blue]

015574031050167 – [SPI Module, 318x238, NO Bezel, Flat Flex Cable – Contacts Up, Heater, 50mm Cable Length, White/Blue]

015574130050167 – [SPI Module, 318x238, w/Bezel, Flat Flex Cable – Contacts Up, NO Heater, 50mm Cable Length, White/Blue] **This display module is used in the 320x240x5.7 SPI Development Kit.*