HIGH EFFICIENCY SINGLE INDUCTOR BUCK-BOOST CONVERTER WITH 4-A SWITCHES

Check for Samples: TPS63020, TPS63021

FEATURES

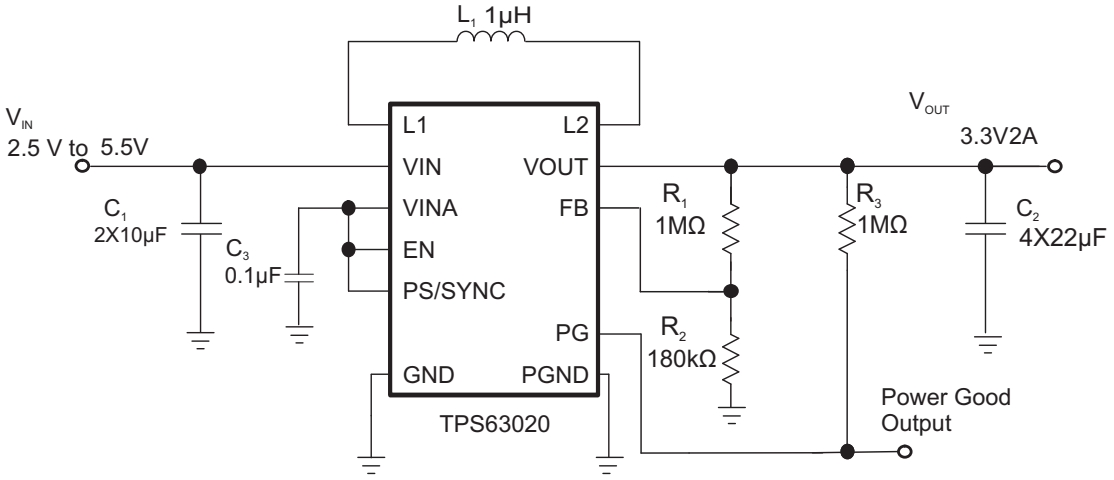
- **Up to 96% Efficiency**
- **3A Output Current at 3.3V in Step Down Mode (VIN = 3.6V to 5.5V)**
- **More than 2A Output Current at 3.3V in Boost Mode (VIN > 2.5V)**
- **Automatic Transition Between Step Down and Boost Mode**
- **Dynamic Input Current Limit**
- **Device Quiescent Current less than 50µA**
- **Input Voltage Range: 1.8V to 5.5V**
- **Fixed and Adjustable Output Voltage Options from 1.2V to 5.5V**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **Forced Fixed Frequency Operation at 2.4MHz and Synchronization Possible**
- **Smart Power Good Output**
- **Load Disconnect During Shutdown**
- **Overtemperature Protection**
- **Overvoltage Protection**
- **Available in a 3 × 4-mm, QFN-14 Package**

APPLICATIONS

- **All Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products**
- **Ultra Mobile PCs and Mobile Internet Devices**
- **Digital Media Players**
- **DSCs and Camcorders**
- **Cellular Phones and Smartphones**
- **Personal Medical Products**
- **Industrial Metering Equipment**
- **High Power LEDs**

DESCRIPTION

The TPS6302x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. Output currents can go as high as 3A while using a single-cell Li-Ion or Li-Polymer Battery, and discharge it down to 2.5V or lower. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters Power Save mode to maintain high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 4A. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 14-pin QFN PowerPAD™ package measuring 3 × 4 mm (DSJ).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTIONS(1)

T_A	OUTPUT VOLTAGE DC/DC	PACKAGE MARKING	PACKAGE	PART NUMBER(2)
–40°C to 85°C	Adjustable	PS63020	14-Pin QFN	TPS63020DSJ
	3.3 V	PS63021		TPS63021DSJ

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, VINA, L1, L2, VOUT, PS/SYNC, EN, FB, PG	–0.3	7	V
Temperature range	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C
ESD rating(3)	Human Body Model - (HBM)		3	kV
	Machine Model - (MM)		200	V
	Charge Device Model - (CDM)		1.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS63020, TPS63021 DSJ 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	41.8	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance	47	
θ_{JB}	Junction-to-board thermal resistance	17	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	16.8	
$\theta_{JC(BOTTOM)}$	Junction-to-case(bottom) thermal resistance	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at VIN, VINA	1.8		5.5	V
Operating free air temperature range, T_A	–40		85	°C
Operating junction temperature range, T_J	–40		125	°C

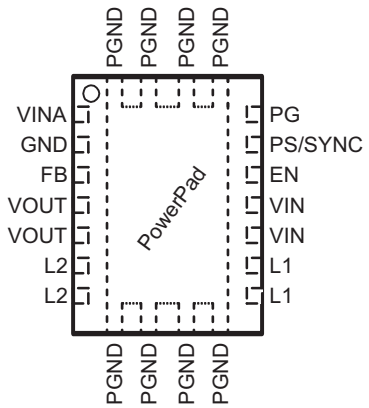
ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			1.8		5.5	V
	Minimum input voltage for startup		0°C ≤ T_A ≤ 85°C	1.5	1.8	1.9	V
	Minimum input voltage for startup			1.5	1.8	2.0	V
V_{OUT}	TPS63020 output voltage range			1.2		5.5	V
	Duty cycle in step down conversion			20%			
V_{FB}	TPS63020 feedback voltage		PS/SYNC = VIN	495	500	505	mV
	TPS63021 output voltage			3.267	3.3	3.333	V
V_{FB}	TPS63020 feedback voltage		PS/SYNC = GND referenced to 500mV	0.6%		5%	
	TPS63021 output voltage regulation		PS/SYNC = GND referenced to 3.3V	0.6%		5%	
	Maximum line regulation				0.5%		
	Maximum load regulation				0.5%		
f	Oscillator frequency			2200	2400	2600	kHz
	Frequency range for synchronization			2200	2400	2600	kHz
I_{SW}	Average switch current limit		V_{IN} = V_{INA} = 3.6 V, T_A = 25°C	3500	4000	4500	mA
	High side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
	Low side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
I_q	Quiescent current	VIN and VINA	I_O = 0 mA, V_{EN} = V_{IN} = V_{INA} = 3.6 V, V_{OUT} = 3.3 V		25	50	µA
		VOUT			5	10	µA
	TPS63021 FB input impedance		V_{EN} = HIGH		1		MΩ
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = V_{INA} = 3.6 V		0.1	1	µA
CONTROL STAGE							
UVLO	Under voltage lockout threshold		V_{INA} voltage decreasing	1.4	1.5	1.6	V
	Under voltage lockout hysteresis				200		mV
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped to GND or VINA		0.01	0.1	µA
	PG output low voltage		V_{OUT} = 3.3 V, I_{PGL} = 10 µA		0.04	0.4	V
	PG output leakage current				0.01	0.1	µA
	Output overvoltage protection			5.5		7	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

PIN ASSIGNMENTS

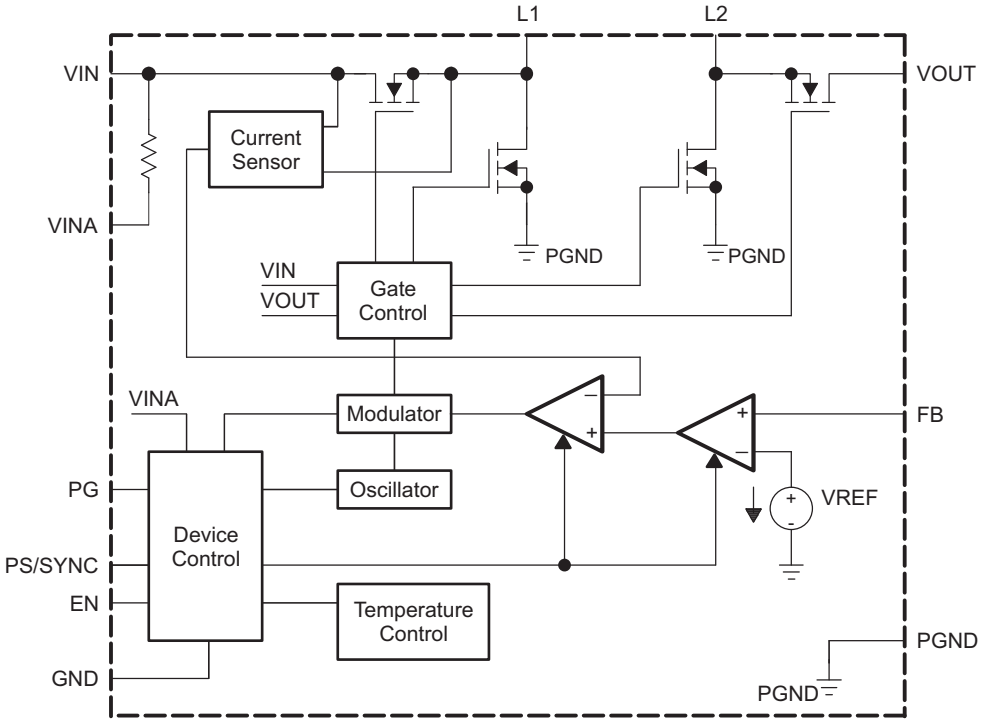
DSJ PACKAGE
(TOP VIEW)



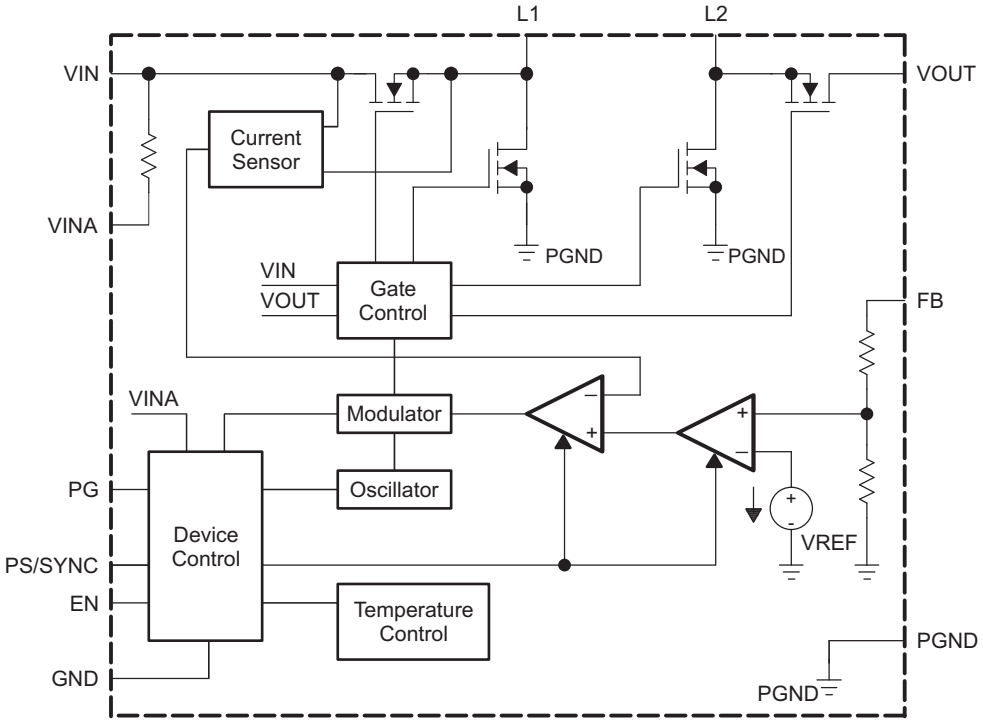
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	12	I	Enable input (1 enabled, 0 disabled) , must not be left open
FB	3	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	2		Control / logic ground
L1	8, 9	I	Connection for inductor
L2	6, 7	I	Connection for inductor
PS/SYNC	13	I	Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization), must not be left open
PG	14	O	Output power good (1 good, 0 failure; open drain)
PGND	PowerPAD™		Power ground
VIN	10, 11	I	Supply voltage for power stage
VOUT	4, 5	O	Buck-boost converter output
VINA	1	I	Supply voltage for control stage
PowerPAD™			Must be connected to PGND. Must be soldered to achieve appropriate power dissipation.

FUNCTIONAL BLOCK DIAGRAM (TPS63020)



FUNCTIONAL BLOCK DIAGRAM (TPS63021)



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

DESCRIPTION		FIGURE
Maximum output current	vs Input voltage (TPS63020, V_{OUT} = 2.5 V / V_{OUT} = 4.5 V)	1
	vs Input voltage (TPS63021, V_{OUT} = 3.3V)	2
Efficiency	vs Output current (TPS63020, Power Save Enabled, V_{OUT} = 2.5 V / V_{OUT} = 4.5 V)	3
	vs Output current (TPS63020, Power Save Disabled, V_{OUT} = 2.5V / V_{OUT} = 4.5V)	4
	vs Output current (TPS63021, Power Save Enabled, V_{OUT} = 3.3V)	5
	vs Output current (TPS63021, Power Save Disabled, V_{OUT} = 3.3V)	6
	vs Input voltage (TPS63020, Power Save Enabled, V_{OUT} = 2.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	7
	vs Input voltage (TPS63020, Power Save Enabled, V_{OUT} = 4.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	8
	vs Input voltage (TPS63020, Power Save Disabled, V_{OUT} = 2.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	9
	vs Input voltage (TPS63020, Power Save Disabled, V_{OUT} = 4.5V, I_{OUT} = {10; 500; 1000; 2000 mA})	10
	vs Input voltage (TPS63021, Power Save Enabled, V_{OUT} = 3.3V, I_{OUT} = {10; 500; 1000; 2000 mA})	11
	vs Input voltage (TPS63021, Power Save Disabled, V_{OUT} = 3.3V, I_{OUT} = {10; 500; 1000; 2000 mA})	12
Output voltage	vs Output current (TPS63020, V_{OUT} = 2.5 V)	13
	vs Output current (TPS63020, V_{OUT} = 4.5 V)	14
	vs Output current (TPS63021, V_{OUT} = 3.3V)	15
Waveforms	Load transient response (TPS63021, VI_N < V_{OUT}, Load change from 500 mA to 1500 mA)	16
	Load transient response (TPS63021, V_{IN} > V_{OUT}, Load change from 500 mA to 1500 mA)	17
	Line transient response (TPS63021, V_{OUT} = 3.3V, I_{OUT} = 1500 mA)	18
	Startup after enable (TPS63021, V_{OUT} = 3.3V, V_{IN} = 2.4V, I_{OUT} = 1500mA)	19
	Startup after enable (TPS63021, V_{OUT} = 3.3V, V_{IN} = 4.2V, I_{OUT} = 1500mA)	20

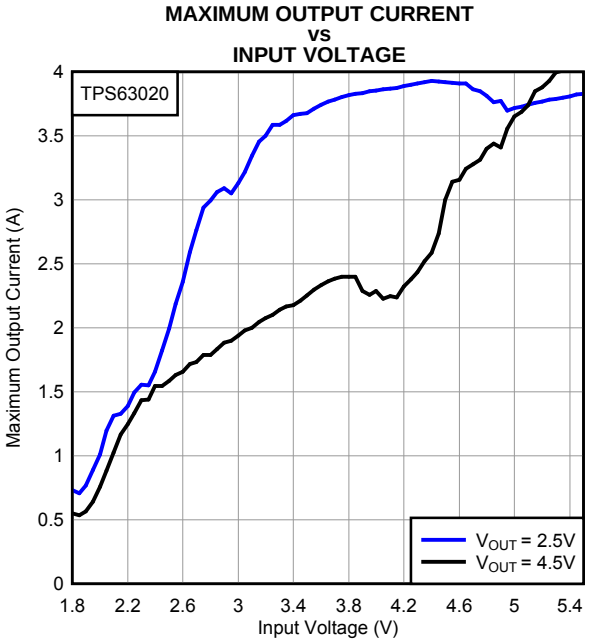


Figure 1.

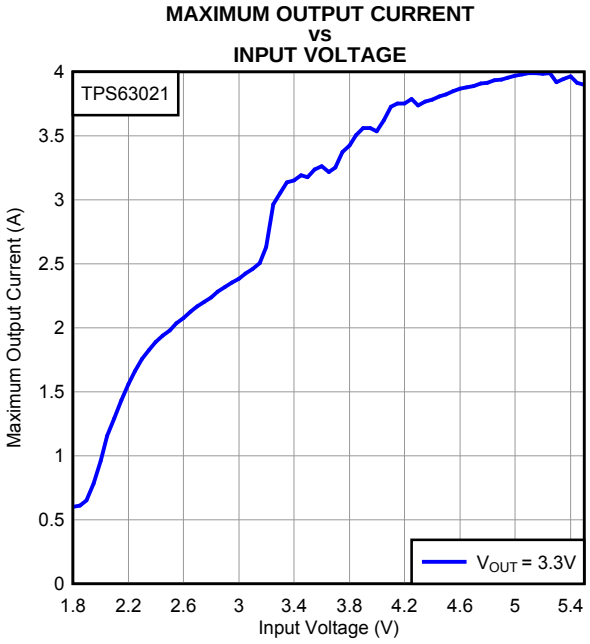


Figure 2.

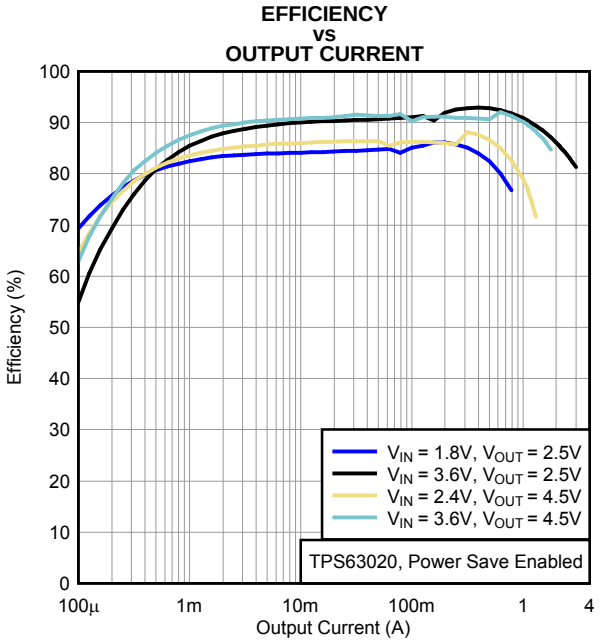


Figure 3.

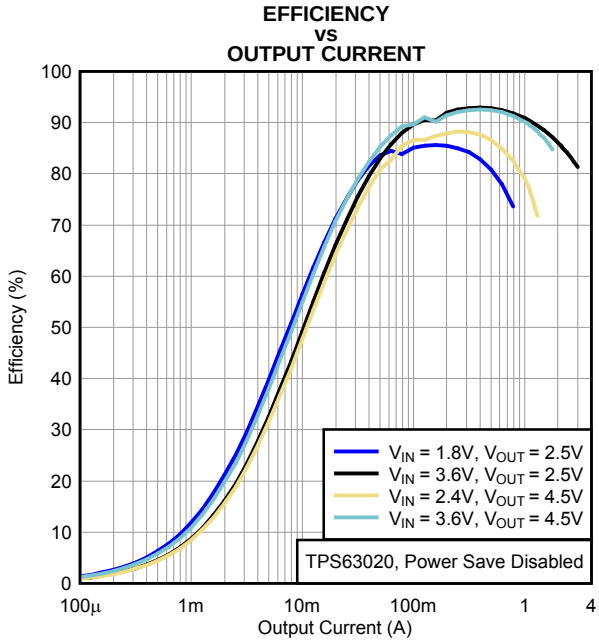


Figure 4.

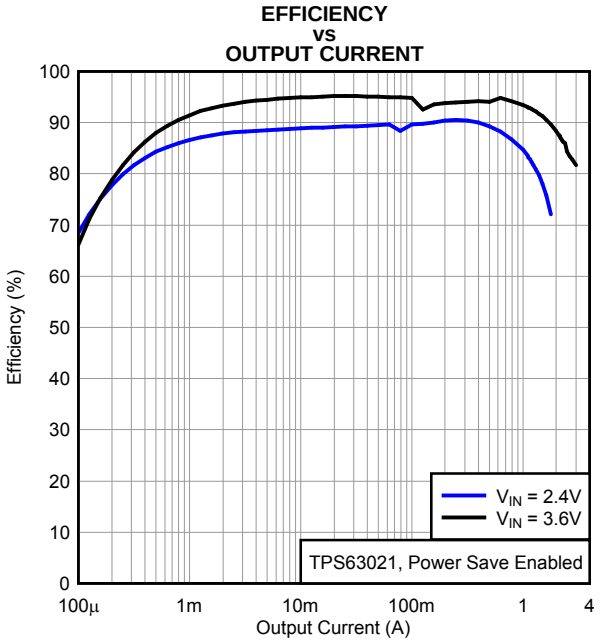


Figure 5.

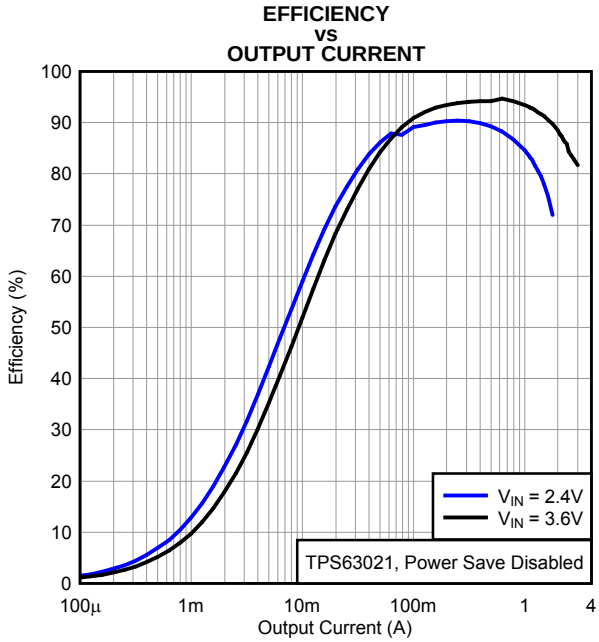


Figure 6.

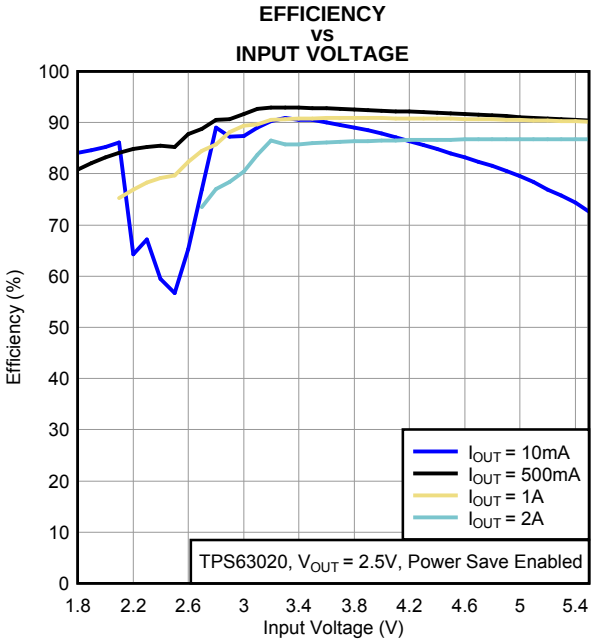


Figure 7.

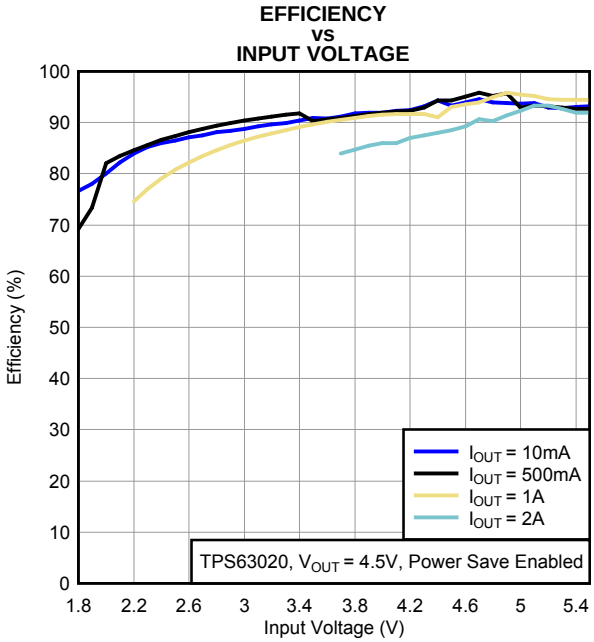


Figure 8.

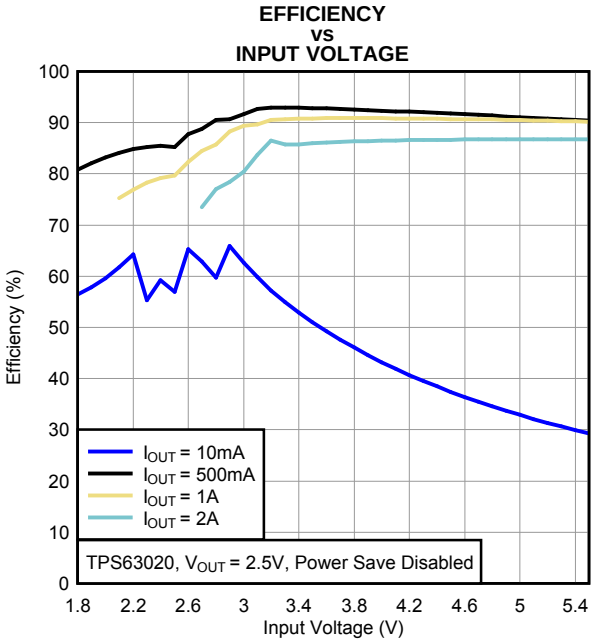


Figure 9.

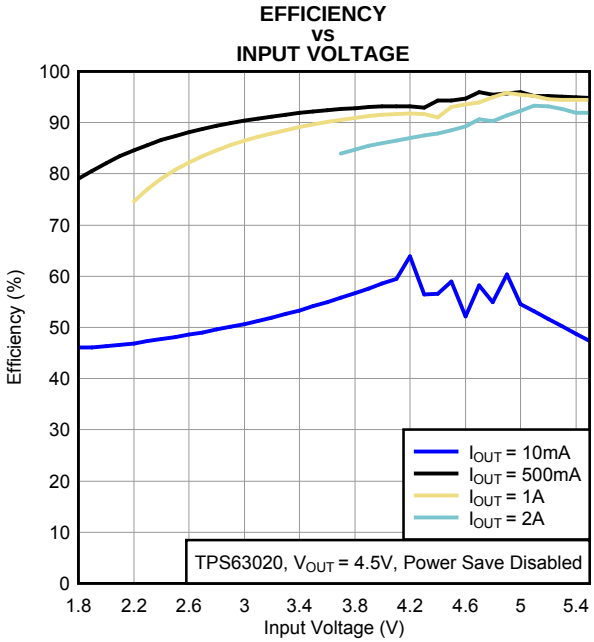


Figure 10.

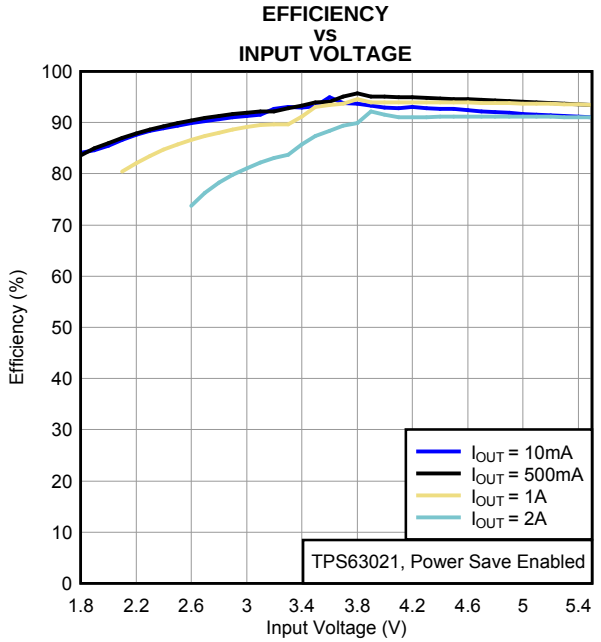


Figure 11.

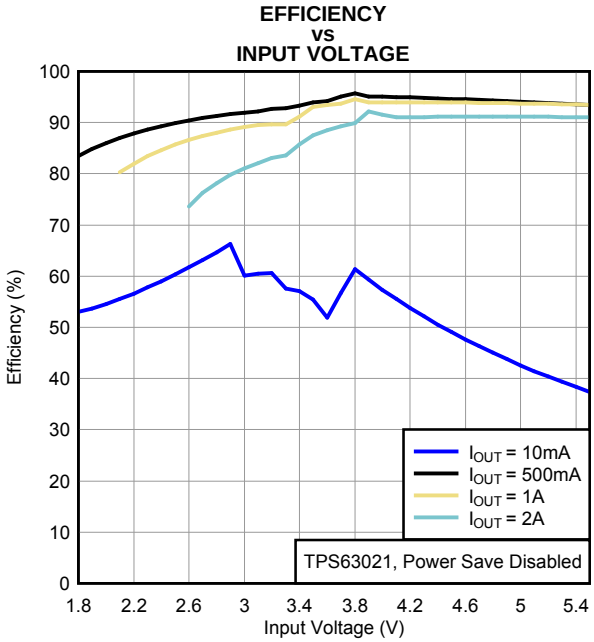


Figure 12.

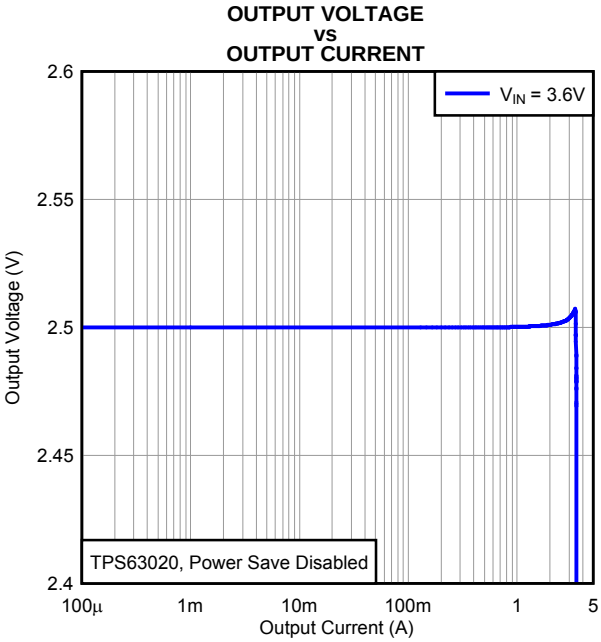


Figure 13.

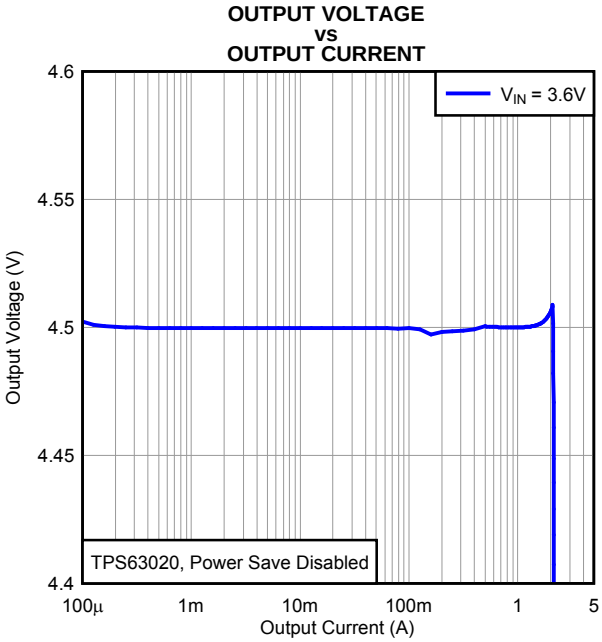


Figure 14.

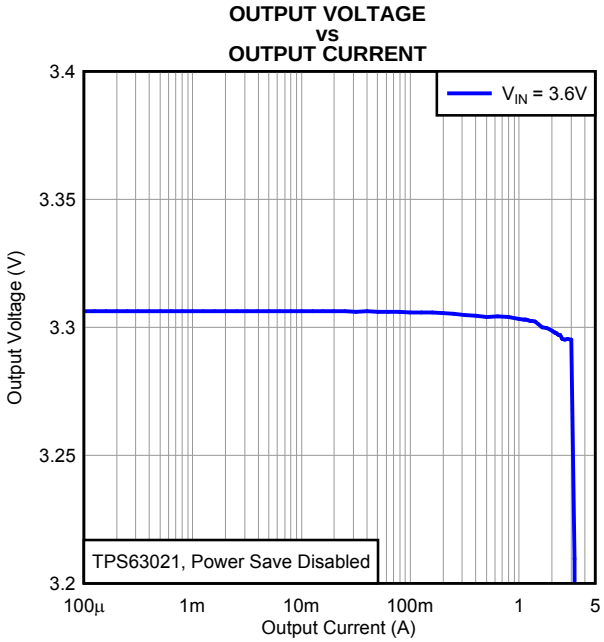


Figure 15.

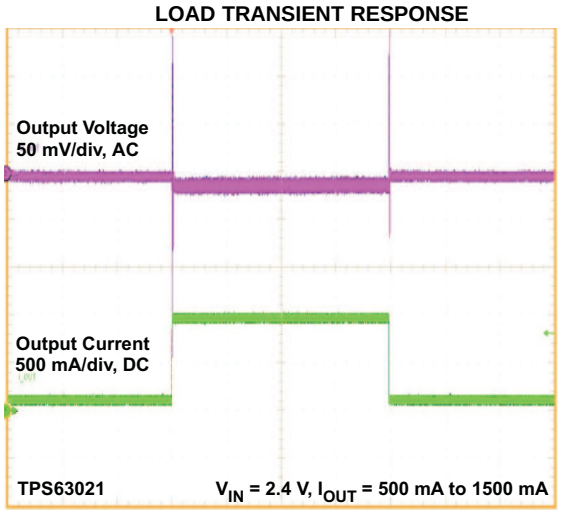


Figure 16.

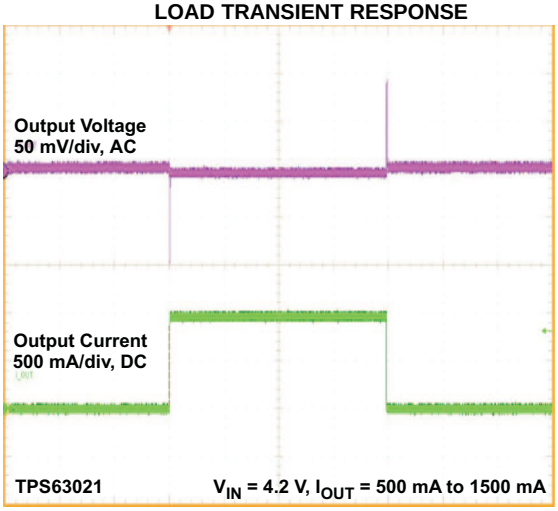


Figure 17.

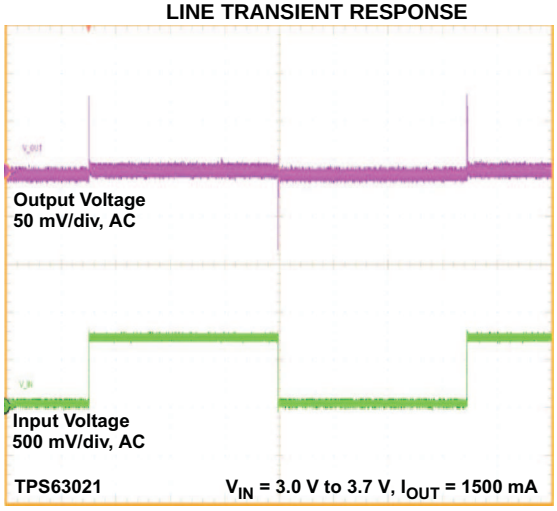
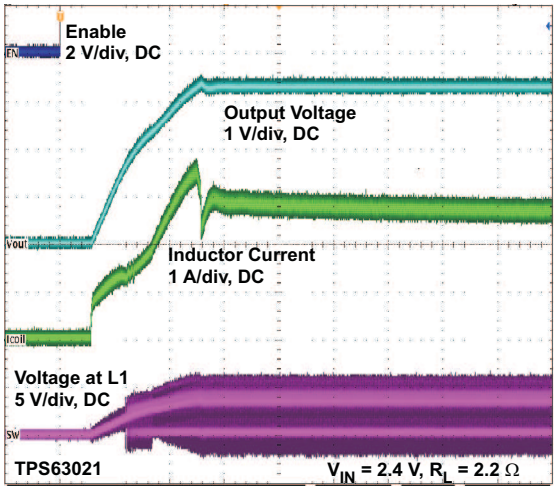


Figure 18.

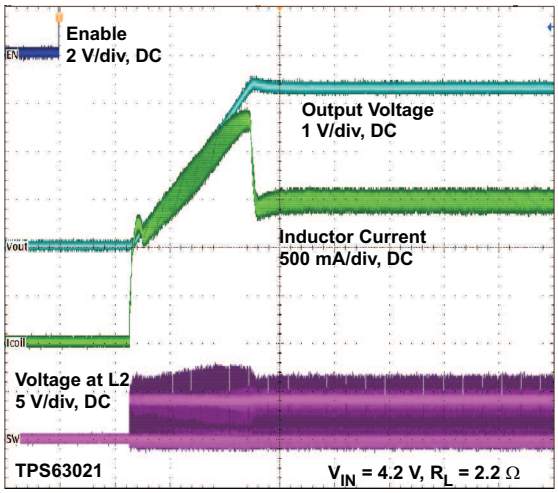
STARTUP AFTER ENABLE



Time 100 µs/div

Figure 19.

STARTUP AFTER ENABLE



Time 40 µs/div

Figure 20.

PARAMETER MEASUREMENT INFORMATION

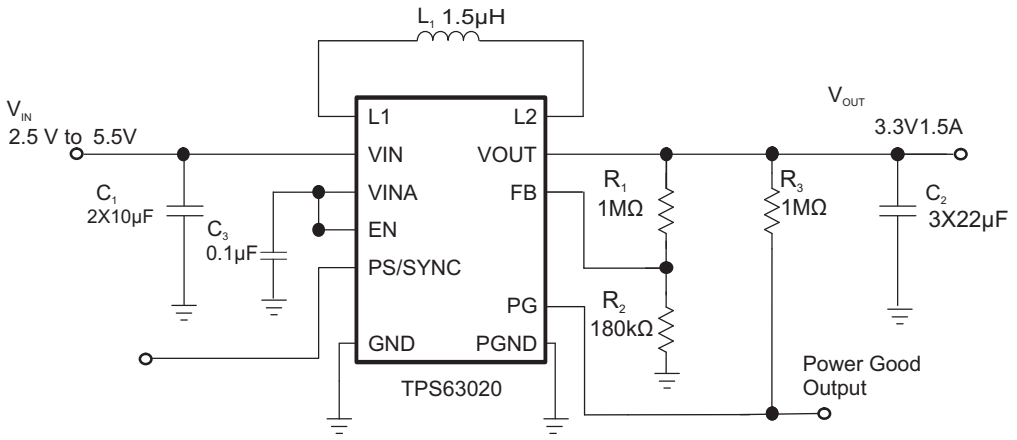


Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63020 or TPS63021	Texas Instruments
L1	1.5 µH, 4 mm x 4 mm x 2 mm	XFL4020-152ML, Coilcraft
C1	2 × 10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C2	3 × 22 µF 6.3V, 0603, X5R ceramic	GRM188R60J226MEAOL Murata
C3	0.1 µF, X5R or X7R ceramic	
R1	Depending on the output voltage at TPS63020, 0 Ω at TPS63021	
R2	Depending on the output voltage at TPS63020, not used at TPS63021	
R3	1 MΩ	

DETAILED DESCRIPTION

The controller circuit of the device is based on an average current mode topology. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages, a resistive voltage divider must be connected to that pin. At fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally, close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter. To protect the device from overheating an internal temperature sensor is implemented.

Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from step down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. For the remaining 2 switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

Control loop description

The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 21 shows the control loop.

The non inverting input of the transconductance amplifier Gmv can be assumed to be constant. The output of Gmv defines the average inductor current. The current through resistor RS, which represents the actual inductor current, is compared to the desired value and the difference, or current error, is amplified and compared to the sawtooth ramp of either the Buck or the Boost.

The Buck-Boost Overlap Control™ makes sure that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Thanks to this block whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other, on the other hand when there is no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result the number of classical buck-boost cycles or no switching is reduced to a minimum and high efficiency values has been achieved.

Slope compensation is not required to avoid subharmonic oscillation which are otherwise observed when working with peak current mode control with D>0.5.

Nevertheless the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This purpose is reached limiting the gain of the current amplifier.

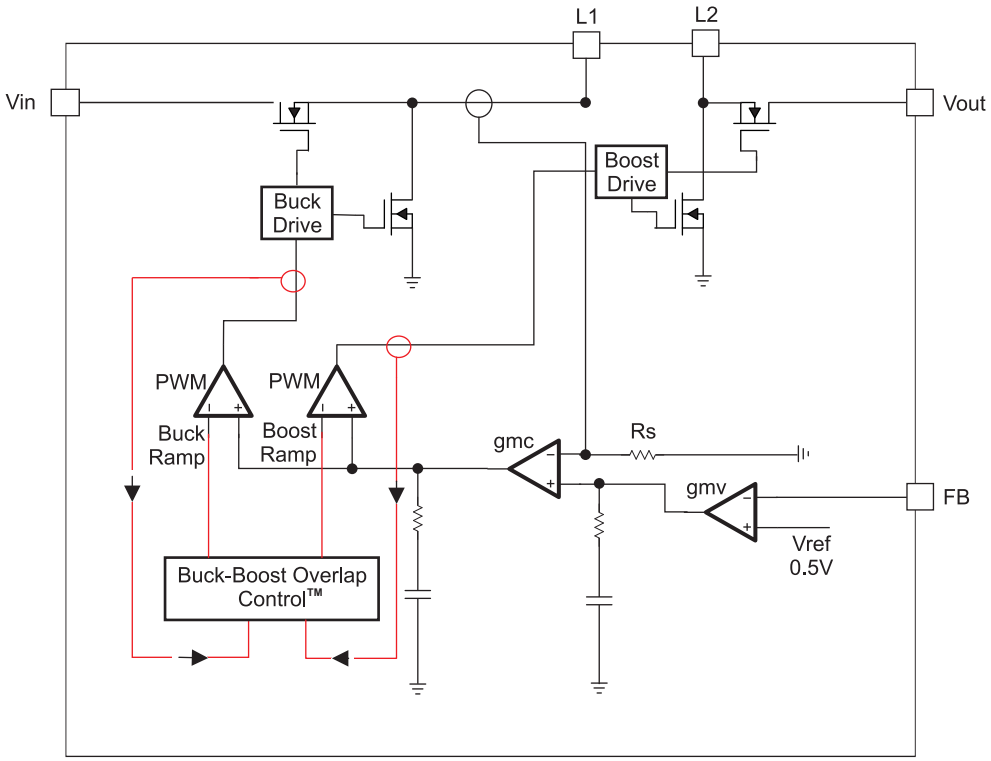


Figure 21. Average Current Mode Control

Power Save Mode and synchronization

The PS/SYNC pin can be used to select different operation modes. Power Save Mode is used to improve efficiency at light load. To enable power-save, PS/SYNC must be set low. If PS/SYNC is set low then Power Save Mode is entered when the average inductor current gets lower then about 100mA. At this point the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

During the Power Save Mode, the output voltage is monitored with a comparator by the threshold comp low and comp high. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comp low threshold set to 2.5% typical above Vout, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last one or several pulses. The converter continues these pulses until the comp high threshold, set to typically 3.5% above Vout nominal, is reached and the average inductance current gets lower than about 100mA. When the load increases above the minimum forced inductor current of about 100mA, the device will automatically switch to PWM mode.

The Power Save Mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a PLL, so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

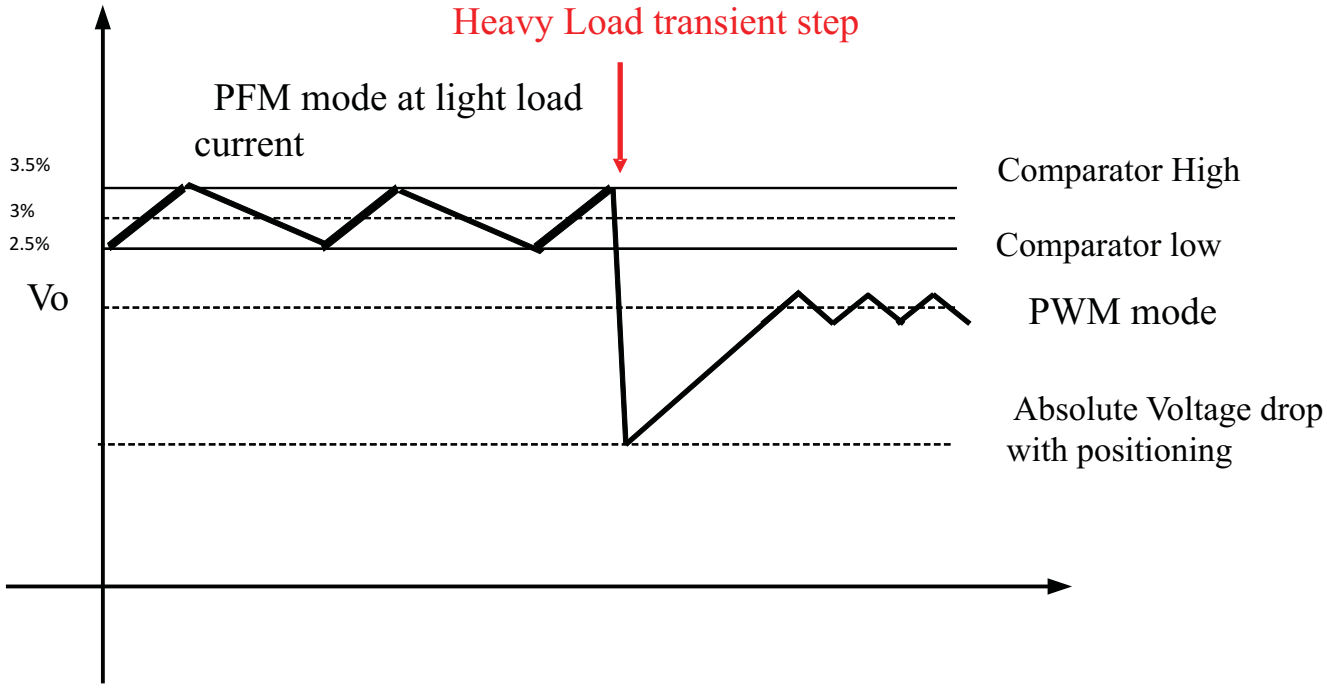


Figure 22. Power-Save Mode Thresholds and Dynamic Voltage Positioning

Dynamic voltage positioning

As detailed in Figure 22, the output voltage is typically 3% above the nominal output voltage at light load currents, as the device is in Power Save Mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. This allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transient changes. See Figure 22 for detailed operation of the power save mode

Dynamic Current Limit

To protect the device and the application, the average inductor current is limited internally on the IC. At nominal operating conditions, this current limit is constant. The current limit value can be found in the electrical characteristics table. If the supply voltage at VIN drops below 2.3V, the current limit is reduced. This can happen when the input power source becomes weak. Increasing output impedance, when the batteries are almost discharged, or an additional heavy pulse load is connected to the battery can cause the VIN voltage to drop. The dynamic current limit has its lowest value when reaching the minimum recommended supply voltage at VIN. At this voltage, the device is forced into burst mode operation trying to stay active as long as possible even with a weak input power source.

If the die temperature increases above the recommended maximum temperature, the dynamic current limit becomes active. Similar to the behavior when the input voltage at VIN drops, the current limit is reduced with temperature increasing.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

Power Good

The device has a built in power good function to indicate whether the output voltage is regulated properly. As soon as the average inductor current gets limited to a value below the current the voltage regulator demands for maintaining the output voltage the power good output gets low impedance. The output is open drain, so its logic function can be adjusted to any voltage level the connected logic is using, by connecting a pull up resistor to the supply voltage of the logic. By monitoring the status of the current control loop, the power good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react.

Softstart and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial 400mA following the output voltage increasing. At an output voltage of about 1.2V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will not increase. There is no timer implemented. Thus, the output voltage overshoot at startup, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. At a short on the output during operation, the current limit also is decreased accordingly.

Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. In case it reaches the overvoltage threshold the voltage amplifier regulates the output voltage to this value.

Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VINA is lower than approximately its threshold (see electrical characteristics table). When in operation, the device automatically enters the shutdown mode if the voltage on VINA drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6302X series of buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected to work with the internal compensation. As a general rule of thumb, the product L×C should not move over a wide range when selecting a different output filter. However, when selecting the output filter a low limit for the inductor value exists to avoid subharmonic oscillation which could be caused by a far too fast ramp up of the amplified inductor current. For the TPS6302X series the minimum inductor value should be kept at 1uH.

In particular either 1uH or 1.5uH is recommended working at output current between 1.5A and 2A. If operating with lower load current is also possible to use 2.2uH.

Selecting a larger output capacitor value is less critical because the corner frequency moves to lower frequencies.

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, with the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation (1) and (5) show how to calculate the peak current I_{PEAK}. Only the equation which defines the switch current in boost mode is reported because this is providing the highest value of current and represents the critical current value for selecting the right inductor.

Duty Cycle Boost

$$D = \frac{Vout - Vin}{Vout} \quad (1)$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \quad (2)$$

With,

D =Duty Cycle in Boost mode
f = Converter switching frequency (typical 2.4 MHz)
L = Selected inductor value
η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
Note: The calculation must be done for the maximum input voltage which is possible to have in boost mode

Consideration must be given to the load transients and error conditions that can cause higher inductor currents. This must be taken into consideration when selecting an appropriate inductor. Please refer to Table 3 for typical inductors.

The size of the inductor can also affect the stability of the feedback loop. In particular the boost transfer function exhibits a right half-plane zero, whose frequency is inverse proportional to the inductor value and the load current. This means higher is the value of inductance and load current more possibilities has the right plane zero to be moved at lower frequency which could degrade the phase margin of the feedback loop. It is recommended to choose the inductor's value in order to have the frequency of the right half plane zero >400KHz. The frequency of the RHPZ can be calculated using equation (6)

$$f_{RHPZ} = \frac{(1 - D)^2 \times Vout}{2\pi \times Iout \times L} \quad (3)$$

With,

D =Duty Cycle in Boost mode
Note: The calculation must be done for the maximum input voltage which is possible to have in boost mode

Table 2. Inductor Selection

VENDOR	INDUCTOR SERIES
Coilcraft	XFL4020
Toko	FDV0530S

Capacitor selection

Input Capacitor

At least a 10µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

Output Capacitor

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC. The recommended typical output capacitor value is 30µF with a variance that depends on the specific application requirements.

There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

When choosing input and output capacitors, it needs to be kept in mind, that the value of capacitance experiences significant losses from their rated value depending on the operating temperature and the operating DC voltage. It's not uncommon for a small surface mount ceramic capacitor to lose 50% and more of it's rated capacitance. For this reason could be important to use a larger value of capacitance or a capacitor with higher voltage rating in order to ensure the required capacitance at the full operating voltage.

Bypass Capacitor

To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VINA and GND. Using a ceramic capacitor with a value of 0.1µF is recommended. The value of this capacitor should not be higher than 0.22µF.

Setting the Output Voltage

When the adjustable output voltage version TPS63020 is used, the output voltage is set by the external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. The maximum recommended value for the output voltage is 8V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 500kΩ, in order to set the divider current at 1µA or higher. It is recommended to keep the value for this resistor in the range of 200kΩ. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (4)$$

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

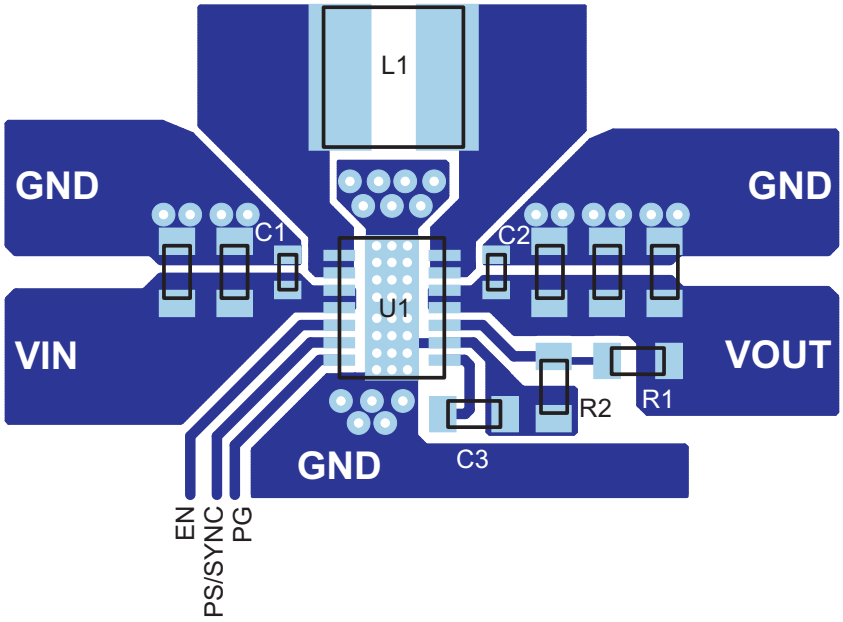


Figure 23. PCB Layout Suggestion

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: *Thermal Characteristics Application Note* (SZZA017), and *IC Package Thermal Metrics Application Note* (SPRA953).

TYPICAL APPLICATION

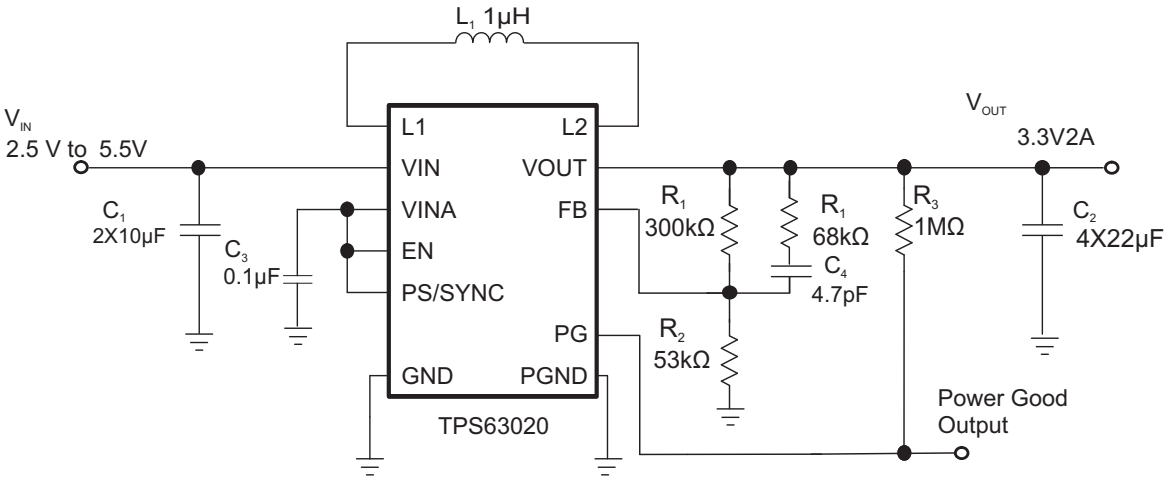


Figure 24. Application Circuit 2A Load Current

Capacitor C4 and resistor R1 are added for improved load transient performance.

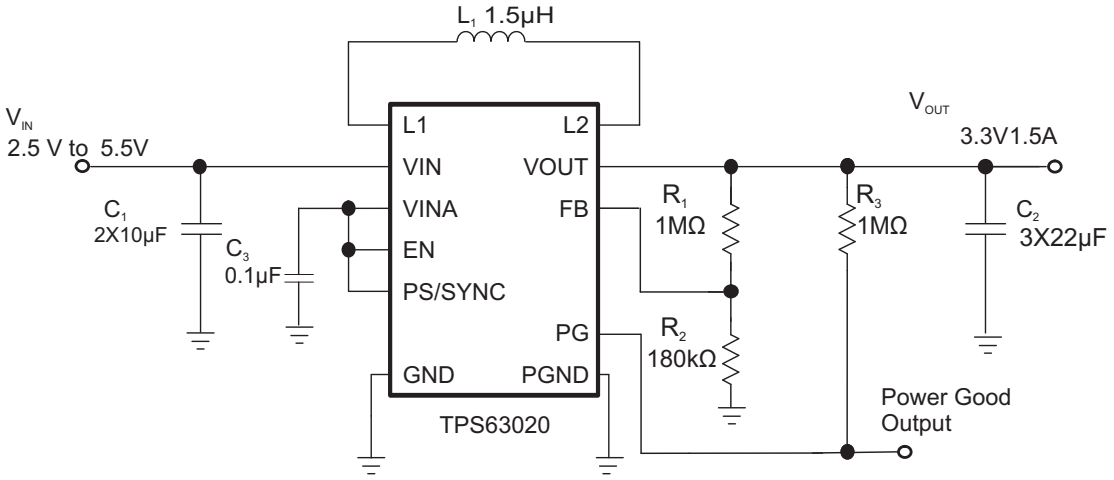


Figure 25. Application Circuit 1.5A Load Current

REVISION HISTORY

Changes from Original (April 2010) to Revision A **Page**

- Changed the List Of Components table. C1 and C2 orderable number From: GRM188R60J106KME84D To: GRM188R60J106ME84D 12
- Updated Figure 23 - PCB Layout Suggestion 19

Changes from Revision A (December 2011) to Revision B **Page**

Changes from Revision B (August 2012) to Revision C **Page**

- Changed front-page circuit to show correct values 1
- Changed Typical Application circuits to show correct component values. 20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS63020DSJR	ACTIVE	VSON	DSJ	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63020	Samples
TPS63020DSJT	ACTIVE	VSON	DSJ	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63020	Samples
TPS63021DSJR	ACTIVE	VSON	DSJ	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63021	Samples
TPS63021DSJT	ACTIVE	VSON	DSJ	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS63021	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

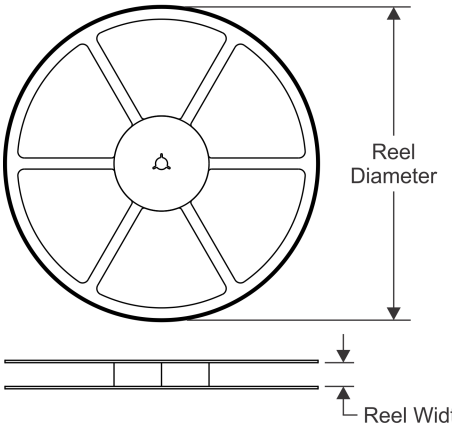
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

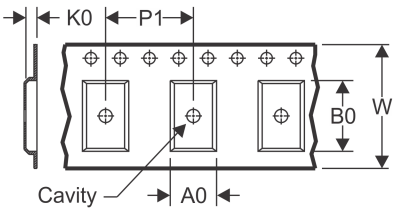
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

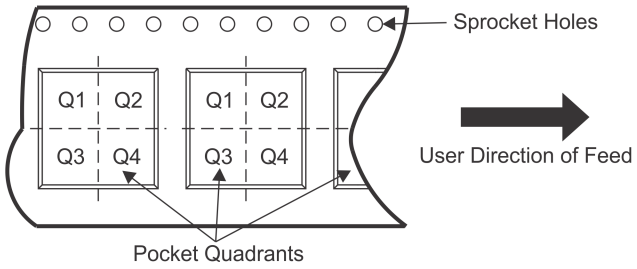


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

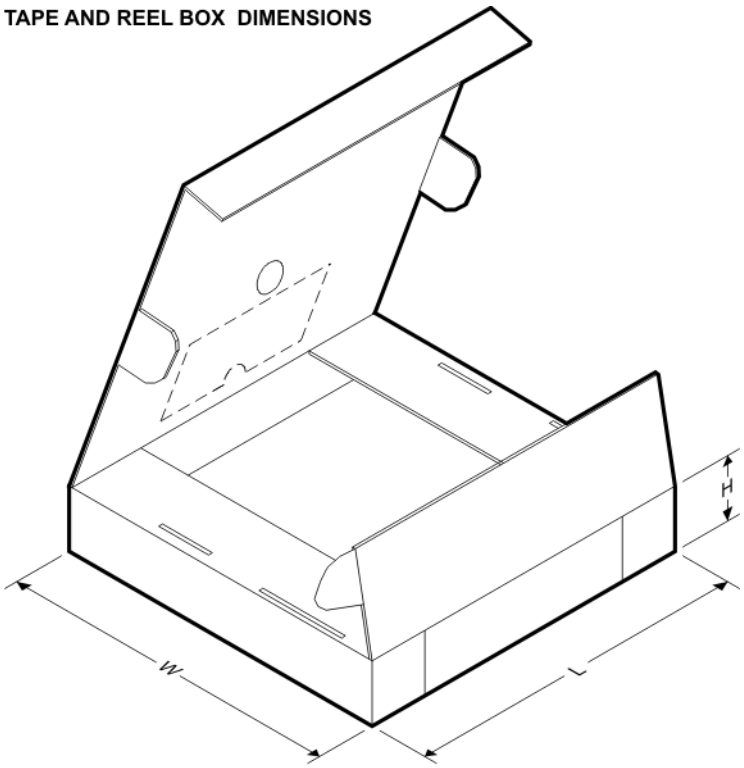
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63020DSJR	VSON	DSJ	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS63020DSJT	VSON	DSJ	14	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS63021DSJR	VSON	DSJ	14	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
TPS63021DSJT	VSON	DSJ	14	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

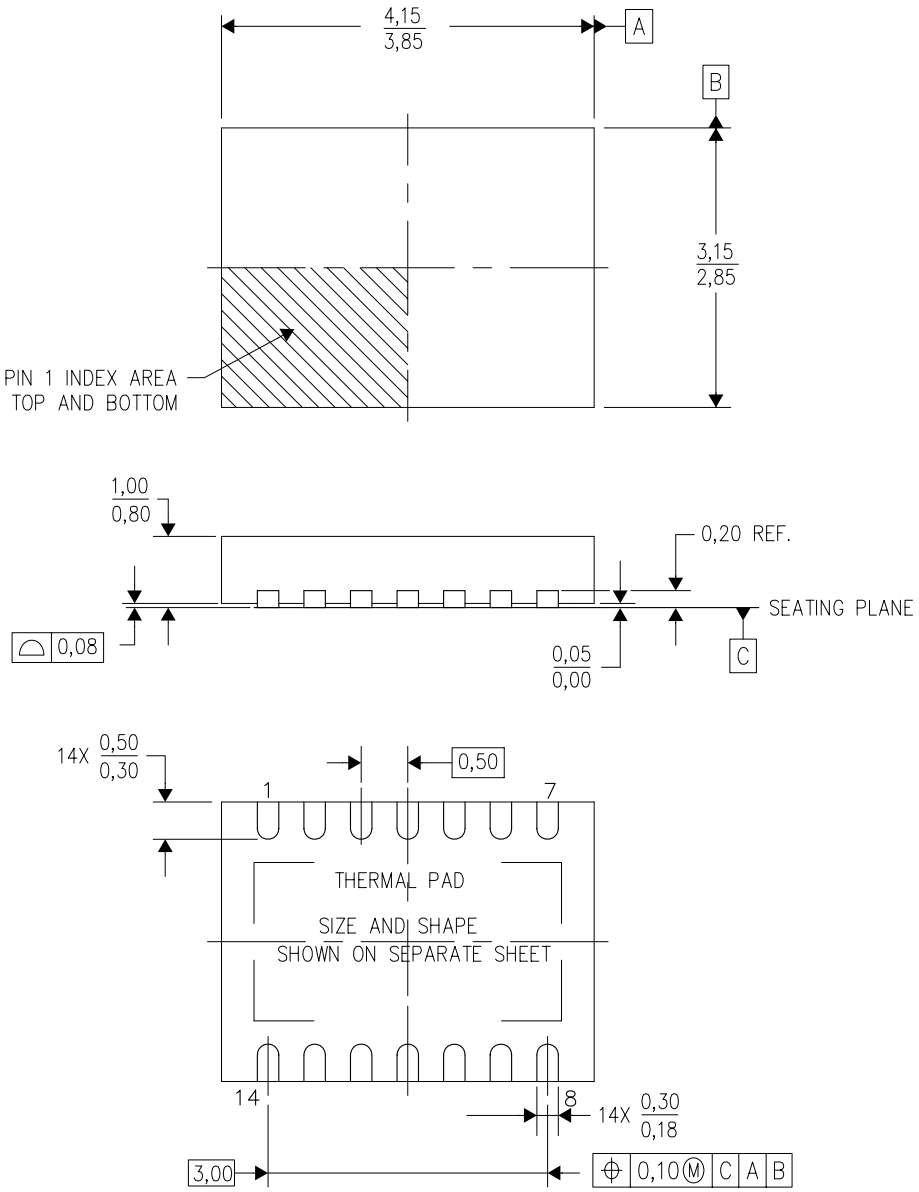
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63020DSJR	VSON	DSJ	14	3000	367.0	367.0	35.0
TPS63020DSJT	VSON	DSJ	14	250	210.0	185.0	35.0
TPS63021DSJR	VSON	DSJ	14	3000	367.0	367.0	35.0
TPS63021DSJT	VSON	DSJ	14	250	210.0	185.0	35.0

DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

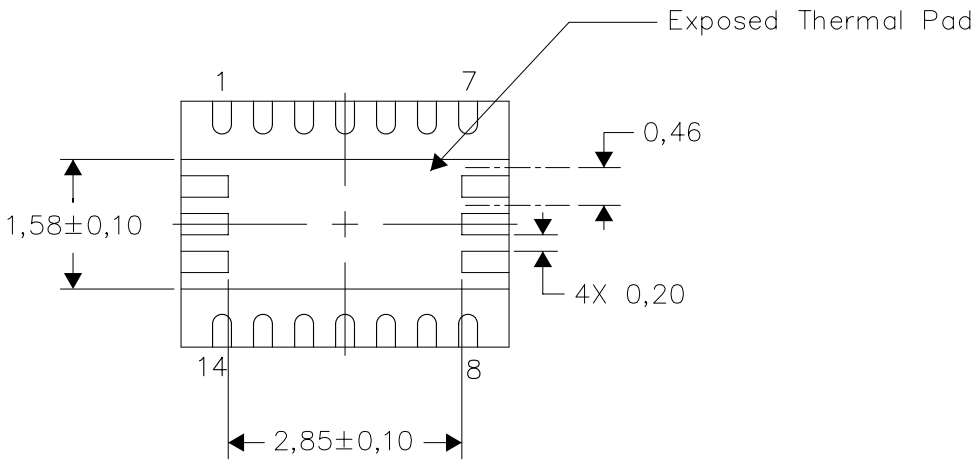
DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



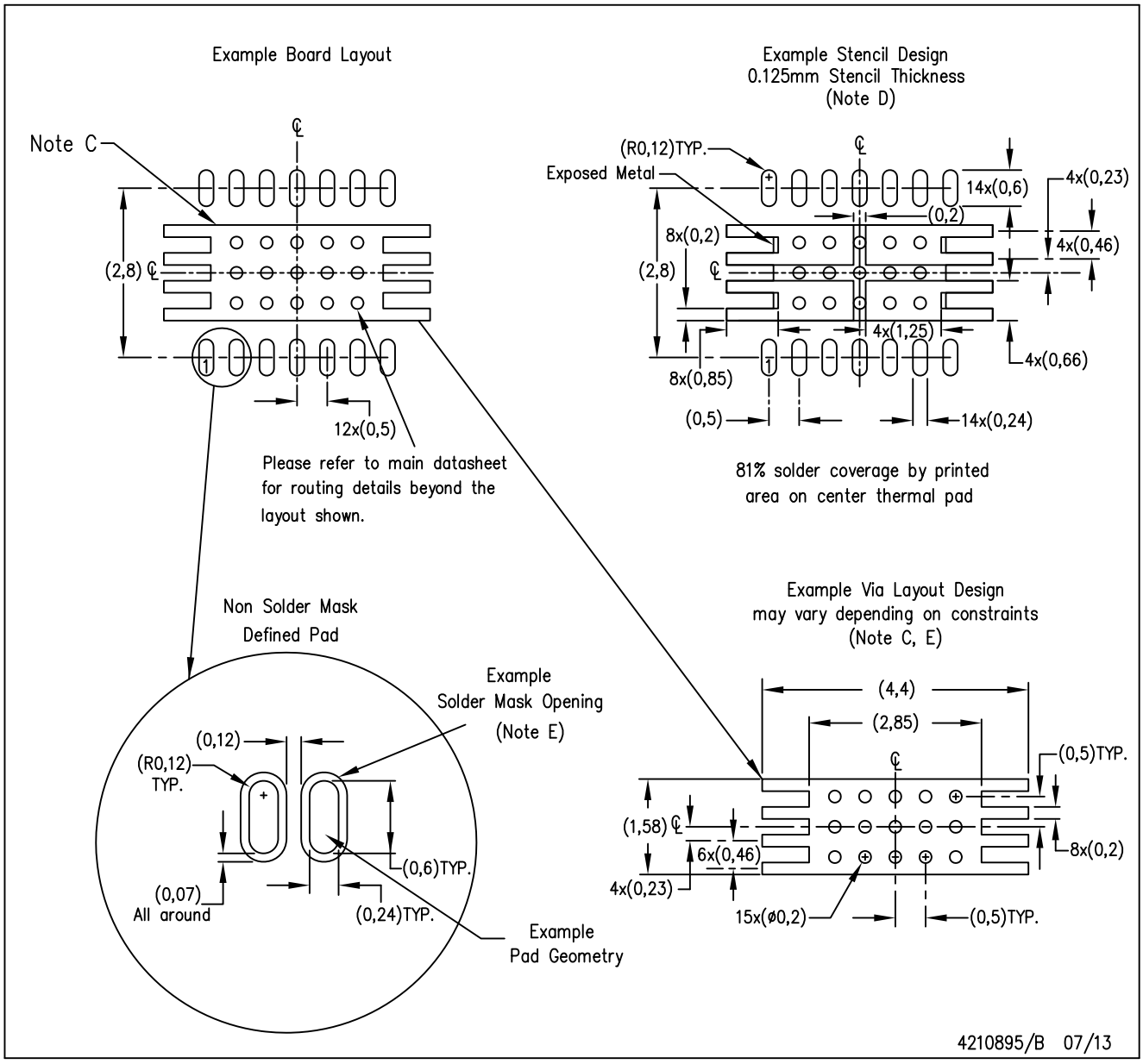
Bottom View

Exposed Thermal Pad Dimensions

4208549–3/E 05/11

NOTE: All linear dimensions are in millimeters

DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265