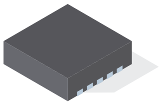


Actual Size
3 mm x 3 mm

18.5 V PFM/PWM STEP-UP DC-DC CONVERTER WITH 2.0 A SWITCH

FEATURES

- 2.3 V to 6.0 V Input Voltage Range
- 18.5 V Boost Converter With 2.0 A Switch Current
- 1.2 MHz Switching Frequency
- Power Save Mode for improved Efficiency at Low Output Power or Forced PWM
- Adjustable Soft-Start
- Thermal Shutdown
- Undervoltage Lockout
- 10-Pin QFN Package

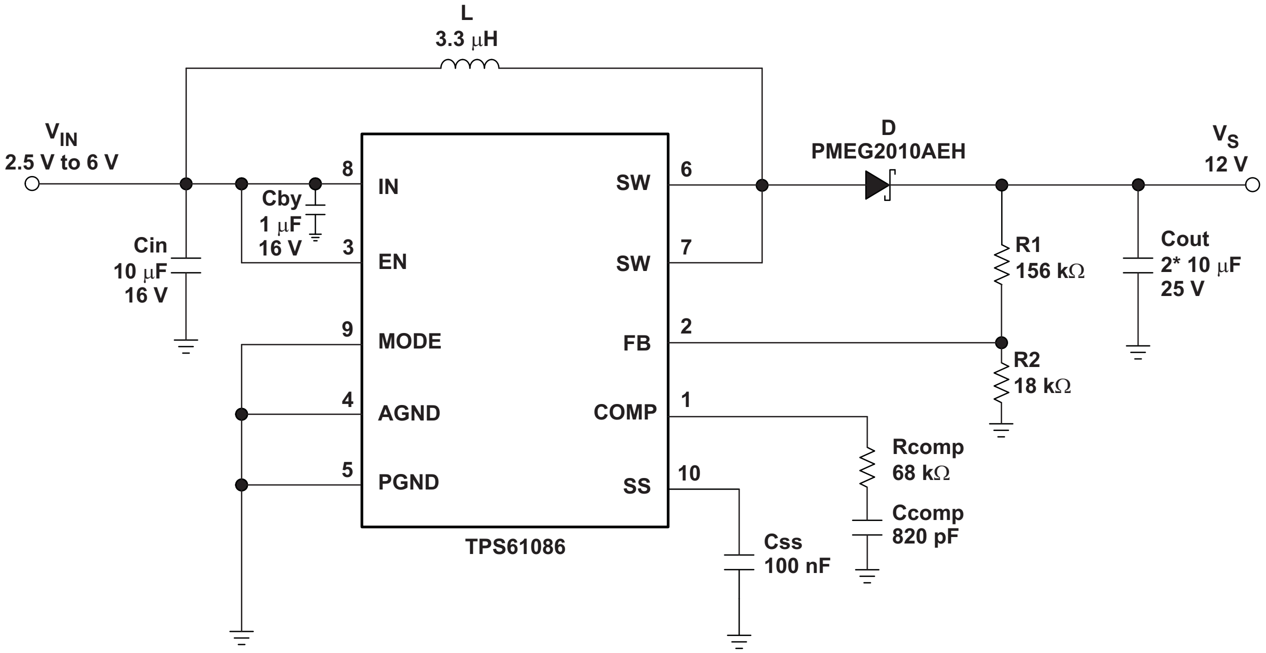
APPLICATIONS

- Handheld Devices
- GPS Receiver
- Digital Still Camera
- Portable Applications
- DSL Modem
- PCMCIA Card
- TFT LCD Bias Supply

DESCRIPTION

The TPS61086 is a high frequency, high efficiency DC to DC converter with an integrated 2.0 A, 0.13 Ω power switch capable of providing an output voltage up to 18.5 V. The implemented boost converter is based on a fixed frequency of 1.2MHz, pulse-width-modulation (PWM) controller that allows the use of small external inductors and capacitors and provides fast transient response.

At light load, the device can operate in Power Save Mode with pulse-frequency-modulation (PFM) to improve the efficiency while keeping a low output voltage ripple. For very noise sensitive applications, the device can be forced to PWM Mode operation over the entire load range by pulling the MODE pin high. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at startup.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)(2)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40 to 85°C	TPS61086DRC	QFN-10 (DRC)	PSRI

(1) The DRC package is available taped and reeled.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE	UNIT
Input voltage range IN(2)	–0.3 to 7.0	V
Voltage range on pins EN, FB, SS, FREQ, COMP	–0.3 to 7.0	V
Voltage on pin SW	–0.3 to 20	V
ESD rating HBM	2	kV
ESD rating MM	200	V
ESD rating CDM	500	V
Continuous power dissipation	See Dissipation Rating Table	
Operating junction temperature range	–40 to 150	°C
Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS(1)(2)

PACKAGE	$R_{\theta JA}$	$T_A \leq 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
QFN	40°C/W	3.3 W	1.8 W	1.3 W

(1) $P_D = (T_J – T_A)/R_{\theta JA}$.
(2) The exposed thermal die is soldered to the PCB using thermal vias. For more information, please refer to the Texas Instruments Application report SLMA002 regarding thermal characteristics of the PowerPAD package.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.3		6.0	V
V_S	Boost output voltage range	V_{IN} + 0.5		18.5	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

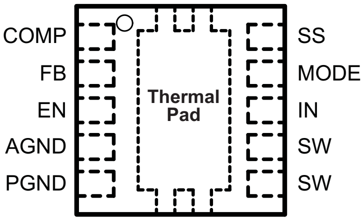
ELECTRICAL CHARACTERISTICS

V_{IN} = 3.3 V, EN = IN, V_S = 12 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.3		6.0	V
I_Q	Operating quiescent current into IN	Device not switching, V_{FB} = 1.3 V		75	100	µA
I_{SDVIN}	Shutdown current into IN	EN = GND			1	µA
V_{UVLO}	Under-voltage lockout threshold	V_{IN} falling			2.2	V
		V_{IN} rising			2.3	V
T_{SD}	Thermal shutdown	Temperature rising		150		°C
T_{SDHYS}	Thermal shutdown hysteresis			14		°C
LOGIC SIGNALS EN, FREQ						
V_{IH}	High level input voltage	V_{IN} = 2.3 V to 6.0 V	2			V
V_{IL}	Low level input voltage	V_{IN} = 2.3 V to 6.0 V			0.5	V
I_{INLEAK}	Input leakage current	EN = GND			0.1	µA
BOOST CONVERTER						
V_S	Boost output voltage		V_{IN} + 0.5		18.5	V
V_{FB}	Feedback regulation voltage		1.230	1.238	1.246	V
gm	Transconductance error amplifier			107		µA/V
I_{FB}	Feedback input bias current	V_{FB} = 1.238 V			0.1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 5 V, I_{SW} = current limit		0.13	0.20	Ω
		V_{IN} = V_{GS} = 3.3 V, I_{SW} = current limit		0.16	0.23	
I_{SWLEAK}	SW leakage current	EN = GND, V_{SW} = 6.0V			10	µA
I_{LIM}	N-Channel MOSFET current limit		2.0	2.6	3.2	A
I_{SS}	Soft-start current	V_{SS} = 1.238 V	7	10	13	µA
f_S	Oscillator frequency		0.9	1.2	1.5	MHz
	Line regulation	V_{IN} = 2.3 V to 6.0 V, I_{OUT} = 10 mA		0.0002		%/V
	Load regulation	V_{IN} = 3.3 V, I_{OUT} = 1 mA to 400 mA		0.11		%/A

PIN ASSIGNMENT

DRC PACKAGE
(TOP VIEW)



10-PIN 3mm x 3mm x 1mm QFN

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Compensation pin
FB	2	I	Feedback pin
EN	3	I	Shutdown control input. Connect this pin to logic high level to enable the device
AGND	4, Thermal Pad		Analog ground
PGND	5		Power ground
SW	6, 7		Switch pin
IN	8		Input supply pin
MODE	9	I	Operating mode selection pin. MODE = 'high' for forced PWM operation. MODE = 'low' for PFM operation
SS	10		Soft-start control pin. Connect a capacitor to this pin if soft-start needed. Open = no soft-start

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
η	Efficiency vs Load current- PFM	V_{IN} = 3.3 V, V_S = 9 V, 12 V, 15 V	Figure 1
η	Efficiencyvs Load current - Forced PWM	V_{IN} = 3.3 V, V_S = 9 V, 12 V, 15 V	Figure 2
	PFM switching 1 - discontinuous conduction	V_{IN} = 3.3 V, V_S = 12 V, I_{out} = 50 mA	Figure 3
	PFM switching 1 - discontinuous conduction	V_{IN} = 3.3 V, V_S = 12 V, I_{out} = 50 mA	Figure 4
	PFM switching - discontinuous conduction	V_{IN} = 3.3 V, V_S = 12 V, I_{out} = 4 mA	Figure 5
	Forced PWM switching - discontinuous conduction	V_{IN} = 3.3 V, V_S = 12 V, I_{out} = 4 mA	Figure 6
	PFM / PWM switching - continuous conduction	V_{IN} = 3.3 V, V_S = 12 V, I_{out} = 300 mA	Figure 7
$I_{out(max)}$	Maximum output current		Figure 8
	Load transient response - PFM	V_{IN} = 3.3 V, V_S = 12 V, I_{out} = 50 mA...150 mA	Figure 9
	Load transient response - Forced PWM	V_{IN} = 3.3 V, V_S = 1 2V, I_{out} = 50 mA...150 mA	Figure 10
	Line transient response - PFM	V_{IN} = 2.3 V...6.0 V, V_S = 12 V, I_{out} = 0 mA	Figure 11
	Line transient response - Forced PWM	V_{IN} = 2.3 V...6.0 V, V_S = 12 V, I_{out} = 150 mA	Figure 12
f_S	Switching frequency - Forced PWM	vs Load current, V_{IN} = 3.3 V, V_S = 12 V	Figure 13
f_S	Switching frequency - Forced PWM	vs Supply voltage, V_S = 12 V, I_{out} = 200 mA	Figure 14
	Soft-start		Figure 15
	Supply current	vs Supply voltage,V_{IN} = 3.3 V, V_S = 12 V	Figure 16

The typical characteristics are measured with the inductor CDRH6D12 3.3 µH from Sumida and the rectifier diode SL22.

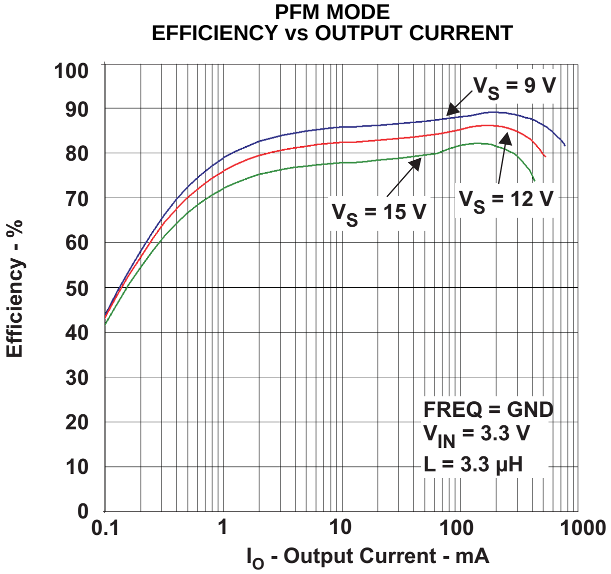

PFM MODE
EFFICIENCY vs OUTPUT CURRENT

Figure 1.

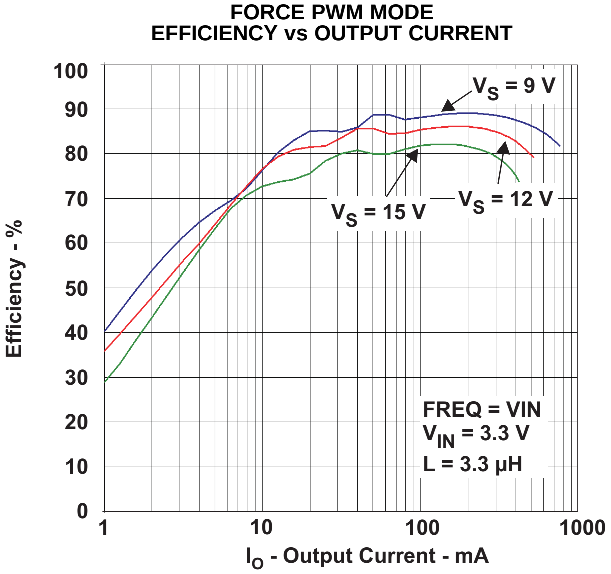

FORCE PWM MODE
EFFICIENCY vs OUTPUT CURRENT

Figure 2.

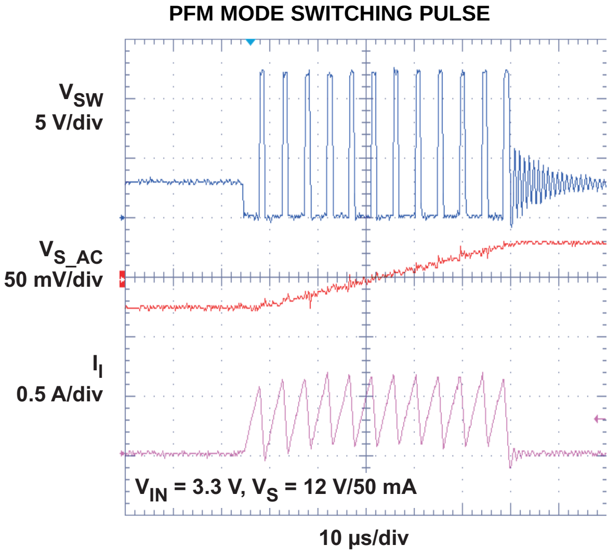

PFM MODE SWITCHING PULSE

Figure 3.

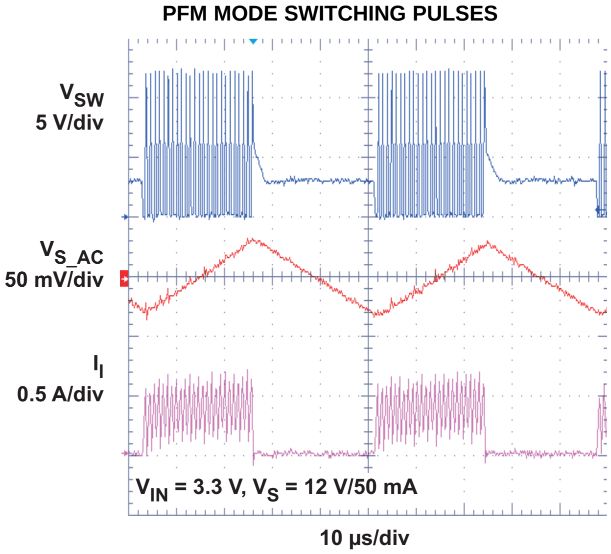

PFM MODE SWITCHING PULSES

Figure 4.

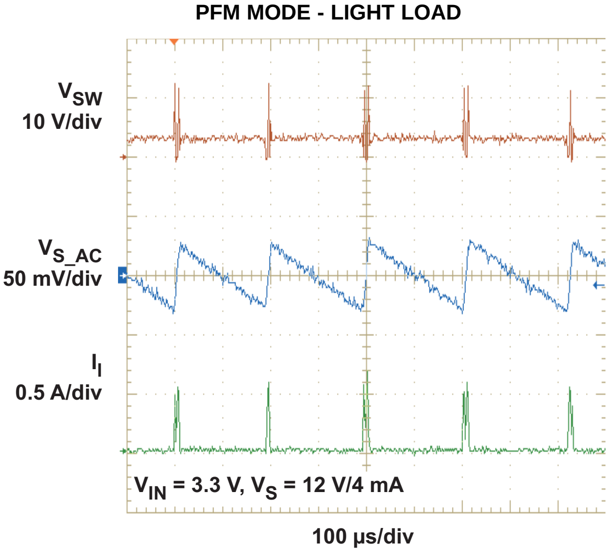


Figure 5.

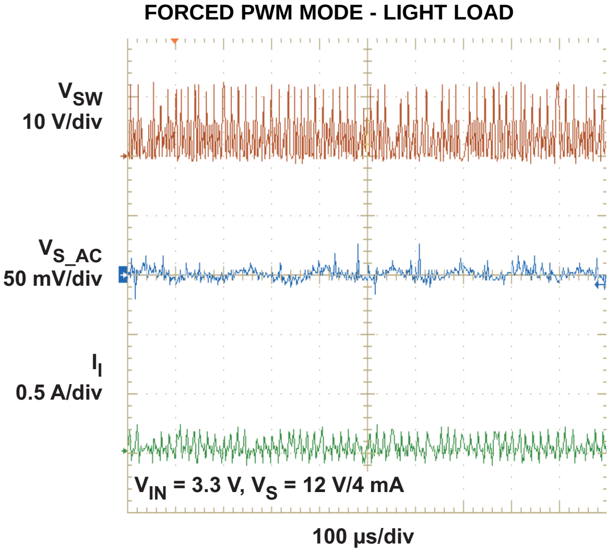


Figure 6.

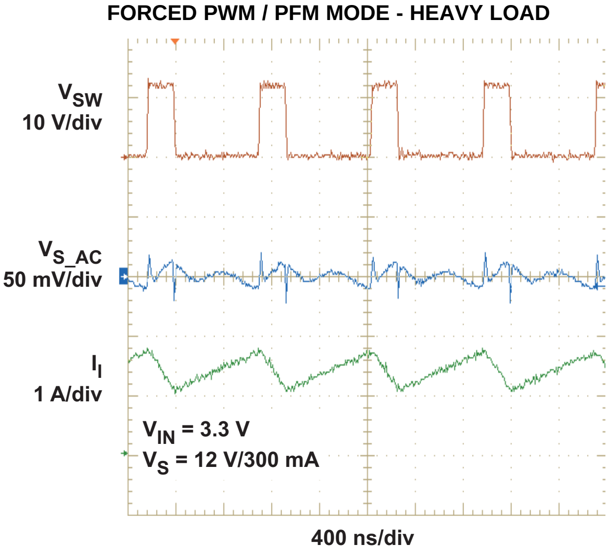


Figure 7.

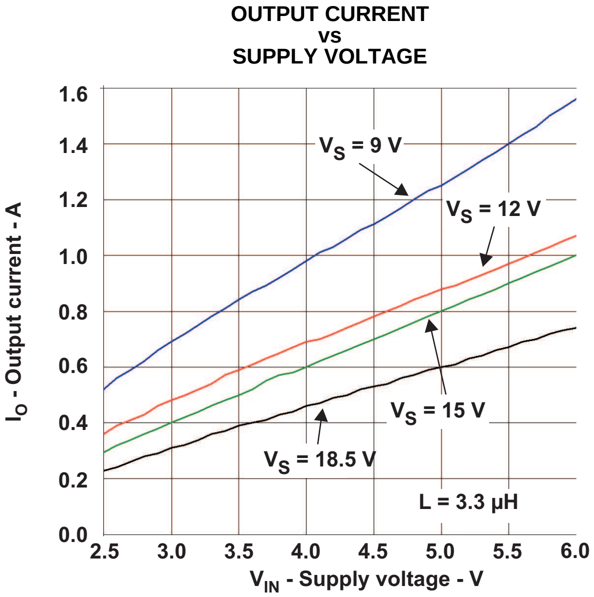
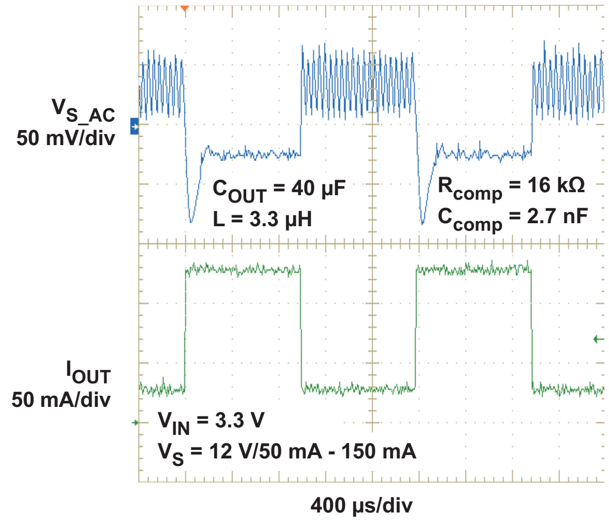
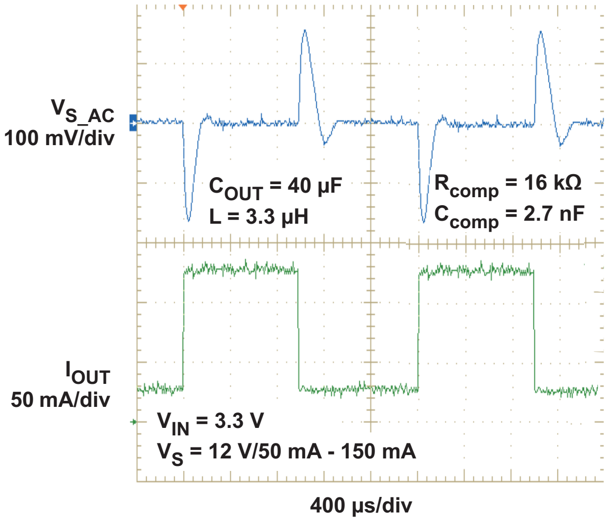


Figure 8.



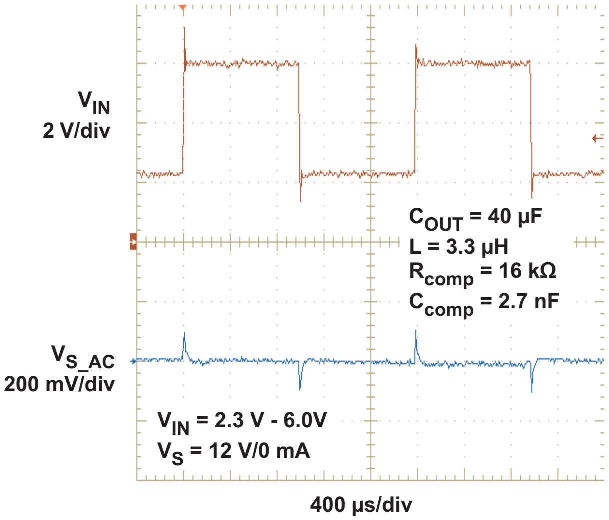
LOAD TRANSIENT RESPONSE
PFM MODE

Figure 9.



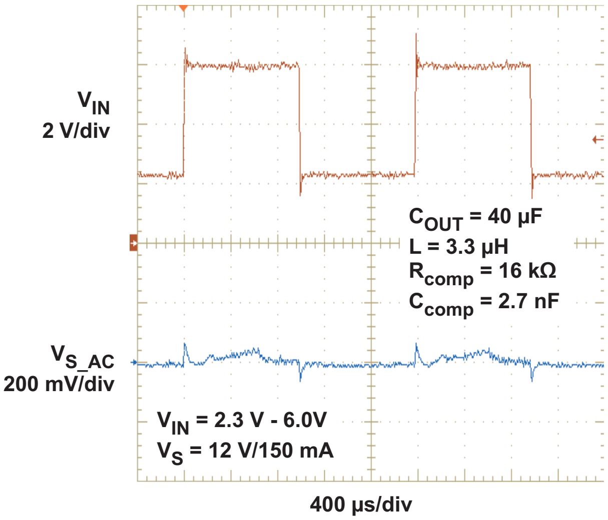
LOAD TRANSIENT RESPONSE
FORCE PWM MODE

Figure 10.



LINE TRANSIENT RESPONSE
LIGHT LOAD

Figure 11.



LINE TRANSIENT RESPONSE
HEAVY LOAD

Figure 12.

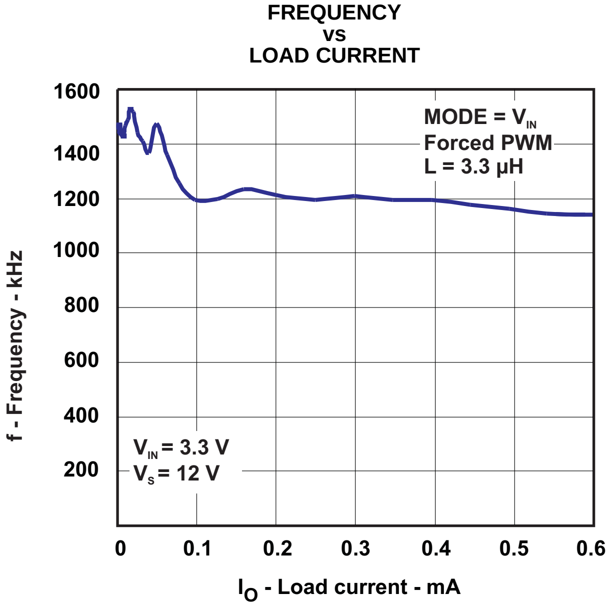


Figure 13.

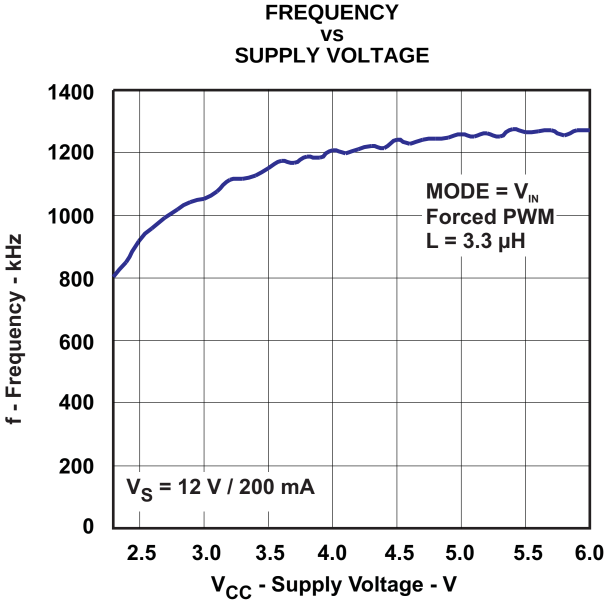


Figure 14.

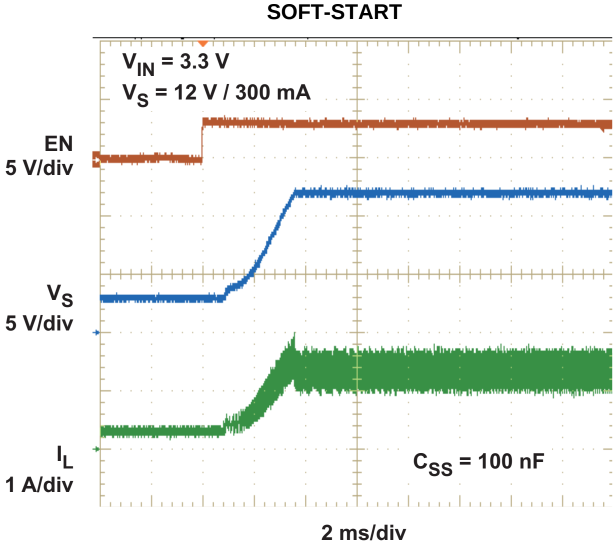


Figure 15.

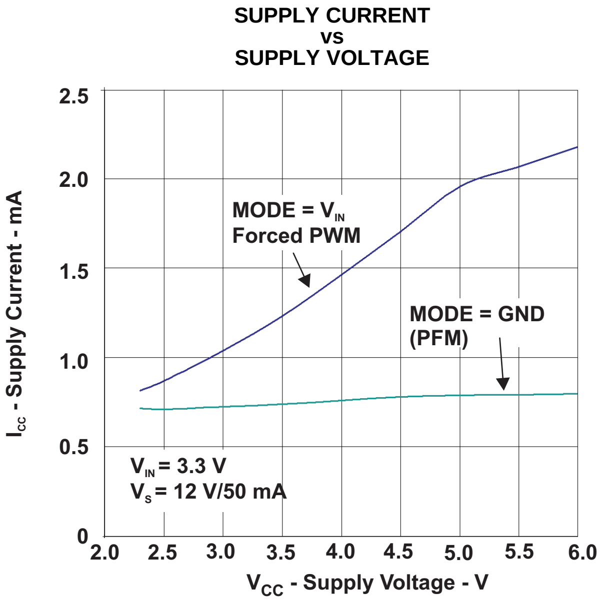


Figure 16.

DETAILED DESCRIPTION

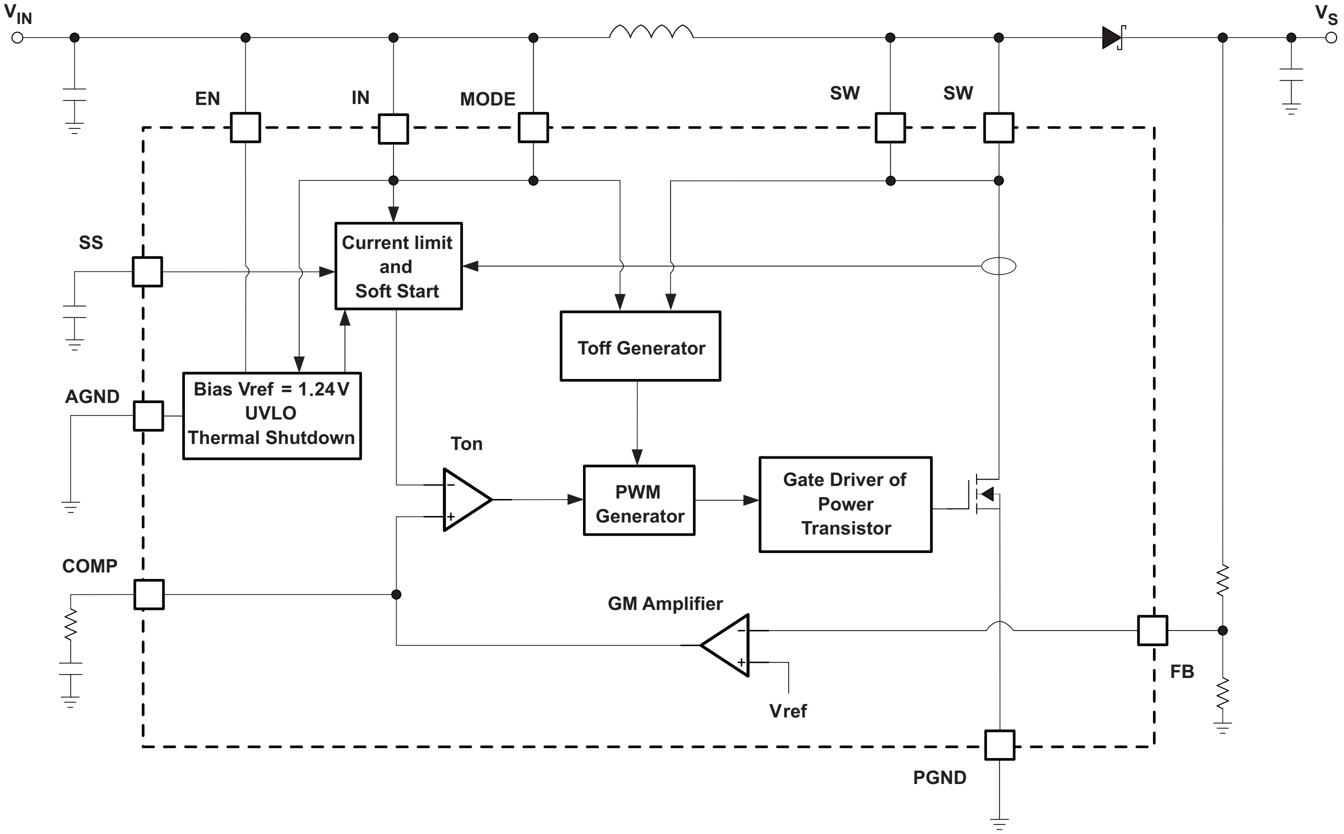


Figure 17. Block Diagram

The boost converter is designed for output voltages up to 18.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is fixed to 1.2 MHz and the minimum input voltage is 2.3 V. To limit the inrush current at start-up a soft-start pin is available.

TPS61086 boost converter's novel topology using adaptive off-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

Design Procedure

The first step in the design procedure is to verify that the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g. 90%.

1. Duty cycle, *D*:

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_S} \tag{1}$$

2. Maximum output current, $I_{out(max)}$:

$$I_{out(\max)} = \left(I_{LIM(\min)} - \frac{\Delta I_L}{2} \right) \cdot (1 - D) \tag{2}$$

3. Peak switch current in application, I_{swpeak}:

$$I_{swpeak} = \frac{\Delta I_L}{2} + \frac{I_{out}}{1 - D} \tag{3}$$

with the inductor peak-to-peak ripple current, ΔI_L

$$\Delta I_L = \frac{V_{IN} \cdot D}{f_S \cdot L} \tag{4}$$

and

V_{IN}	Minimum input voltage
V_S	Output voltage
$I_{LIM(min)}$	Converter switch current limit (minimum switch current limit = 2.0 A)
f_S	Converter switching frequency (typically 1.2 MHz)
L	Selected inductor value
η	Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation)

The peak switch current is the steady state peak switch current that the integrated switch, inductor and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

Soft-start

The boost converter has an adjustable soft-start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor, connected to the soft-start pin SS and charged with a constant current, is used to slowly ramp up the internal current limit of the boost converter. When the EN pin is pulled high, the soft-start capacitor C_{SS} is immediately charged to 0.3 V. The capacitor is then charged at a constant current of 10 μA typically until the output of the boost converter V_S has reached its Power Good threshold (90% of V_S nominal value). During this time, the SS voltage directly controls the peak inductor current, starting with 0 A at V_{SS} = 0.3 V up to the full current limit at $V_{SS} \approx$ 800 mV. The maximum load current is available after the soft-start is completed. The larger the capacitor the slower the ramp of the current limit and the longer the soft-start time. A 100 nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.

Inductor Selection

The TPS61086 is designed to work with a wide range of inductors. The main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the *Design Procedure* section with additional margin to cover for heavy load transients. An alternative, more conservative, is to choose an inductor with a saturation current at least as high as the maximum switch current limit of 3.2 A. The other important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS61086, inductor values between 3 µH and 6 µH are a good choice. Possible inductors are shown in Table 1.

Typically, it is recommended that the inductor current ripple is below 35% of the average inductor current. The following equation can therefore be used to calculate the inductor value, *L*:

$$L = \left(\frac{V_{IN}}{V_S}\right)^2 \cdot \left(\frac{V_S - V_{IN}}{I_{out} \cdot f_S}\right) \cdot \left(\frac{\eta}{0.35}\right) \tag{5}$$

with

V_{IN}	Minimum input voltage
V_S	Output voltage
I_{out}	Maximum output current in the application
f_S	Converter switching frequency (typically 1.2 MHz)
η	Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation)

Table 1. Inductor Selection

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (L×W×H mm)	DCR TYP (mΩ)	I_{sat} (A)
3.3	Sumida	CDH38D09	4 x 4 x 1	240	1.25
4.7	Sumida	CDPH36D13	5 x 5 x 1.5	155	1.36
3.3	Sumida	CDPH4D19F	5.2 x 5.2 x 2	33	1.5
3.3	Sumida	CDRH6D12	6.7 x 6.7 x 1.5	62	2.2
4.7	Würth Elektronik	7447785004	5.9 x 6.2 x 3.3	60	2.5
5	Coilcraft	MSS7341	7.3 x 7.3 x 4.1	24	2.9

Rectifier Diode Selection

To achieve high efficiency a Schottky type should be used for the rectifier diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. The averaged rectified forward current I_{avg}, the Schottky diode needs to be rated for, is equal to the output current I_{out}:

$$I_{avg} = I_{out} \tag{6}$$

Usually a Schottky diode with 1A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current I_{out} but has to be able to dissipate the power. The dissipated power, P_D, is the average rectified forward current times the diode forward voltage, $V_{forward}$.

$$P_D = I_{avg} \cdot V_{forward} \tag{7}$$

Typically the diode should be able to dissipate around 500mW depending on the load current and forward voltage.

Table 2. Rectifier Diode Selection

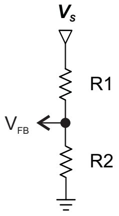
CURRENT RATING I_{avg}	V_r	$V_{forward}/I_{avg}$	SUPPLIER	COMPONENT CODE	PACKAGE TYPE
750 mA	20 V	0.425 V / 1 A	Fairchild Semiconductor	FYV0704S	SOT 23
1 A	20 V	0.39 V / 1 A	NXP	PMEG2010AEH	SOD 123
1 A	20 V	0.5 V / 1 A	Vishay Semiconductor	SS12	SMA
1 A	20 V	0.44 V / 1 A	Vishay Semiconductor	MSS1P2L	µ -SMP
2 A	20 V	0.44 V / 2 A	Vishay Semiconductor	SL22	SMB

Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 µA flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 18 kΩ is typically selected. The resistors are then calculated as:

$$R2 = \frac{V_{FB}}{70\mu A} \approx 18k\Omega \qquad R1 = R2 \cdot \left(\frac{V_s}{V_{FB}} - 1 \right)$$

$$V_{FB} = 1.238V$$



(8)

Compensation (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier.

Standard values of R_{COMP} = *16 k*Ω and C_{COMP} = *2.7 nF* will work for the majority of the applications.

Please refer to Table 3 for dedicated compensation networks giving an improved load transient response. The following equations can be used to calculate R_{COMP} and C_{COMP}:

$$R_{COMP} = \frac{110 \cdot V_{IN} \cdot V_s \cdot C_{out}}{L \cdot I_{out}} \qquad C_{COMP} = \frac{V_s \cdot C_{out}}{7.5 \cdot I_{out} \cdot R_{COMP}} \tag{9}$$

with

V_{IN}	Minimum input voltage
V_S	Output voltage
C_{out}	Output capacitance
L	Inductor value, e.g. 3.3 µH or 4.7 µH
I_{out}	Maximum output current in the application

Make sure that R_{COMP} < *120 k*Ω and C_{COMP}> *820 pF*, independent of the results of the above formulas.

Table 3. Recommended Compensation Network Values at High/Low Frequency

L	V_S	V_{IN} ± 20%	R_{COMP}	C_{COMP}
3.3 µH	15 V	5 V	100 kΩ	820 pF
		3.3 V	91 kΩ	1.2 nF
	12 V	5 V	68 kΩ	820 pF
		3.3 V	68 kΩ	1.2 nF
	9 V	5 V	39 kΩ	820 pF
		3.3 V	39 kΩ	1.2 nF

Table 3 gives conservative R_{COMP} and C_{COMP} values for certain inductors, input and output voltages providing a very stable system. For a faster response time, a higher R_{COMP} value can be used to enlarge the bandwidth, as well as a slightly lower value of C_{COMP} to keep enough phase margin. These adjustments should be performed in parallel with the load transient response monitoring of TPS61086.

Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS61086 has an analog input IN. Therefore, a 1 µF bypass is highly recommended as close as possible to the IC from IN to GND.

One 10 µF ceramic input capacitors are sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to Table 4 and typical applications for input capacitor recommendation

Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor like ceramic capcaitor is recommended. Two to four 10 µF ceramic output capacitors (or two 22 µF) work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to Table 4 for the selection of the output capacitor.

Table 4. Rectifier Input and Output Capacitor Selection

	CAPACITOR/SIZE	VOLTAGE RATING	SUPPLIER	COMPONENT CODE
C_{IN}	22 µF/1206	16 V	Taiyo Yuden	EMK316 BJ 226ML
IN bypass	1 µF/0603	16 V	Taiyo Yuden	EMK107 BJ 105KA
C_{OUT}	10 µF/1206	25 V	Taiyo Yuden	TMK316 BJ 106KL

To calculate the output voltage ripple, the following equation can be used:

$$\Delta V_C = \frac{V_S - V_{IN}}{V_S \cdot f_S} \cdot \frac{I_{out}}{C_{out}} \qquad \Delta V_{C\_ESR} = I_{L(peak)} \cdot R_{C\_ESR} \tag{10}$$

with

ΔV_C	Output voltage ripple dependent on output capacitance,output current and switching frequency
V_S	Output voltage
V_{IN}	Minimum input voltage of boost converter
f_S	Converter switching frequency (typically 1.2 MHz)
I_{out}	Output capacitance
ΔV_{C_ESR}	Output voltage ripple due to output capacitors ESR (equivalent series resistance)
I_{SWPEAK}	Inductor peak switch current in the application
R_{C_ESR}	Output capacitors equivalent series resistance (ESR)

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

Operating Mode (MODE)

Power Save Mode

Connecting the MODE pin to GND (or any low logic level) enables the Power Save Mode operation. The converter operates in quasi fixed frequency PWM (Pulse Width Modulation) mode at moderate to heavy load and in the PFM (Pulse Frequency Modulation) mode during light loads, which maintains high efficiency over a wide load current range.

In PFM mode the converter is skipping switch pulses. However, within a PFM pulse, the switching frequency is still fixed to 1.2 MHz typically and the duty cycle determined by the input and output voltage. Therefore, the inductor peak current will remain constant for a defined application. With an increasing output load current, the PFM pulses become closer and closer (the PFM mode frequency gets higher) until no pulse is skipped anymore: the device operates then in CCM (Continuous Conduction Mode) with normal PWM mode.

The PFM mode frequency (between each PFM pulse) depends on the load current, the external components like the inductor or the output capacitor values as well as the output voltage. The device enters Power Save Mode as the inductor peak current falls below a 0.6A typically and switches until V_S is 1% higher than its nominal value. The converter stops switching when $V_S = V_S + 0.5\%$. The output voltage will thenrefore oscillate between 0.5% and 1% more than its nominal value which will provide excellent transient response to sudden load change, since the output voltage drop will be reduced due to this slight positive offset (see Figure 9).

Forced PWM Mode

Pulling the MODE pin high forces the converter to operate in a continuous PWM mode evan at light load currents. The advantage is that the converter operates with a quai constant frequency that allows simple filtering of the swithcing frequency for noise-sensitive applications. In this mode and at light load, the efficiency is lower compared to the Power Save Mode.

For additional flexibility, it is possible to switch from Power Save Mode to Forced PWM Mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.2 V.

Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered the device stops switching until the junction temperature falls below typically 136°C. Then the device starts switching again.

Overvoltage Prevention

If overvoltage is detected on the FB pin (typically 3 % above the nominal value of 1.238 V) the part stops switching immediately until the voltage on this pin drops to its nominal value. This prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

APPLICATION INFORMATION

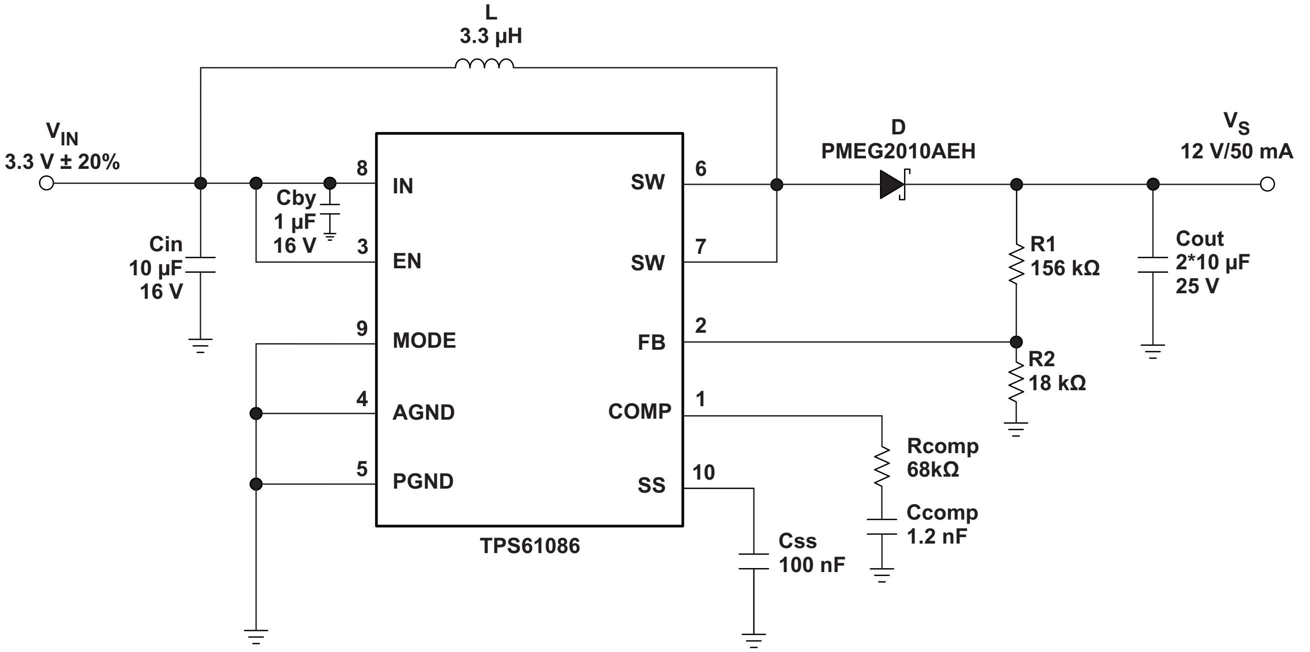


Figure 18. Typical Application, 3.3 V to 12 V (PFM MODE)

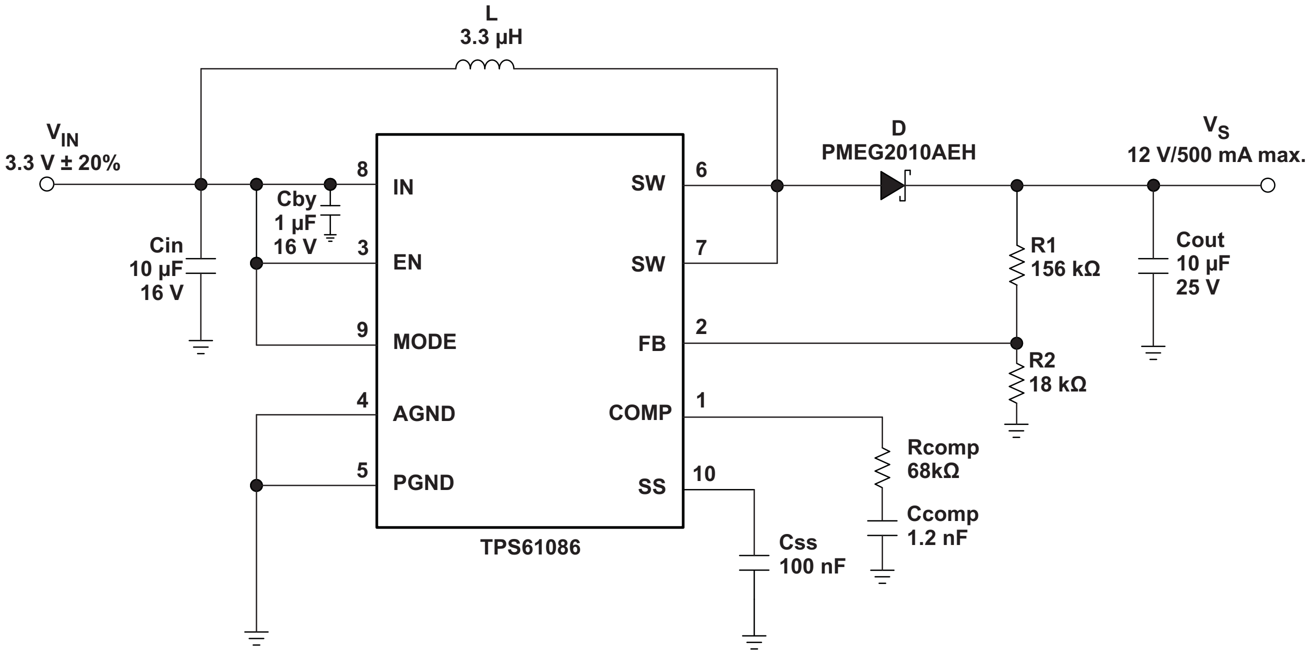


Figure 19. Typical Application, 3.3V to 12 V (FORCE PWM MODE)

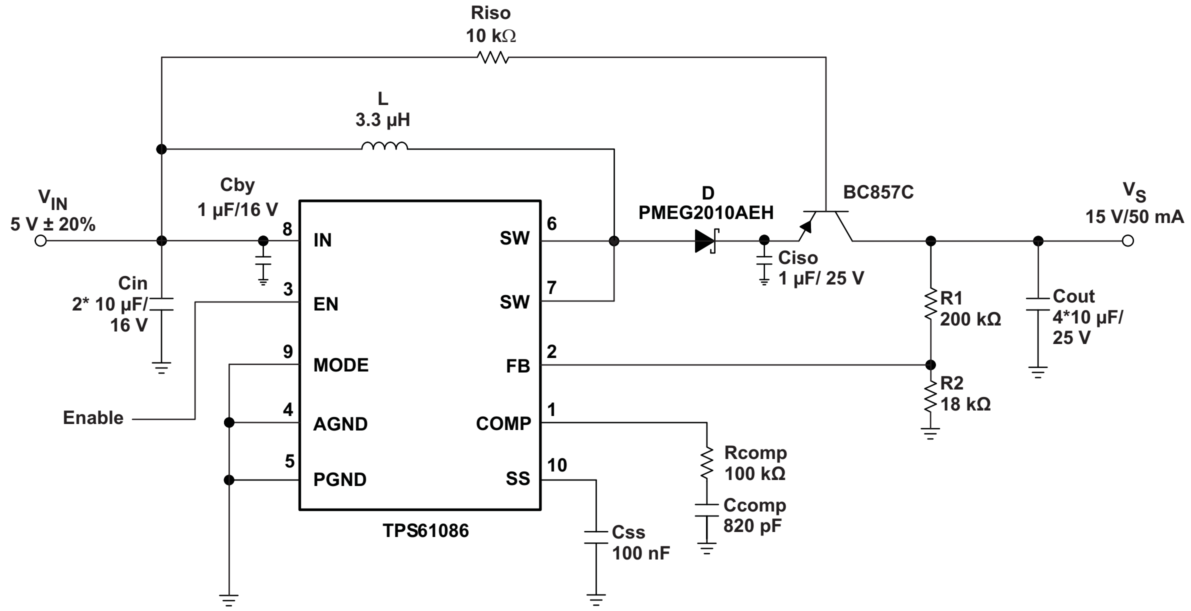


Figure 20. Typical Application with External Load Disconnect Switch

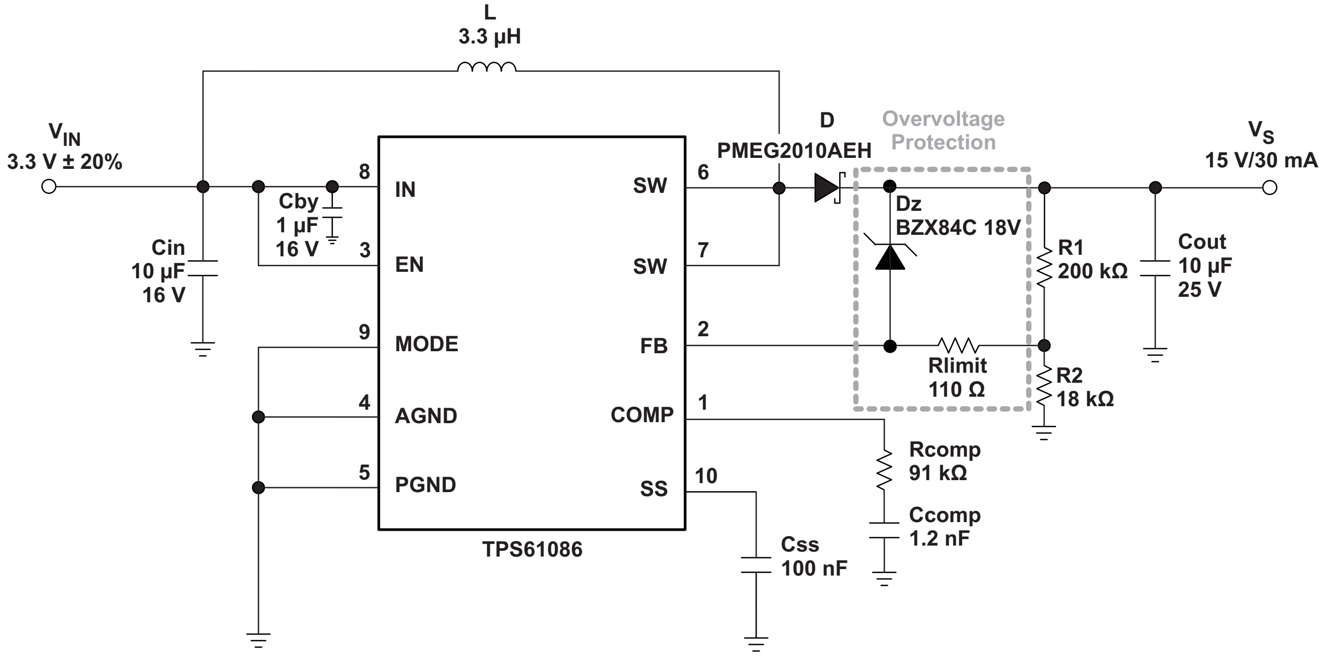


Figure 21. Typical Application, 3.3 V to 15 V (PFM MODE) with Overvoltage Protection

TFT LCD APPLICATION

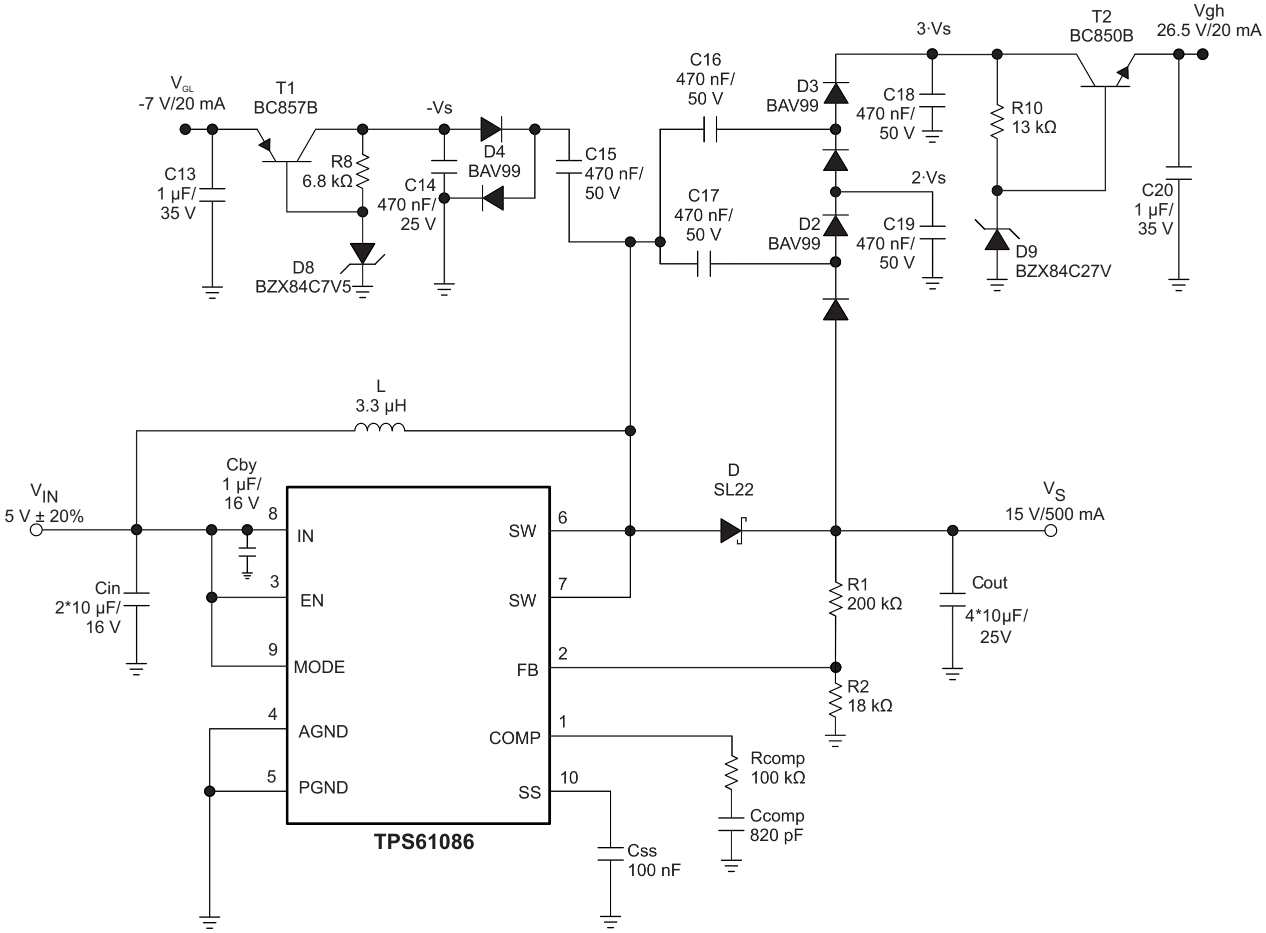


Figure 22. Typical Application 5 V to 15 V (FORCE PWM MODE) for TFT LCD with External Charge Pumps (VGH, VGL)

WHITE LED APPLICATIONS

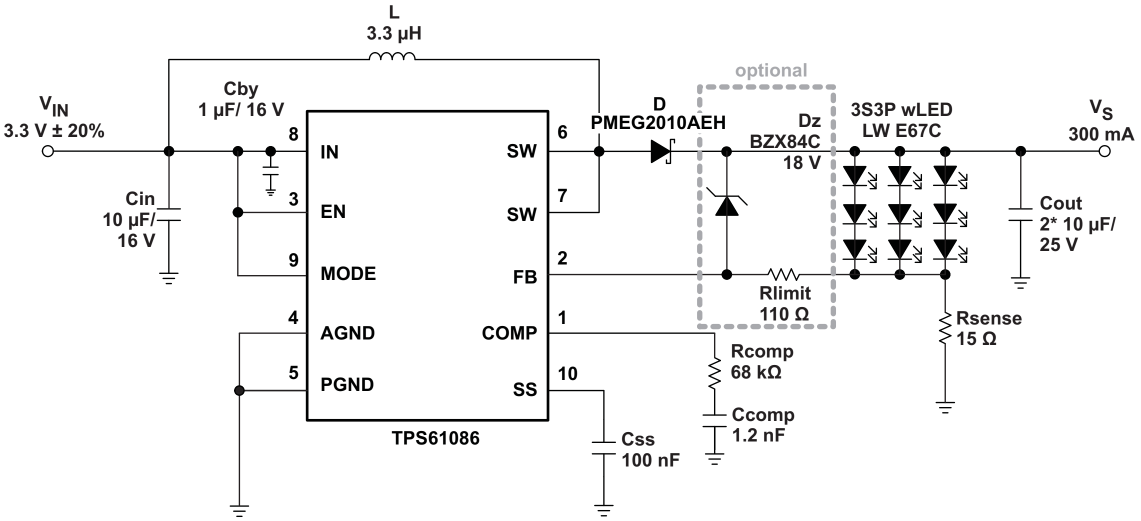


Figure 23. Simple Application (3.3 V input voltage - FORCED PWM MODE) for wLED Supply (3S3P) (with optional clamping Zener diode)

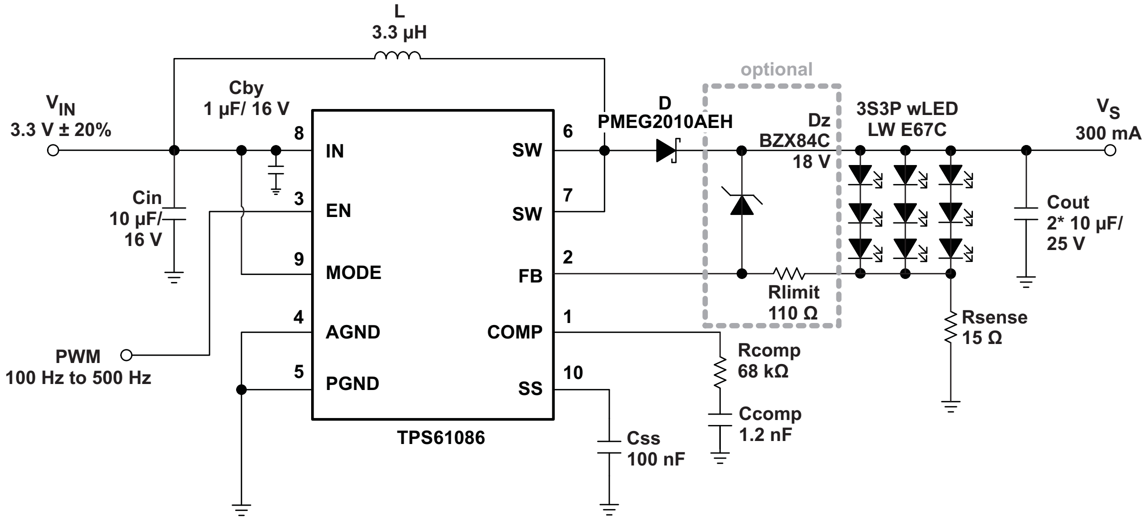


Figure 24. Simple Application (3.3 V input voltage - FORCED PWM MODE) for wLED Supply (3S3P) with Adjustable Brightness Control using a PWM Signal on the Enable Pin (with optional clamping Zener diode)

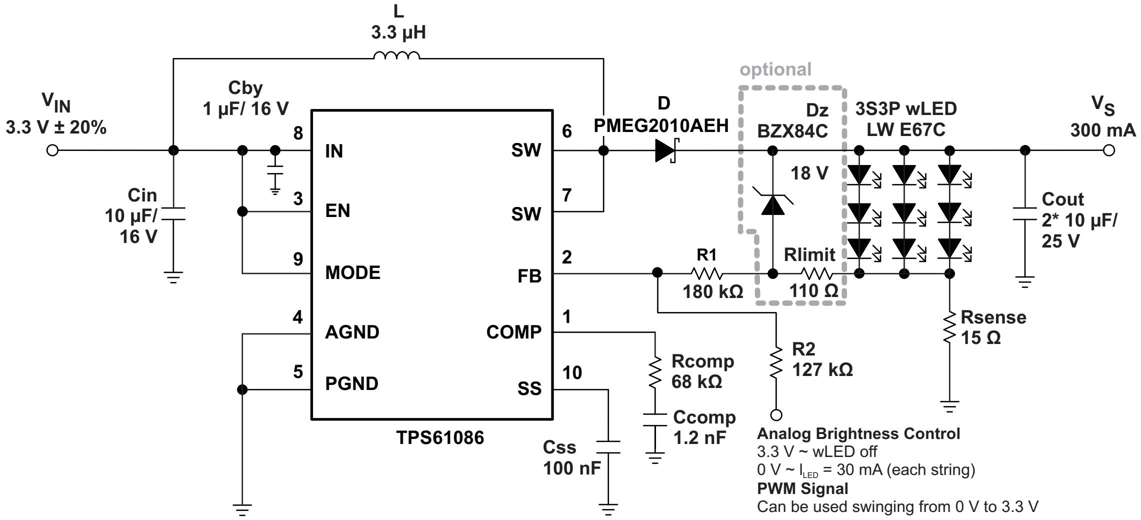


Figure 25. Simple Application (3.3 V input voltage - FORCED PWM MODE) for wLED Supply (3S3P) with Adjustable Brightness Control using an Analog Signal on the Feedback Pin (with optional clamping Zener diode)

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS61086DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS61086DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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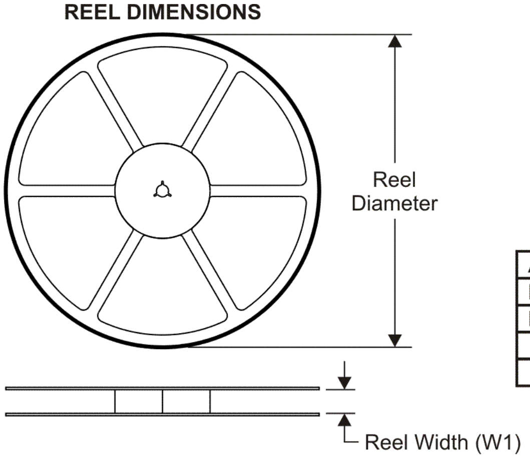
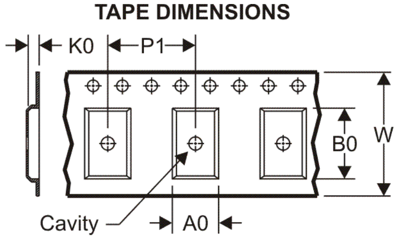
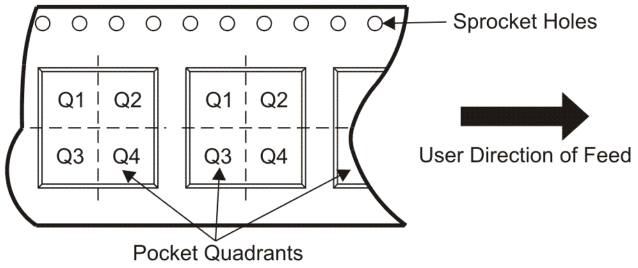
TAPE AND REEL INFORMATION


REEL DIMENSIONS


TAPE DIMENSIONS

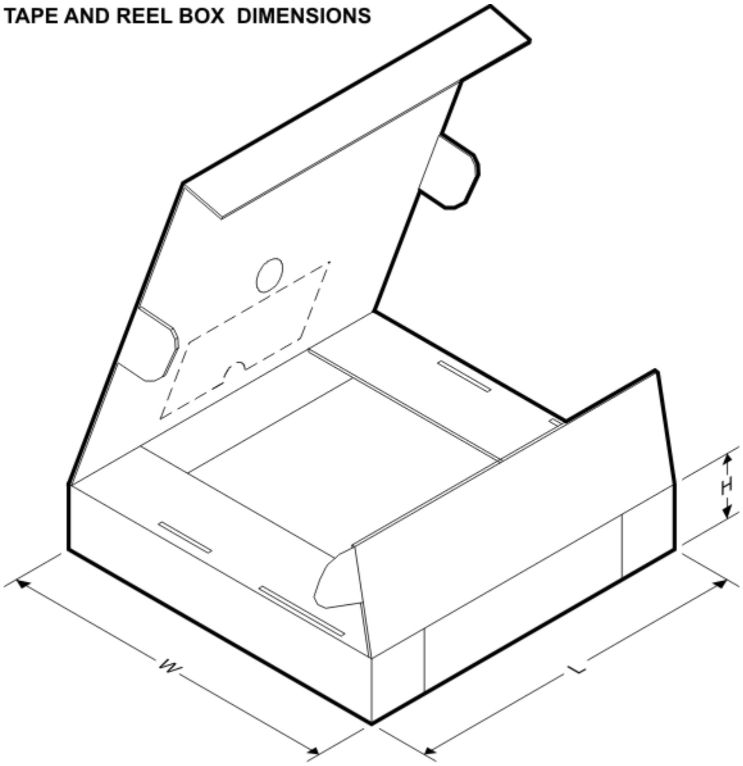
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61086DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61086DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

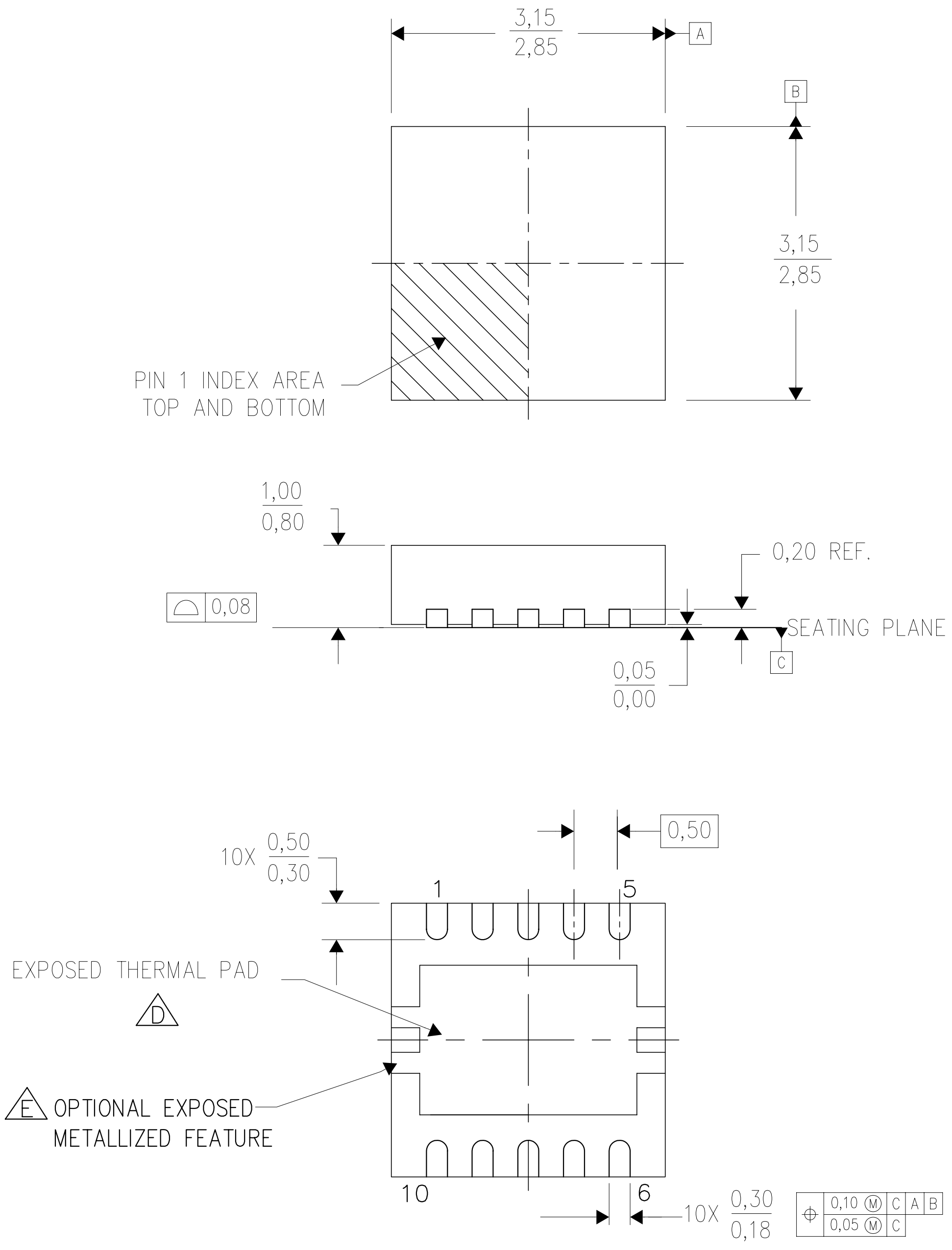
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61086DRCR	SON	DRC	10	3000	346.0	346.0	29.0
TPS61086DRCT	SON	DRC	10	250	190.5	212.7	31.8

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



4204102-3/J 01/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

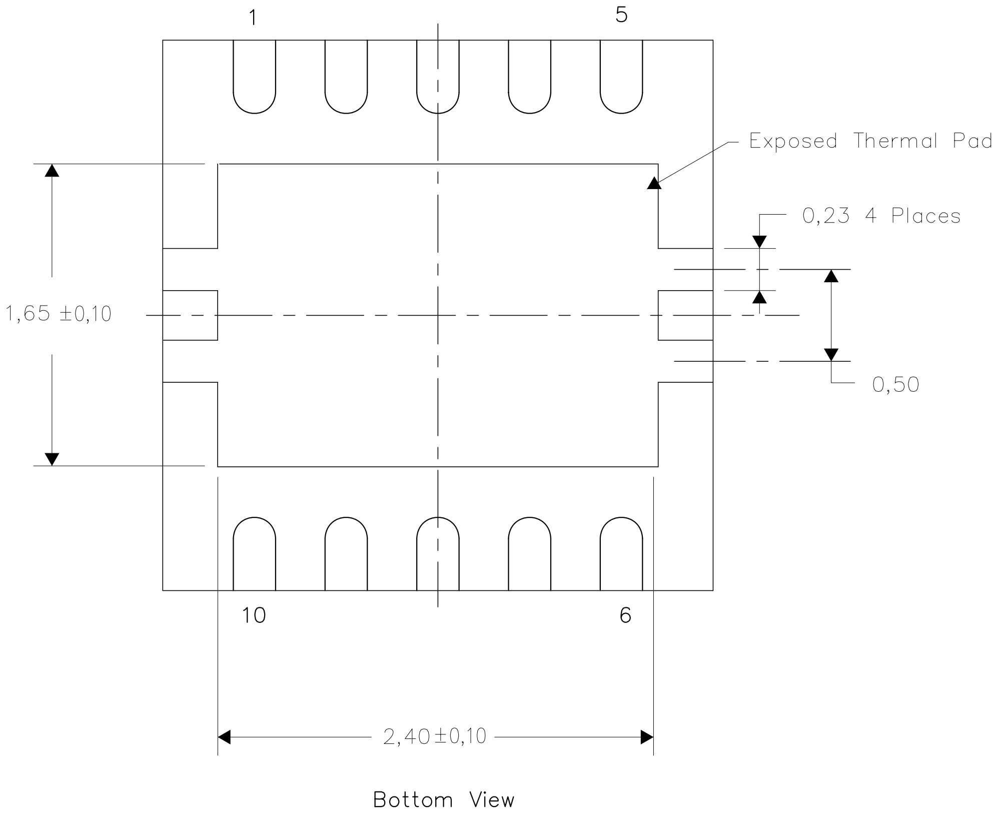
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

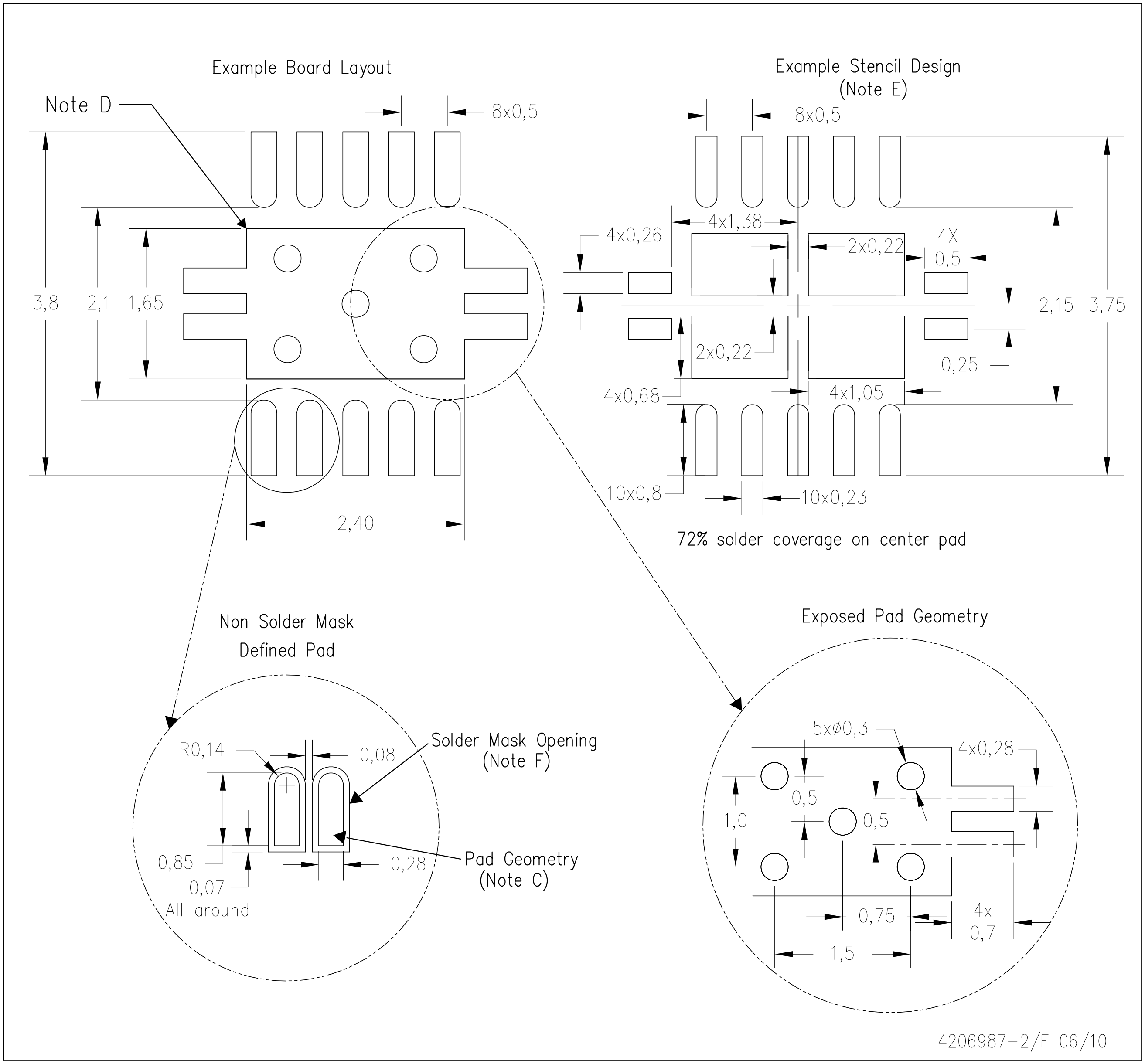


Exposed Thermal Pad Dimensions

4206565–3/L 02/11

NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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