SAM R34/R35 Low Power LoRa® Sub-GHz SiP Datasheet

Introduction

The SAM R34/R35 is a family of ultra-low power microcontrollers combined with a UHF transceiver communication interface. It uses a 32-bit ARM® Cortex® -M0+ processor and offers up to 256 KB of Flash and 40 KB of SRAM, including an area of battery backed-up SRAM. The UHF transceiver supports LoRa® and FSK modulation. LoRa technology is a spread spectrum protocol optimized for low data-rate, ultra-long range signaling. It is ideal for battery-powered remote sensors and controls.

The SAM R34 includes an integrated microcontroller with USB and the UHF transceiver, making it suitable for USB dongle applications or for software updates via USB. The SAM R35 offers the same microcontroller functions along with the UHF transceiver without the USB interface.

Features

Operational Features

- Processor:
  - ARM Cortex -M0+ CPU running at up to 48 MHz (2.46CoreMark®/MHz)
  - Single-Cycle Hardware Multiplier
  - Micro Trace Buffer (MTB)
- Memory:
  - In-System Self-Programmable Flash Memory, with options for sizes - 256 KB, 128 KB or 64 KB
  - Static Random Access Memory (SRAM) with options for sizes - 32 KB, 16 KB or 8KB
  - 8 KB low-power RAM with battery backup retention (with 4 KB option)
- System:
  - Power-on Reset (POR) and Brown-out Reset
  - Internal and External Clock Options with 48 MHz Digital Frequency Locked Loop (DFLL48M) and 48 MHz to 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - Up to 15 External Interrupts
  - One Non-Maskable Interrupt
  - Two Pin Serial Wire Debug (SWD) Programming, Test and Debugging Interfaces
- Operating Voltage: 1.8V- 3.6V
- Low Power Consumption
  - Transceiver:
    - RX = 16 mA (typical)
    - RFO_HF = 33 mA (typical)

        - PA_BOOST = 95 mA (typical)
    - MCU:
        - Idle and Standby Sleep Modes
        - SleepWalking peripherals
- Temperature Range: -40°C to +85°C (Industrial)

RF/Analog Features

- Integrated LoRa Technology Transceiver:
    - Tri-band Coverage
        - 137 MHz to 175 MHz
        - 410 MHz to 525 MHz
        - 862 MHz to 1020 MHz
    - +20 dBm (100 mW) Max Power (VDDANA > 2.4 VDC)
    - +17 dBm (50 mW) Max Power (Regulated PA)
    - +13 dBm (20 mW) High-efficency PA
- High Sensitivity:
    - Down to -136 dBm (LoRaWAN™ protocol compliant modes)
    - Down to -148 dBm (proprietary narrowband modes)
- Up to 168 dB Maximum Link Budget
- Robust Front-End: IIp3 = -11 dBm
- Excellent Blocking Immunity
- Low RX Current of 17 mA (typical)
- Fully Integrated Synthesizer with a Resolution of 61 Hz
- LoRa Technology, (G)FSK, (G)MSK and OOK Modulation
- Preamble Detection
- 127 dB Dynamic Range RSSI
- Automatic RF Sense and CAD with Ultra-Fast Automatic Frequency Control (AFC) Packet Engine up to 256 bytes with Cyclic Redundancy Check (CRC)

Peripheral Information

- 12-Channel Direct Memory Access Controller (DMAC)
- 12-Channel Event System
- Three 16-bit Timer/Counters (TC), configurable as either of the following:
    - One 8-bit TC with compare/capture channels
    - One 16-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
- Three 16-bit Timer/Counters for Control (TCC), with Extended Functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized Pulse Width Modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increases resolution with up to five bit and reduces quantization error
- 32-bit Real Time Counter (RTC) with Clock/Calendar Function
- Watchdog Timer (WDT)

- CRC-32 Generator
- One Full-Speed (12 Mbps) Universal Serial Bus (USB) 2.0 Interface:
  - Embedded host and device function
  - Eight endpoints
- Up to Five Serial Communication Interfaces (SERCOM), each configurable to operate as either of the following:
  - USART with full-duplex and single-wire half-duplex configuration
  - I2C up to 3.4 MHz
  - Serial Peripheral Interface (SPI)
  - Local Interconnect Network (LIN) Slave
- One 12-bit, 1 Msps Analog-to-Digital Converter (ADC) with up to Eight External Channels:
  - Differential and single-ended input
  - 1/2x to 16x programmable gain stage
  - Automatic offset and gain error compensation
  - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
- Two Analog Comparators (AC) with Window Compare Function
- Peripheral Touch Controller (PTC):
  - 48-channel capacitive touch and proximity sensing

Package Information

- 27 Programmable I/O Pins
- 64 Lead Ball Grid Array (BGA)

Table of Contents

1. Description

The SAM R34/R35 devices are a series of ultra-low power microcontrollers equipped with a UHF transceiver. It uses the 32-bit ARM Cortex-M0+ processor at max. 48 MHz (2.46 CoreMark/MHz) and offers 256 KB of Flash and 40 KB of SRAM. Sophisticated power management technologies, such as power domain gating, SleepWalking, ultra-low power peripherals and more, allow for very low line-power consumptions.

The UHF transceiver supports LoRa and FSK modulation schemes. The LoRa technology is optimized for long-range communication with minimal line-power demand. The transceiver can work from frequencies of 137 MHz to 1020 MHz. Maximum transmit power is +20 dBm without an external amplification. Operational frequency bands and power limits are defined by local regulations and the LoRa Alliance. LoRa network stack regional options insure compliance. FSK modulation is also supported for applications including IEEE 802.15.4g, WiSUN, and legacy proprietary networks.

All devices have accurate low power external and internal oscillators. Different clock domains can be independently configured to run at different frequencies, enabling power-saving by running each peripheral at its optimal clock frequency, thus maintaining a high CPU frequency while reducing power consumption.

The SAM R34/R35 devices have four software-selectable sleep modes: Idle, Standby, Backup and Off. In Idle mode, the CPU is stopped while all other functions may be kept running. In Standby mode, all clocks and functions are stopped except those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking, which allows some peripherals to wake-up from sleep based on predefined conditions, thus allowing some internal operations like DMA transfer and/or the CPU to wake-up only when needed; for example, when a threshold is crossed or a result is ready. The event system supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in Standby mode. Off mode is not advised, as high impedance on the internal SPI bus results in metastability.

The SAM R34/R35 devices have two software-selectable performance levels (PL0 and PL2) allowing the user to scale the lowest core voltage level that supports the operating frequency. To further minimize current consumption, specifically leakage dissipation, the devices utilize a power domain gating technique with retention to turn off some logic areas while keeping their logic state. This technique is fully handled in hardware.

The Flash program memory can be reprogrammed in-system through the Serial Wire Debug (SWD) interface. The same interface can also be used for non-intrusive on-chip debugging of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM R34/R35 devices are supported with a full suite of programs and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

2. Configuration Summary

Table 2-1. Configuration Summary

Parameter	SAM R34	SAM R35
Total Pins	64	64
General Purpose I/O pins (GPIOs)	27	27
Flash	256 KB	256 KB
Flash RWW Section	8 KB	8 KB
System SRAM	32 KB	32 KB
Low Power SRAM	8 KB	8 KB
Timer Counter (TC) Instances	3	3
Waveform Output Channels per TC Instance	2	2
Timer Counter for Control (TCC) Instances	3	3
Waveform Output Channels per TCC	4/2/2	4/2/2
USB Interface	1	0
Serial Communication Interface (SERCOM) Instances	5+1 (1)	5+1 (1)
Analog-to-Digital Converter (ADC) Channels	8	8
Analog Comparators (AC)	2	2
Real-Time Counter (RTC)	Yes	Yes
RTC Alarms	1	1
RTC Compare Values	1 for 32-bit value or 2 for 16-bit values	1 for 32-bit value or 2 for 16-bit values
External Interrupt Lines	15	15
Maximum CPU Frequency	48 MHz	48 MHz
Package	BGA	BGA

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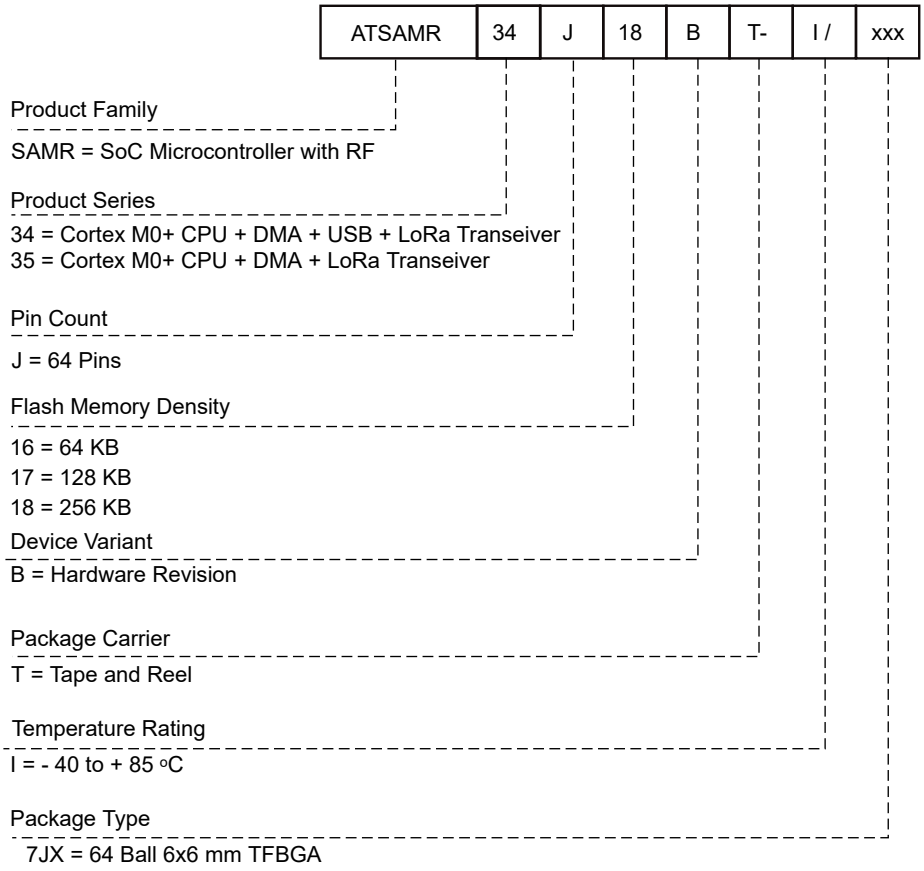
Parameter	**SAM R34**	**SAM R35**
32.768 kHz Crystal Oscillator (XOSC32K)	External	External
Oscillators	• 16 MHz crystal oscillator for TRX (XOSCRF) • 0.4-32 MHz crystal oscillator (XOSC) • 32.768 kHz external oscillator (OSC32K) • 32 kHz ultra-low power internal oscillator (OSCULP32K) • 8 MHz high-accuracy internal oscillator (OSC8M) • 48 MHz Digital Frequency Locked Loop (DFLL48M) • 96 MHz Fractional Digital Phased Locked Loop (FDPLL96)	• 16 MHz crystal oscillator for TRX (XOSCRF) • 0.4-32 MHz crystal oscillator (XOSC) • 32.768 kHz external oscillator (OSC32K) • 32 kHz ultra-low power internal oscillator (OSCULP32K) • 8 MHz high-accuracy internal oscillator (OSC8M) • 48 MHz Digital Frequency Locked Loop (DFLL48M) • 96 MHz Fractional Digital Phased Locked Loop (FDPLL96)
Event System Channels	12	12
SW Debug Interface	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes

1. SERCOM4 is internally connected to the Transceiver (TRX).

3. Ordering Information for SAM R34/R35

Figure 3-1. SAM R34/R35 Ordering Information



3.1 SAM R34/R35 Ordering Codes

Table 3-1. SAM R34/R35 Ordering Codes

Ordering Code	Description
ATSAMR34J16BT-I/7JX	LoRa SiP Transceiver USB 64K Flash 8K SRAM, 4KB LP SRAM, T&R
ATSAMR34J17BT-I/7JX	LoRa SiP Transceiver USB 128K Flash 16K SRAM, 8KB LP SRAM, T&R
ATSAMR34J18BT-I/7JX	LoRa SiP Transceiver USB 256K Flash 32K SRAM, 8KB LP SRAM, T&R
ATSAMR35J16BT-I/7JX	LoRa SiP Transceiver 64K Flash 8K SRAM, 4KB LP SRAM, T&R
ATSAMR35J17BT-I/7JX	LoRa SiP Transceiver 128K Flash 16K SRAM, 8KB LP SRAM, T&R
ATSAMR35J18BT-I/7JX	LoRa SiP Transceiver 256K Flash 32K SRAM, 8KB LP SRAM, T&R

4. System Introduction

4.1 SAM R34/R35 Pinout Details

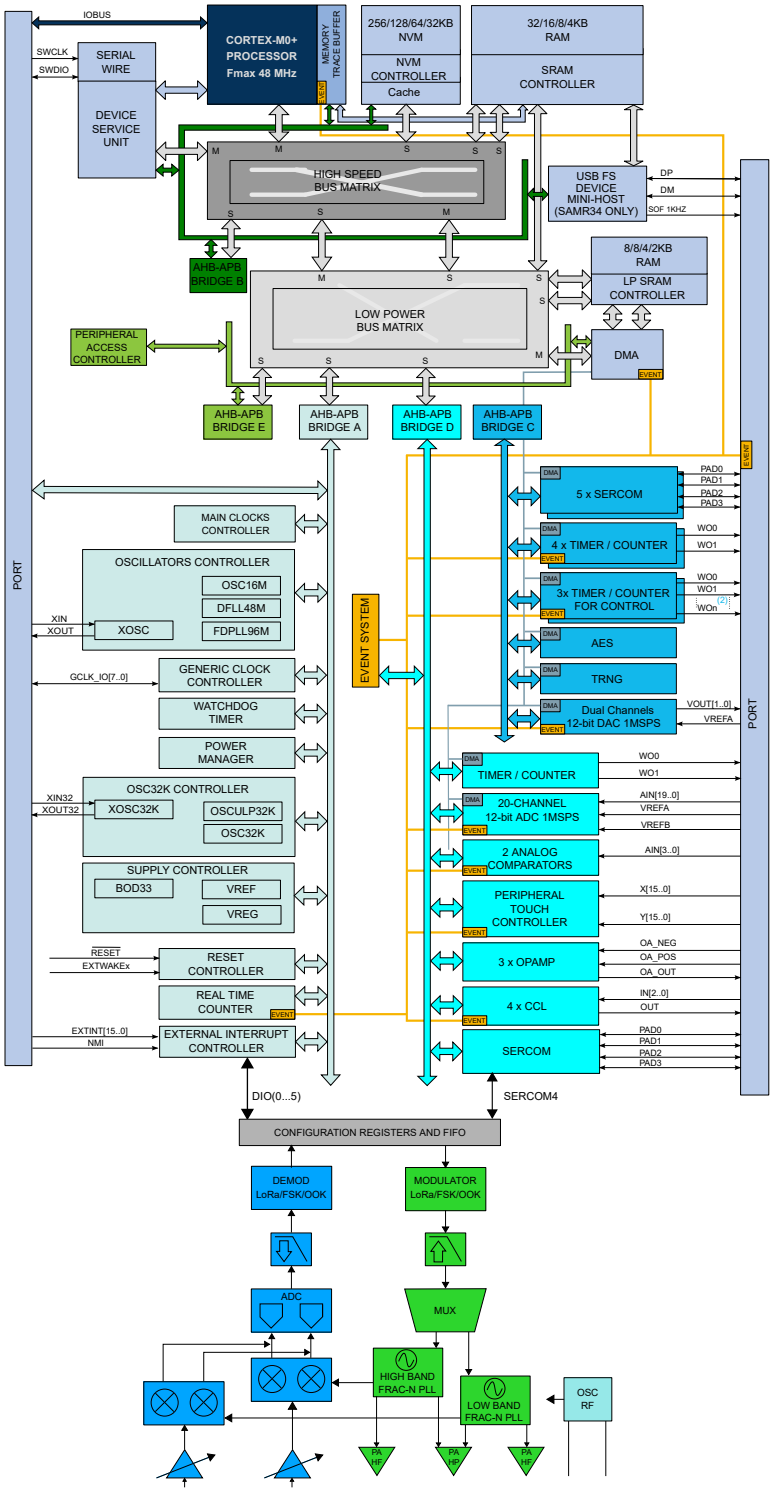
Figure 4-1. SAM R34/R35 Pin Placement

	1	2	3	4	5	6	7	8
A	RFI_HF	GND_RF	PA00	PA01	VDDCORE	VSW	VDDIN	VDDIO2
B	RFO_HF	GND_RF	GNDANA	PB02	GND	RESET*	GND	PA24
C	VBAT_RF	VDDANA	PB03	PA05	PA30	PA28	PB23	PA25
D	VR_PA	RXTX	PA04	GND	PA31	GND	PA23	PA22
E	GND_RF	GNDANA	PA06	PA27	PB22	PA17	PA18	PA19
F	PA_BOOST	GND_RF	PA07	PA08	PA09	PA13	PA16	PA14
G	RFO_LF	GND_RF	GND_RF	VDDI01	GND_RF	GND_RF	GND_RF	PA15
H	RFI_LF	VR_ANA	VBAT_ANA	VR_DIG	GND_RF	XTA	XTB	VBAT_DIG

4.2 SiP Block Diagram

The following figure illustrates the SAM R34/R35 System-in-Package (SiP) block diagram.

Figure 4-2. System Block Diagram with MCU and Transceiver



4.3 Peripheral Key Table

Table 4-1. Peripheral Key Table

Peripheral	Description	Reference Document	Topic # and Keyword	Notes
AC	Analog Comparator	1	43. AC – Analog Comparators	
ADC	Analog-to-Digital Converter	1	42. ADC – Analog-to-Digital Converter	
AES	Advanced Encryption Engine	1	38. AES – Advanced Encryption Standard	
BOD33	Brown-out Detector	1	23. SUPC – Supply Controller	
CCL	Configurable Custom Logic	1	40. CCL – Configurable Custom Logic	
CRC	Cyclic Redundancy Check-sum	1	15.11.3 32-bit Cyclic Redundancy Check CRC32	
DAC	Digital-to-Analog Converter	1	44. DAC – Digital-to-Analog Converter	
DMA	Direct Memory Access Controller	1	26. DMAC – Direct Memory Access Controller	
EIC	External Interrupt	1	27. EIC – External Interrupt Controller	
EVSYS	Event System	1	30. EVSYS – Event System	
GCLK	Generic Clock Control	1	17. GCLK - Generic Clock Controller	
I2C	Inter-integrated Circuit Interface	1	34. SERCOM I2C – SERCOM Inter-integrated Circuit	SERCOM 4 Reserved
MCLK	Main Clock Control	1	18. MCLK – Main Clock	
NVMCTRL	Nonvolatile Memory Controller	1	28. NVMCTRL – Nonvolatile Memory Controller	
OPAMP	Operational Amplifier	1	41. OPAMP – Operational Amplifier Controller	
OSC32KCTRL	32 kHz Clock	1	22. OSC32KCTRL – 32KHz Oscillators Controller	
OSCCTRL	Clock Control	1	21. OSCCTRL – Oscillators Controller	
PA_BOOST	RF Output High-power	5	5.4.2. RF Power Amplifiers	
PM	Power Management	1	20. PM – Power Manager	

.....continued

Peripheral	Description	Reference Document	Topic # and Keyword	Notes
PORT	GPIO Port Controller	1	29. PORT - I/O Pin Controller	Limited to 27 Ports
PORT	Power-On Reset	1	23. SUPC – Supply Controller	
PTC	Peripheral Touch Controller (RC)	1	45. PTC - Peripheral Touch Controller	
RFI_HF	RF Input High Frequency	5	5.5. Receiver Description	
RFI_LF	RF Input Low Frequency	5	5.5. Receiver Description	
RFO_HF	RF Output High Frequency	5	5.4.2. RF Power Amplifiers	
RFO_LF	RF Output Low Frequency	5	5.4.2. RF Power Amplifiers	
RSTC	Reset Control	1	19. RSTC – Reset Controller	
RTC	Real-Time Counter	1	25. RTC – Real-Time Counter	
SPI	Serial Peripheral Interface	1	33. SERCOM SPI – SERCOM Serial Peripheral Interface	SERCOM 4 Reserved
TC	Timer Counter	1	35. TC – Timer/Counter	
TCC	Timer Counter for Control	1	36. TCC – Timer/Counter for Control Applications	
TRNG	Random Number Generator	1	37. TRNG – True Random Number Generator	
USART	Universal Synchronous and Asynchronous Receiver/Transmitter	1	32. SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter	SERCOM 4 Reserved
USB	Full-speed Universal Serial Bus 2.0 interface	1	39. USB – Universal Serial Bus	SAMR34 Only
VBAT	External Battery Input	1	23. SUPC – Supply Controller	
VSW	Switch Mode Power Output	1	50.2 Power Supply	
WDT	Watchdog Timer	1	24. WDT – Watchdog Timer	
XTA/B	RF Oscillator	5	5.3. Frequency Synthesis	

5. I/O Multiplexing and Considerations

5.1 Multiplexed Signals

By default, each pin is controlled by the PORT as a general purpose I/O and alternatively may be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0..31) in the PORT must be written to '1'. The selection of peripheral functions A to H are done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

Table 5-1. Port Function Multiplexing

Pin	I/O Pin	Supply	A		B (1)(2)						C	D	E	F	G	H	I
SAM R34/ R35			EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM (1)(2)	SERCOM-ALT	TC/TC C	TCC	COM	AC/GCLK/ SUPC	CCL
A3	PA00	VSWOUT	EXTINT[0]	EXTWAKE[0]	-	-	-	-	-	-	-	SERCOM1/ PAD[0]	TCC2/ WO[0]	-	-	-	-
A4	PA01	VSWOUT	EXTINT[1]	EXTWAKE[1]	-	-	-	-	-	-	-	SERCOM1/ PAD[1]	TCC2/ WO[1]	-	-	-	-
D3	PA04	VDDANA	EXTINT[4]	EXTWAKE[4]	VREFB	AIN[4]	AIN[0]	-	-	OAOUT[2]	-	SERCOM0/ PAD[0]	TCC0/ WO[0]	-	-	-	CCL0/ IN[0]
C4	PA05	VDDANA	EXTINT[5]	EXTWAKE[5]	-	AIN[5]	AIN[1]	-	-	OAPOS[2]	-	SERCOM0/ PAD[1]	TCC0/ WO[1]	-	-	-	CCL0/ IN[1]
E3	PA06	VDDANA	EXTINT[6]	EXTWAKE[6]	-	AIN[6]	AIN[2]	-	Y[4]	OAPOS[0]	-	SERCOM0/ PAD[2]	TCC1/ WO[0]	-	-	-	CCL0/ IN[2]
F3	PA07	VDDANA	EXTINT[7]	EXTWAKE[7]	-	AIN[7]	AIN[3]	-	-	OAOUT[0]	-	SERCOM0/ PAD[3]	TCC1/ WO[1]	-	-	-	CCL0/ OUT[0]
F4	PA08	VDDIO	NMI	-	-	AIN[16]	-	X[0]	Y[6]	-	SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/ WO[0]	TCC1/ WO[2]	-	-	CCL1/ IN[3]
F5	PA09	VDDIO	EXTINT[9]	-	-	AIN[17]		X[1]	Y[7]	-	SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TCC0/ WO[1]	TCC1/ WO[3]	-	-	CCL1/ IN[1]
F6	PA13	VDDIO	EXTINT[13]	-	-	-	-	-	-	-	SERCOM2/ PAD[1]	SERCOM4/ PAD[1]	TCC2/ WO[1]	TCC0/ WO[7]	-	AC/CMP[1]	-
F8	PA14	VDDIO	EXTINT[14]	-	-	-	-	-	-	-	SERCOM2/ PAD[2]	SERCOM4/ PAD[2]	TC4/ WO[0]	TCC0/ WO[4]	-	GCLK_IO[0]	-
G8	PA15	VDDIO	EXTINT[15]	-	-	-	-	-	-	-	SERCOM2/ PAD[3]	SERCOM4/ PAD[3]	TC4/ WO[1]	TCC0/ WO[5]	-	GCLK_IO[1]	-
F7	PA16	VDDIO	EXTINT[0]	-	-	-	-	X[4]	-	-	SERCOM1/ PAD[0]	SERCOM3/ PAD[0]	TCC2/ WO[0]	TCC0/ WO[6]	-	GCLK_IO[2]	CCL0/ IN[0]
E6	PA17	VDDIO	EXTINT[1]	-	-	-	-	X[5]	-	-	SERCOM1/ PAD[1]	SERCOM3/ PAD[1]	TCC2/ WO[1]	TCC0/ WO[1]	-	GCLK_IO[3]	CCL0/ IN[1]
E7	PA18	VDDIO	EXTINT[2]	-	-	-	-	X[6]	-	-	SERCOM1/ PAD[2]	SERCOM3/ PAD[2]	TC4/ WO[0]	TCC0/ WO[2]	-	AC/CMP[0]	CCL0/ IN[2]
E8	PA19	VDDIO	EXTINT[3]	-	-	-	-	X[7]	-	-	SERCOM1/ PAD[3]	SERCOM3/ PAD[3]	TC4/ WO[1]	TCC0/ WO[3]	-	AC/CMP[1]	CCL0/ OUT[0]
D8	PA22	VDDIO	EXTINT[6]	-	-	-	-	X[10]	-	-	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC0/ WO[0]	TCC0/ WO[4]	-	GCLK_IO[6]	CCL2/ IN[0]
D7	PA23	VDDIO	EXTINT[7]	-	-	-	-	X[11]	-	-	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC0/ WO[1]	TCC0/ WO[5]	USB/SO F 1 kHz[6]	GCLK_IO[7]	CCL2/ IN[1]
B8	PA24	VDDIO	EXTINT[12]	-	-	-	-	-	-	-	SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC1/ WO[0]	TCC1/ WO[2]	USB/ DM[6]	-	CCL2/ IN[2]
C8	PA25	VDDIO	EXTINT[13]	-	-	-	-	-	-	-	SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC1/ WO[1]	TCC1/ WO[3]	USB/ DP[6]	-	CCL2/ OUT[2]
E5	PB22	VDDIN	EXTINT[6]	-	-	-	-	-	-	-	-	SERCOM5/ PAD[2]	TC3/ WO[0]	-	-	GCLK_IO[0]	CCL0/ IN[0]
C7	PB23	VDDIN	EXTINT[7]	-	-	-	-	-	-	-	-	SERCOM5/ PAD[3]	TC3/ WO[1]	-	-	GCLK_IO[1]	CCL0/ OUT[0]
E4	PA27	VDDIN	EXTINT[15]	-	-	-	-	-	-	-	-	-	-	-	-	GCLK_IO[0]	-

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Pin	I/O Pin	Supply	A		B (1)(2)						C	D	E	F	G	H	I
SAM R34/ R35			EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM (1)(2)	SERCOM-ALT	TC/TC C	TCC	COM	AC/GCLK/ SUPC	CCL
C6	PA28	VDDIN	EXTINT[8]	-	-	-	-	-	-	-	-	-	-	-	-	GCLK_IO[0]	-
C5	PA30	VDDIN	EXTINT[10]	-	-	-	-	-	-	-	-	SERCOM1/ PAD[2]	TCC1/ WO[0]	-	SWCLK	GCLK_IO[0]	CCL1/ IN[0]
D5	PA31	VDDIN	EXTINT[11]	-	-	-	-	-	-	-	-	SERCOM1/ PAD[3]	TCC1/ WO[1]	-	SWDIO(3)	-	CCL1/ OUT[1]
B4	PB02	VSWOUT	EXTINT[2]	-	-	AIN[10]	-	-	-	-	-	SERCOM5/ PAD[0]	TC2/ WO[0]	-	-	SUPC/ OUT[1]	CCL0/ OUT[0]
C3	PB03	VSWOUT	EXTINT[3]	-	-	AIN[11]	-	-	-	-	-	SERCOM5/ PAD[1]	TC2/ WO[1]	-	-	SUPC/VBAT	

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I2Cmode. See 5.3.3 SERCOM I2C Pins .
3. This function is only activated in the presence of a debugger.
4. When an analog peripheral is enabled, the analog output of the peripheral interferes with the alternative functions of this pin. This is also true even when the peripheral is used for internal purposes.
5. Clusters of multiple GPIO pins are sharing the same supply pin. See 5.3.4 GPIO Cluster.
6. USB is not available on the SAM R35 devices.

5.2 Internal Multiplexed Signals

By default, each pin is controlled by the PORT as a general purpose I/O and alternatively may be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to '1'. The selection of peripheral functions A to H are done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

Table 5-2. Internal Multiplexed Signals

Internal Signal	I/O Pin	Supply	Type	A		B						C	D	E	F	G	H	I
				EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM	SERCOM-ALT	TC/TC C	FECTRL/ TCC/ SERCOM	COM	AC/GCLK/ SUPC	CCL
DIO0	PB16	VDDIO	I/O	EXTINT[0]	-	-	-	-	-	-	-	SERCOM5/ PAD[0]	-	TCC2/ WO[0]	TCC0/ WO[4]	-	GCLK_IO[2]	CCL3/ IN[11]
DIO1/ DCLK	PA11	VDDIO	I/O	EXTINT[11]	-	-	AIN[19]	-	X[3]	Y[9]	-	SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TCC1/ WO[1]	TCC0/ WO[3]	-	GCLK_IO[5]	CCL1/ OUT[1]
DIO2/ DATA	PA12	VDDIO	I/O	EXTINT[12]	-	-	-	-	-	-	-	SERCOM2/ PAD[0]	SERCOM4/ PAD[0]	TCC2/ WO[0]	TCC0/ WO[6]	-	AC/CMP[0]	-
DIO3	PB17	VDDIO	I/O	EXTINT[1]	-	-	-	-	-	-	-	SERCOM5/ PAD[1]	-	TCC2/ WO[1]	TCC0/ WO[5]	-	GCLK_IO[3]	CCL3/ OUT[3]
DIO4	PA10	VDDIO	I/O	EXTINT[10]	-	-	AIN[18]	-	X[2]	Y[8]	-	SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TCC1/ WO[0]	TCC0/ WO[2]	-	GCLK_IO[4]	CCL1/ IN[5]
DIO5	PB00	VDDANA	I/O	EXTINT[0]	-	-	AIN[8]	-	-	-	-	-	SERCOM5/ PAD[2]	TCC3/ WO[0]	-	-	SUPC_PSOK	CCL0/ IN[1]
RF_RST	PB15	VDDIO	I/O	EXTINT[15]	-	-	-	-	X[15]	-	-	SERCOM4/ PAD[3]	-	TCC0/ WO[1]	-	-	GCLK_IO[1]	CCL3/ IN[10]
MOSI	PB30	VDDIO	I/O	EXTINT[14]	-	-	-	-	-	-	-	-	SERCOM5/ PAD[0]	TCC0/ WO[0]	SERCOM4/ PAD[2]	-	-	-
SEL	PB31	VDDIO	I/O	EXTINT[15]	-	-	-	-	-	-	-	-	SERCOM5/ PAD[1]	TCC0/ WO[1]	SERCOM4/ PAD[1]	-	-	-

.....continued

Internal Signal	I/O Pin	Supply	Type	A		B						C	D	E	F	G	H	I
				EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM	SERCOM-ALT	TC/TCC	FECTRL/ TCC/ SERCOM	COM	AC/GCLK/ SUPC	CCL
SCLK	PC18	VDDIO	I/O	-	-	-	-	-	-	-	-	-	-	-	SERCOM4/ PAD[3]	-	-	-
MISO	PC19	VDDIO	I/O	-	-	-	-	-	-	-	-	-	-	-	SERCOM4/ PAD[0]	-	-	-

5.3 Other Functions

5.3.1 Oscillator Pinout

The oscillators are not mapped to the normal PORT functions, and their multiplexing is controlled by registers in the Oscillator Controller (OSCCTROL) and in the 32kHz Oscillators Controller (OSC32KCTRL).

Table 5-3. Oscillator Pinout

Oscillator	Supply	Signal	I/O Port
XOSC	VDDIO	XIN	PA14
		XOUT	PA15
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

5.3.2 Serial Wire Debug Interface Pins

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 5-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O Pin
SWCLK	VDDIN	PA30
SWDIO	VDDIN	PA31

5.3.3 SERCOM I^2C Pins

Table 5-5. SERCOM Pins Supporting I^2C

Device	Pins Supporting I^2C HS Mode
SAM R34/R35	PA08, PA09, PA13, PA16, PA17, PA22, PA23

5.3.4 GPIO Cluster

Table 5-6. GPIO Clusters

Package	Cluster	GPIO													Supply Pins Connected to the Cluster
64 Pins	1	PA31	PA30	-	-	-	-	-	-	-	-	-	-	-	VDDIN C4/GND D4
	2	PA28	PA27	PB23	PB22	-	-	-	-	-	-	-	-	-	VDDIN C4/GND D4 and VDDIO C6/GND C5
	3	PA25	PA24	PA23	PA22	-	-	PA19	PA18	PA17	PA16	PA15	PA14	PA13	VDDIO C6/GND C5 and VDDIO F3/GND F4
	4	-	-	PA09	PA08	-	-	-	-	-	-	-	-	-	VDDIO F3/GND F4
	5	PA07	PA06	PA05	PA04	-	-	-	-	-	-	-	-	-	VDDANA C1/GNDANA C3
	6	-	-	PA01	PA00	PB03	PB02	-	-	-	-	-	-	-	VDDANA C1/GNDANA C3

5.3.5 TCC Configurations

The SAML21 has three instances of the Timer/Counter for Control applications (TCC) peripheral, TCC<2:0>.

Table 5-7. TCC Configuration Summary

TCC No.	Channels (CC_NUM)	Waveform Output (WO_NUM)	Counter Size	Fault	Dithering	Output Matrix	Dead Time Insertion (DTI)	SWAP	Pattern Generation
0	4	8	24-bit	Yes	Yes	Yes	Yes	Yes	Yes
1	2	4	24-bit	Yes	Yes	—	—	—	Yes
2	2	2	16-bit	Yes		—	—	—	—

Note: The number of CC register (CC_NUM)_ for each TCC corresponds to the number of compare/capture channels to ensure that a TCC can have more Waveform Outputs (WO_NUM) than CC registers.

6. Signal Description

This section provides the required information to understand the origin and the function of each such signal. The nature of a SIP results in the situation where the package pins may be bonded to the microcontroller die or the transceiver die. There are also signals bonded in-between the two dies.

6.1 Signal Details

This section provides the naming and functional description of the internal and external signals. 5. I/O Multiplexing and Considerations describes the routing of these signals between the MCU core and transceiver subsystem and to the external package pins.

Table 6-1. Signal Descriptions List

Signal Name	Function	Type
Analog Comparators (AC)		
AIN<3:0>	AC analog inputs	Analog
CMP<1:0>	AC comparator outputs	Digital
Analog Digital Converter (ADC)		
AIN<19:0>	ADC analog inputs	Analog
VREFB	ADC voltage external reference B	Analog
Operational Amplifier (OPAMP)		
OANEG<2:0>	OPAMP analog negative inputs	Analog
OAPOS<2:0>	OPAMP analog positive inputs	Analog
OAOUT<2:0>	OPAMP analog outputs	Analog
External Interrupt Controller (EIC)		
EXTINT<15:0>	External interrupts inputs	Digital
NMI	External non-maskable interrupt input	Digital
Reset Controller (RSTC)		
EXTWAKE<7:0>	External wake-up inputs	Digital
Generic Clock Generator (GCLK)		
GCLK_IO<7:0>	Generic clock (source clock inputs or generic clock generator output)	Digital
Custom Control Logic (CCL)		
IN<11:0>	Logic inputs	Digital
OUT<3:0>	Logic outputs	Digital
Supply Controller (SUPC)		
VBAT	External battery supply inputs	Analog
PSOK	Main power supply OK input	Digital

.....continued

Signal Name	Function	Type
OUT<1:0>	Logic outputs	Digital
Power Manager (PM)		
RESETN	Active low Reset input	Digital
Serial Communication Interface (SERCOMx)		
PAD<3:0>	SERCOM Input/Output pads	Digital
Oscillators Control (OSCCTRL)		
XIN	Crystal or external clock input	Analog/Digital
XOUT	Crystal output	Analog
32KHz Oscillators Control (OSC32KCTRL)		
XIN32	32KHz crystal or external clock input	Analog/Digital
XOUT32	32KHz crystal output	Analog
Timer Counter (TCx)		
WO<1:0>	Waveform outputs	Digital
Timer Counter (TCCx)		
WO<7:0>	Waveform outputs	Digital
General Purpose I/O (PORT)		
PA01-PA00	Parallel I/O controller I/O Port A	Digital
PA09-PA04	Parallel I/O controller I/O Port A	Digital
PA25-PA22	Parallel I/O controller I/O Port A	Digital
PA28-PA27	Parallel I/O controller I/O Port A	Digital
PA03-PB02	Parallel I/O controller I/O Port B	Digital
PA23-PB22	Parallel I/O controller I/O Port B	Digital
Universal Serial Bus (USB)		
DP	DP for USB (SAM R34 only)	Digital
DM	DM for USB (SAM R34 only)	Digital
External RF Signals		
RF_XTB	XTAL connection	OSC
RF_XTA	XTAL connection or TCXO input	OSC
VR_DIG	Regulated supply voltage for digital blocks	Reg Output
VBAT_ANA	Supply voltage for analog circuitry	Analog Power
VR_ANA	Regulated supply voltage for analog circuitry	Reg Output

.....continued		
Signal Name	**Function**	**Type**
RFI_LF	RF input for bands 2 and 3	RF Input
RFO_LF	RF output for bands 2 and 3	RF Output
PA_BOOST	Optional high-power PA output, all frequency bands	RF Output
VR_PA	Regulated supply voltage for the PA	Reg Output
VBAT_RF	Supply voltage for RF blocks	RF Power
RFO_HF	RF output for band 1	RF Output
VBAT_DIG	Supply voltage for digital blocks	Digital Power
RXTX	RX/TX switch control: High in TX	Digital I/O
RFI_HF	RF input for band 1	RF Input
Internal Interconnect Signals		
DIO0	Digital I/O, software configured	I/O
DIO1/DCLK	Digital I/O, software configured	I/O
DIO2/DATA	Digital I/O, software configured	I/O
DIO3	Digital I/O, software configured	I/O
DIO4	Digital I/O, software configured	I/O
DIO5	Digital I/O, software configured	I/O
SCLK	SPI clock input	Input
MISO	SPI data output	Output
MOSI	SPI data input	Input
SEL	SPI chip select input	Input
RF_RST	Reset trigger input	I/O

7. Processor and Architecture

7.1 Cortex M0+ Processor

The SAM R34/R35 contains an ATSAML21J18B ARM Cortex-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex-M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com.

7.1.1 Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration in SAM R34/R35

Features	Cortex M0+ options	SAM R34/R35 configuration
Interrupts	External interrupts 0-32	29
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent - All software run in privileged mode only
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory including Flash memory and RAM
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores

7.1.1.1 Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)

  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).
    Note: When the CPU frequency is much higher than the APB frequency it is recommended to insert a memory read barrier after each CPU write to registers mapped on the APB. Failing to do so in such conditions may lead to unexpected behavior such as re-entering a peripheral interrupt handler just after leaving it.
- System Timer (SysTick)
  - The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com)
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section MTB-Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (http://www.arm.com).

Related Links

7.2 Nested Vector Interrupt Controller

7.1.1.2 Cortex M0+ Address Map

Table 7-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000	Micro Trace Buffer (MTB)

7.1.1.3 I/O Interface

The device allows direct access to PORT registers. Accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, so the Cortex M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O access to be sustained for as long as necessary.

7.2 Nested Vector Interrupt Controller

7.2.1 Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM R34/R35 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (http://www.arm.com).

7.2.2 Interrupt Line Mapping

Each of the 23 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a 1 to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing 1 to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 7-3. Interrupt Line Mapping

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32KHz Oscillators Controller SUPC - Supply Controller PAC - Protecion Access Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Counter	2
EIC – External Interrupt Controller	3
NVMCTRL – Non-Volatile Memory Controller	4
DMAC - Direct Memory Access Controller	5
USB - Universal Serial Bus	6
EVSYS – Event System	7
SERCOM0 – Serial Communication Interface 0	8
SERCOM1 – Serial Communication Interface 1	9
SERCOM2 – Serial Communication Interface 2	10
SERCOM3 – Serial Communication Interface 3	11
SERCOM4 – Serial Communication Interface 4	12

.....continued	
Peripheral Source	**NVIC Line**
SERCOM5 – Serial Communication Interface 5	13
TCC0 – Timer Counter for Control 0	14
TCC1 – Timer Counter for Control 1	15
TCC2 – Timer Counter for Control 2	16
TC0 – Timer Counter 0	17
TC1 – Timer Counter 1	18
TC4 – Timer Counter 4	19
ADC – Analog-to-Digital Converter	20
AC – Analog Comparator	21

7.3 Micro Trace Buffer

7.3.1 Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2 Overview

When enabled, the MTB records the changes in program flow that are reported by the Cortex-M0+ processor over the execution trace interface. This interface is shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. The information is stored by the MTB in the SRAM as trace packets. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB stores trace information into the SRAM and gives the processor access to the SRAM simultaneously. The MTB ensures that trace write accesses have priority over processor accesses.

An execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects a non-sequential change of the program pounter (PC) value. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-

M0+ Technical Reference Manual. The MTB has four programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit
- MASTER: Contains the main trace enable bit and other trace control fields
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location by a debug agent

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

7.4 High-Speed Bus System

7.4.1 Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

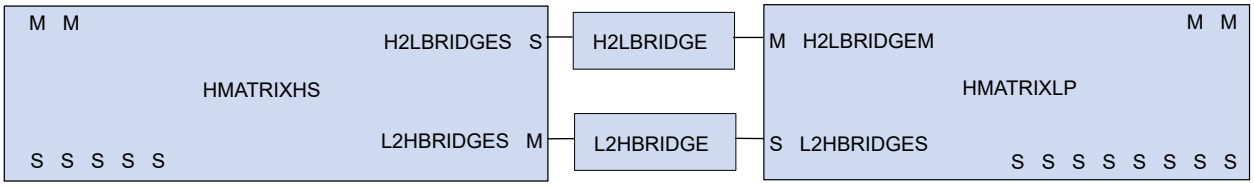
H2LBRIDGE has the following features:

- LP clock division support
- Write: Posted-write FIFO of 3 words, no bus stall until it is full
- Write: 1 cycle bus stall when full when LP clock is not divided
- 2 stall cycles on read when LP clock is not divided
- Ultra-Low Latency mode:
  - Suitable when the HS clock frequency is not above half the maximum device clock frequency
  - Removes all intrinsic bridge stall cycles (except those needed for LP clock ratio adaptation)
  - Enabled by writing a '1' in 0x41008120 using a 32-bit write access

L2HBRIDGE has the following features:

- LP clock division support
- Write: Posted-write FIFO of 1 word, no bus stall until it is full
- Write: 1 cycle bus stall when full when LP clock is not divided
- 2 stall cycles on read when LP clock is not divided
- Ultra-Low Latency mode:
  - Suitable when the HS clock frequency is not above half the maximum device clock frequency
  - Removes all intrinsic bridge stall cycles (except those needed for LP clock ratio adaptation)
  - Enabled by writing a '1' in 0x41008120 using a 32-bit write access

Figure 7-1. High-Speed Bus System Components



7.4.2 Configuration

Figure 7-2. Master-Slave Relations High-Speed Bus Matrix

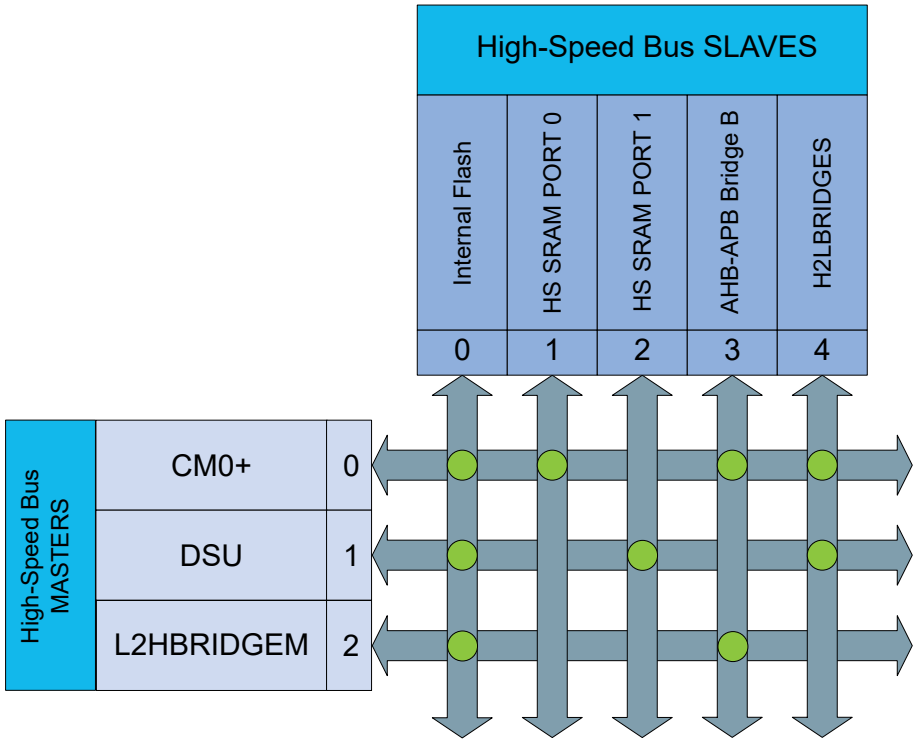


Figure 7-3. Master-Slave Relations Low-Power Bus Matrix

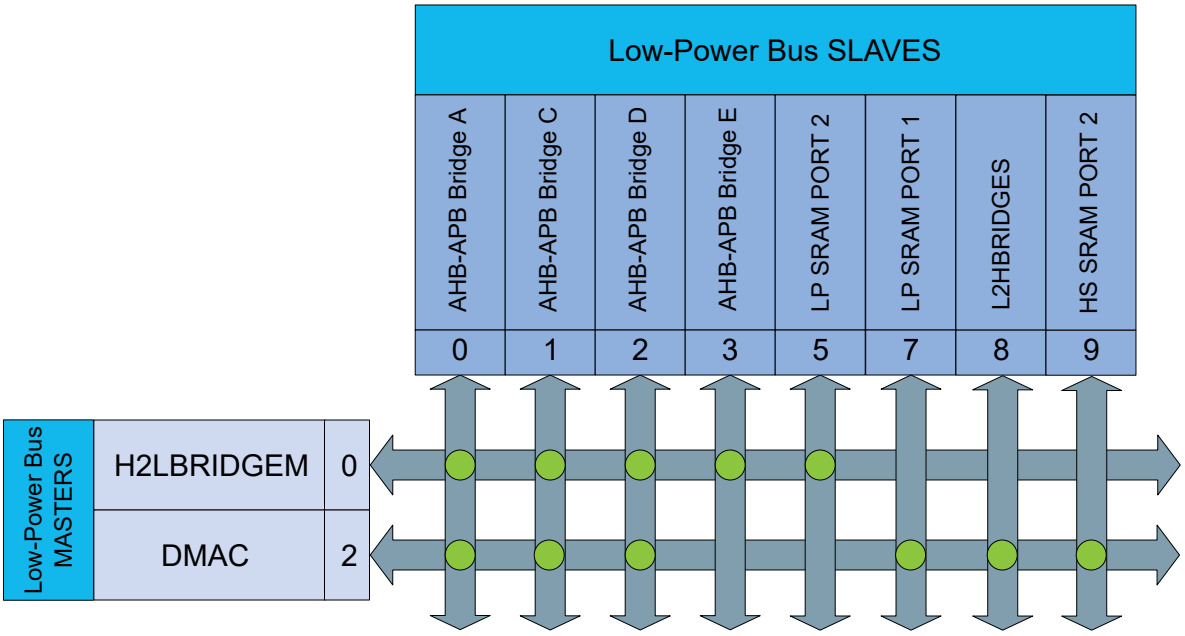


Table 7-4. High-Speed Bus Matrix Masters

High-Speed Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

.....continued	
High-Speed Bus Matrix Masters	**Master ID**
L2HBRIDGEM - Low-Power to High-Speed bus matrix AHB to AHB bridge	2

Table 7-5. High-Speed Bus Matrix Slaves

High-Speed Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
HS SRAM Port 0 - CM0+ Access	1
HS SRAM Port 1 - DSU Access	2
AHB-APB Bridge B	3
H2LBRIDGES - High-Speed to Low-Power bus matrix AHB to AHB bridge	4

Table 7-6. Low-Power Bus Matrix Masters

Low-Power Bus Matrix Masters	Master ID
H2LBRIDGEM - High-Speed to Low-Power bus matrix AHB to AHB bridge	0
DMAC - Direct Memory Access Controller - Data Access	2

Table 7-7. Low-Power Bus Matrix Slaves

Low-Power Bus Matrix Slaves	Slave ID
AHB-APB Bridge A	0
AHB-APB Bridge C	1
AHB-APB Bridge D	2
AHB-APB Bridge E	3
LP SRAM Port 2- H2LBRIDGEM access	5
LP SRAM Port 1- DMAC access	7
L2HBRIDGES - Low-Power to High-Speed bus matrix AHB to AHB bridge	8
HS SRAM Port 2- HMATRIXLP access	9

7.4.3 SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, priority levels can be assigned to the masters for different types of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM, the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration are shown in the following table.

Table 7-8. Quality of Service

Value	Name	Description
0x0	DISABLE	Background (no sensitive operation)
0x1	LOW	Sensitive Bandwidth
0x2	MEDIUM	Sensitive Latency
0x3	HIGH	Critical Latency

If a master is configured with QoS level DISABLE (0x0) or LOW (0x1) there will be a minimum latency of one cycle for the RAM access.

The priority order for concurrent accesses are decided by two factors. First, the QoS level for the master and second, a static priority given by the port ID. The lowest port ID has the highest static priority. See the tables below for details.

The MTB has a fixed QoS level HIGH (0x3).

The CPU QoS level can be written/read, using 32-bit access only, at address 0x41008114 bits [1:0]. Its reset value is 0x3.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

Table 7-9. HS SRAM Port Connections QoS

HS SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
MTB - Micro Trace Buffer	4	Direct	STATIC-3	0x3
USB - Universal Serial Bus	3	Direct	IP-QOSCTRL	0x3
HMATRIXLP - Low-Power Bus Matrix	2	Bus Matrix	0x44000934(1), bits[1:0]	0x2
DSU - Device Service Unit	1	Bus Matrix	0x4100201C(1)	0x2
CM0+ - Cortex M0+ Processor	0	Bus Matrix	0x41008114(1), bits[1:0]	0x3

Note:

1. Using 32-bit access only.

Table 7-10. LP SRAM Port Connections QoS

LP SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2

.....continued

LP SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
H2LBRIDGEM - HS to LP bus matrix AHB to AHB bridge	2	Bus Matrix	0x44000924(1), bits[1:0]	0x2
DMAC - Direct Memory Access Controller - Data Access	1	Bus Matrix	IP-QOSCTRL.DQOS	0x2

Note:

1. Using 32-bit access only.

8. Application Schematic Introduction

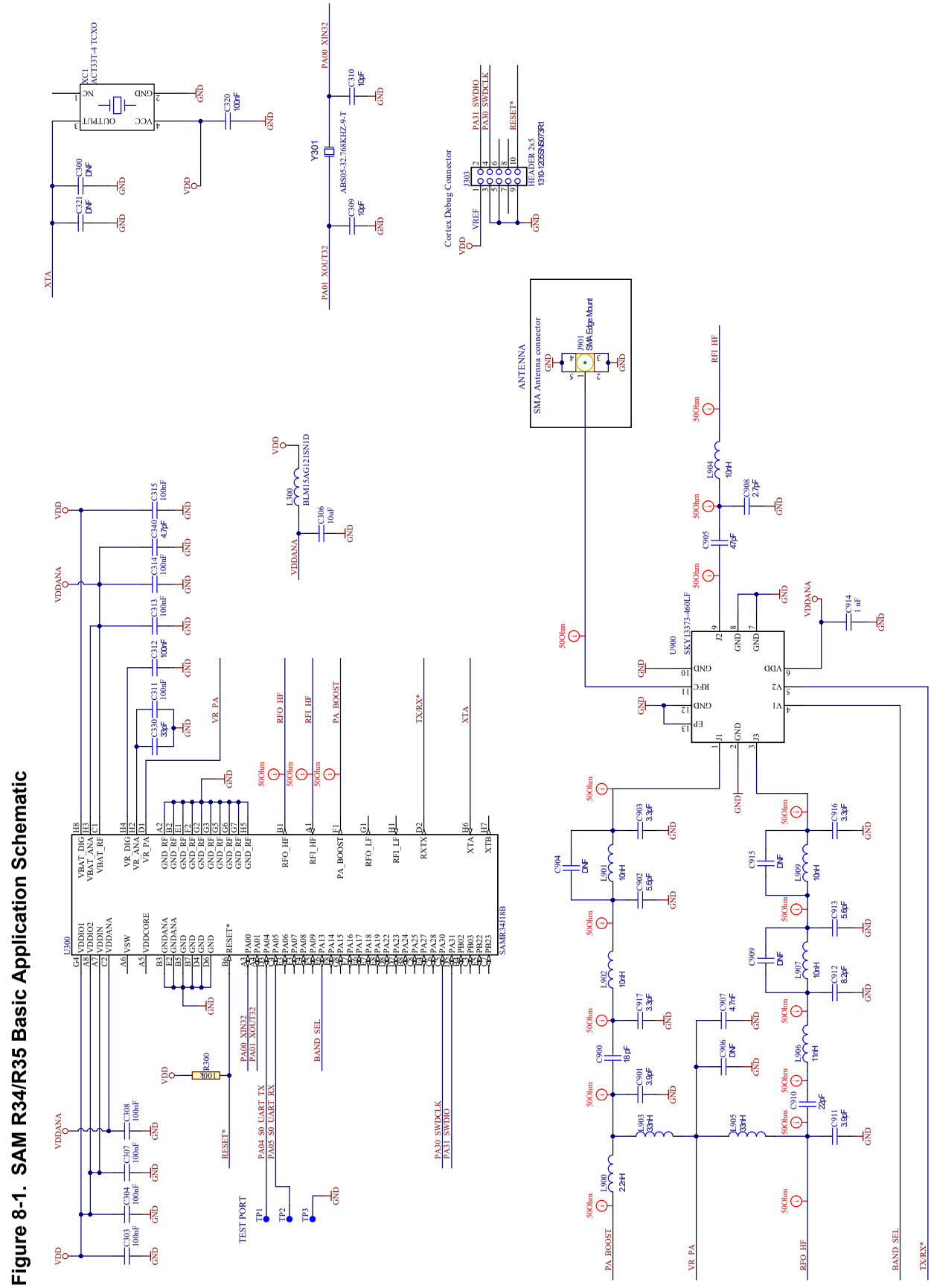
The SAM R34/R35 application schematic has to provide the environment for both integrated circuits inside the package. The microcontroller as well as the radio have integrated LDOs to provide the required core voltages. To achieve the full radio performance, the application layout has to take the noise decoupling in-between the analog radio part and the digital processor and signal processing power domains into account.

8.1 SAM R34/R35 Basic Application Schematic

The following application schematic shows the minimum circuit elements required for the SAM R34/R35 system. In this schematic, both the high-power PA_BOOST and high-efficiency RFO_HF transmitter configurations are populated. Some applications may require only one transmitter configuration.

For unused pins, the default state of the pins will give the lowest current leakage. Thus, there is no need to perform any configuration of the unused pins in order to lower the power consumption.

Figure 8-1. SAM R34/R35 Basic Application Schematic



8.2 SAM R34/R35 Bill of Materials

Table 8-1. Bill of Materials for SAM R34/R35

Sl. No.	Designator	Quantity	Value	Manufacturer	MPN	Description
1	C300, C321, C904, C906, C909, C915	6	DNF			Capacitor 0201 Do Not Fit
2	C303, C304, C307, C308, C311, C312, C313, C314, C315, C320	10	100 nF	KEMET Electronics Corporation	C0201C104K9PACTU	CAP CER 0.1 µF 6.3V 10% X5R 0201
3	C306	1	10 µF	Murata	GRM155R60J106ME15	Ceramic capacitor, SMD 0402, X5R, 6.3V, 20%
4	C309, C310	2	10 pF	TDK Corporation	C0603C0G1E100C	CAP CER 10 pF 25V C0G 0201
5	C330	1	33 pF	Johanson Technology Inc.	250R05L330GV4T	Ceramic capacitor, SMD 0201, C0G/NP0, 25V, +/-2%
6	C340	1	4.7 pF	Johanson Technology Inc.	250R05L4R7BV4T	Ceramic capacitor, SMD 0201, C0G/NP0, 25V, +/-0.1 pF
7	C900	1	18 pF	Murata	GRM0335C1H180GA01D	CAP CER 18 pF 50V C0G/NP0 0201 +/- 2%
8	C901, C911	2	3.9 pF	Murata	GRM0335C1H3R9BA01D	CAP CER 3.9 pF 50V C0G/NP0 0201, +/-0.1 pF
9	C902, C913	2	5.6 pF	Murata	GRM0335C1E5R6BA01D	CAP CER 5.6 pF 25V 0201
10	C903, C916, C917	3	3.3 pF	Johanson Technology Inc.	250R05L3R3BV4T	Ceramic capacitor, SMD 0201, C0G/NP0, 25V, +/-0.1 pF
11	C905	1	47 pF	Johanson Technology Inc.	250R05L470GV4T	Ceramic capacitor, SMD 0201, C0G/NP0, 25V, +/-2%
12	C907	1	4.7 nF	Murata	GRM033R71A472KA01D	Ceramic capacitor, SMD 0201, X7R, 10V, +/-10%
13	C908	1	2.7 pF	Murata	GJM0335C1E2R7BB01E	Ceramic capacitor, SMD 0201, C0G/NP0, 25V, +/-0.1 pF
14	C910	1	22 pF	Johanson Technology Inc.	250R05L220GV4T	Ceramic capacitor, SMD 0201, C0G/NP0, 25V, +/-2%
15	C912	1	8.2 pF	Johanson Technology Inc.	250R05L8R2CV4T	CAP CER 8.2 pF 25V NP0 0201 Å±0.25 pF
16	C914	1	1 nF	Murata	GRM033R71C102KA01D	Ceramic capacitor, SMD 0201, X7R, 16V, 0.1
17	J303	1	1310-1205SNS073R1	WCON Hardware Electronics Co., Ltd	1310-1205SNS073R1	2x5 pin header, 1.27 mm pitch, THM
18	J901	1	SMA Edge Mount	Cinch Connectivity Solutions Johnson	142-0771-831	Cinch Connectivity Solutions Johnson 50Ω, SMA Edge Mount Jack Receptacle

.....continued

Sl. No.	Designator	Quantity	Value	Manufacturer	MPN	Description
19	L300	1	BLM15AG121SN1D	Murata	BLM15AG121SN1D	Chip Bead, 120Ω@100MHz, 0.55A, 0402, Rdc 0.19Ω
20	L900	1	2.2 nH	Murata	LQW15AN2N2C10D	FIXED IND 2.2 nH 1A 27mΩ SMD, +-0.2 nH, 0201
21	L901, L902, L907, L909	4	10 nH	Murata	LQP03TN10NH02D	FIXED IND 10 nH 250MA 700mΩ, +-3%, 0201
22	L903, L905	2	33 nH	Johanson Technology Inc.	L-05B33NJV6T	RF Inductor, 33 nH, +/-5%, I_{rms}=0.2A, Q=5@100 MHz, DCR=2.3(Max), SMD, 0201
23	L904	1	10 nH	TDK Corporation	MLK0603L10NJT000	RF Inductor, 10 nH, +/-5%, I_{rms}=0.2A, Q=6@300 MHz, DCR=0.8(Max), SMD, 0201
24	L906	1	11 nH	Murata	LQP03HQ11NH02	FIXED IND 11 nH 300 mA 500mΩ 0201 +/-3%
25	R300	1	100 kΩ	Generic		Thick film resistor, SMD 0402, 1/16W, 1%
26	U300	1	SAMR34J18B			SAMR34 BGA-64
27	U900	1	SKY13373-460LF	Skyworks Solutions, Inc. Solutions Inc.		0.1-6.0 GHz SPT3 SWITCH
28	XC1	1	32 MHz TCXO	Taitien Electronics Co., LTD	TYETBCSANF-32.000000	32 MHz TCXO, 2.8 ~ 3.3V, Clipped sine wave 10kΩ/10 pF, 2 x 1.6 mm SMD
29	Y301	1	ABS05-32.768 kHz-9-T	Abracon® Corporation (LLC)		CRYSTAL 32.768 kHz 9 pF SMD ABS05

9. Transceiver Circuit Description

Note: The SAM R34/R35 incorporates a LoRa transceiver.

The integrated Sub-GHz transceiver supports LoRa technology spread spectrum modulation, combining ultra-long range communications and high interference immunity with extremely low current consumption.

Receive sensitivities of over -148 dBm can be achieved in narrowband modes, and -136 dBm in LoRaWAN protocol compliant modes, using a low cost crystal and bill of materials.

The transmit section offers two integrated power amplifiers. The highly efficient RFO port delivers up to +13 dBm for European regions and battery conservation. The high powered PA_BOOST port delivers a regulated output of +17 dBm with low EMI across the entire working voltage range or, up to +20 dBm of raw RF power with high-voltage supplies. This combination of high power and high RX sensitivity yields industry leading link budget, making it ideal for any application requiring long range low-data-rate communications. LoRa technology also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference robustness and energy consumption. For maximum flexibility, the user may decide on the spread spectrum modulation bandwidth (BW), spreading factor (SF), and forward error correction rate (CR). Another benefit of the spread spectrum modulation is that each spreading factor is orthogonal, thus multiple transmitted signals can occupy the same channel without interfering.

The SAM R34/R35 also supports high performance (G)FSK, (G)MSK, and OOK modes for systems including WMBus and IEEE802.15.4g.

This transceiver offers bandwidth options ranging from 7.8 kHz to 500 kHz with spreading factors ranging from 6 to 12, and covering all available frequency bands from 137 to 1020 MHz.

9.1 Transceiver Pin Description

Table 9-1. Description of Transceiver Signals Available Outside the Package

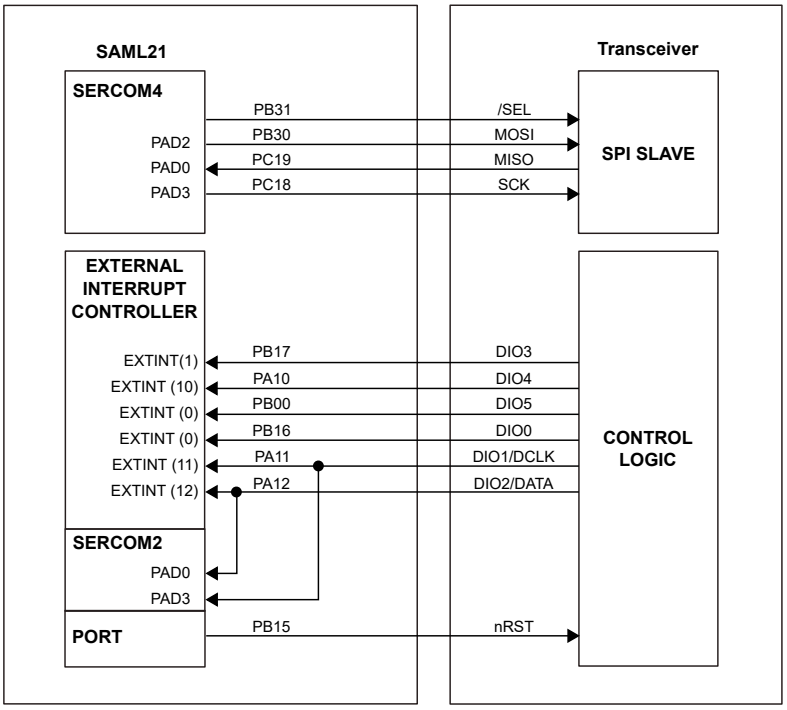
Name	Type	Description
RFI_LF	I	RF Input for Bands 2 and 3
RFO_LF	O	RF Output for Bands 2 and 3
VR_ANA	Supply	Regulated Supply Voltage for Analog Circuitry
VBAT_ANA	Supply	Supply Voltage for Analog Circuitry
VR_DIG	Supply	Regulated Supply Voltage for Digital Blocks
VBAT_DIG	Supply	Supply Voltage for Digital Blocks
XTA	I/O	XTAL Connection or TCXO Input
XTB	I/O	XTAL Connection
RXTX	O	RX/TX Switch Control: High in TX
RFI_HF	I	RF Input for Band 1
RFO_HF	O	RF Output for Band 1
VBAT_RF	Supply	Supply Voltage for RF Blocks

.....continued		
Name	**Type**	**Description**
VR_PA	Supply	Restricted Supply for the PA
PA_BOOST	O	Optional High Power PA Output, All Frequency Bands

10. Microcontroller Interface

This section describes the transceiver to microcontroller interface. The interface is comprised of a slave SPI and additional control signals. This interface is connected to a SAM L21 master interface as shown below.

Figure 10-1. Microcontroller to Transceiver Interface



The SPI is used for register, Frame Buffer, and SRAM access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller. The table below introduces the radio transceiver I/O signals and their functionalities.

Table 10-1. Microcontroller Interface Signal Description

Signal	Description
/SEL	SPI select signal, active-low
MOSI	SPI data (master output slave input) signal
MISO	SPI data (master input slave output) signal
SCLK	SPI clock signal
NRESET	Transceiver Reset signal, Active-low
DIO0	Digital I/O, software configured
DIO1	Digital I/O, software configured
DIO2	Digital I/O, software configured
DIO3	Digital I/O, software configured
DIO4	Digital I/O, software configured

.....continued	
Signal	**Description**
DIO5	Digital I/O, software configured

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Stresses beyond those listed in following table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11-1. Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Units
V_{DD}	Power supply voltage	0	3.8	V
V_{PIN}	Pin voltage with respect to GND and V_{DD} $V_{DD\ MAX}$=3.6V	GND-0.6V	VDD+0.6V	V
P_{RF}	Input RF level	-	+10	dBm
$T_{storage}$	Storage temperature	-50	150	°C
T_{LEAD}	T=10s (soldering profile compliant with IPC/JEDEC J STD 020B)	-	260	°C

⚠ CAUTION This device is sensitive to electrostatic discharges (ESD). Improper handling may lead to permanent performance degradation or malfunctioning. Handle the device following best practice ESD protection rules: Be aware that the human body can accumulate charges large enough to impair functionality or destroy the device.

11.2 General Operating Conditions

The device must operate within the ratings listed in the following table in order for all other electrical characteristics and typical characteristics of the device to be valid.

For unused pins, the default state of the pins gives the lowest current leakage. Thus, specific configuration is not required for the unused pins in order to lower the power consumption.

Table 11-2. General Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Units
V_{DDIN}	Power supply voltage	1.8	3.3	3.63	V
V_{DDIO}	IO Supply Voltage	1.8	3.3	3.63	V
V_{DDANA}	Analog supply voltage	1.8	3.3	3.63	V
T_A	Temperature range	-40	25	85	°C
T_J	Junction temperature	-	-	100	°C

⚠ CAUTION In debugger Cold-Plugging mode, NVM erase operations are not protected by the BOD33 and BOD12. NVM erase operation at supply voltages below specified minimum can cause corruption of NVM areas that are mandatory for correct device behavior.

11.3 Performance Characteristics

The following data shows SAM R34/R35 performance as a combined system including both the SAML21 and the transceiver under the following conditions:

- Modulation = LoRa
- VCC = 3.3 VDC
- Temperature = 25°C
- F_{RF_XTA} = 32.000000 MHz +/- 1 ppm (TCXO)
- DFLL = 48 MHz
- BW = 125 kHz
- SF = 12
- EC = 4/6
- PER = 1%
- CRC = ENABLED
- Payload = 64 Bytes
- Preamble = 12 symbols
- Matched Impedance

Estimates for ACTIVE state of the SAML21 are derived using the CoreMark benchmarking algorithm, a 48 MHz DFLL clock and 3.3 VDC supply. These are intended to show a conservative estimate of power consumption. Results are related to CPU activity, clock speed and temperature and may be improved with optimization.

11.3.1 Method of Derivation

Combined specifications in this data sheet are derived from the published data sheets of the components. See Reference Documents [1] and [5]. For example, the *Line Current in TX Mode* entry for RFO_HF +13 dBm is 32.5 mA. This is calculated using the IDDT_L current in *LoRa Receiver Specification Table* 10 of [5] and the *Active Current Consumption Table* 46-7 of [1] for the operational conditions shown below.

Table 11-3. TRX TX Current Derivation

Condition	Value	Unit
Bandwidth	125	kHz
Carrier Frequency	868	MHz
CRC	ENABLED	
Error Correction Code	4/6	
Fxosc	32	MHz
Impedances	MATCHED	
Packet Error rate	1	%

.....continued		
Condition	**Value**	**Unit**
Payload Length	64	Bytes
Preamble Length	12	Symbols
RF Output Power	+13	dBm
RF Port	RFO_HF	
Spreading Factor	12	
Supply Voltage	3.3	VDC
Temperature	25	Celsius
IDDT_L	28	mA (TYP)

Table 11-4. TRX RX Current Derivation

Condition	Value	Unit
Bandwidth	125	kHz
Carrier Frequency	868	MHz
CRC	ENABLED	
Error Correction Code	4/6	
Fxosc	32	MHz
Impedances	MATCHED	
LNA Boost	OFF	
Packet Error rate	1	%
Payload Length	64	Bytes
Preamble Length	12	Symbols
RF Port	RFI_HF	
Spreading Factor	12	
Supply Voltage	3.3	VDC
Temperature	25	Celsius
IDDR_L	10.3	mA (TYP)

Table 11-5. CPU Current Derivation

CPU Contribution		
Conditions	**Value**	**Unit**
Clock	DFLL 48	MHz
Benchmark Algorithm	COREMARK	-

.....continued		
CPU Contribution		
Conditions	**Value**	**Unit**
Current/MHz	95	uA/MHz
Mode	ACTIVE	-
PL	PL2	-
Regulator	LDO	-
Supply Voltage (VDC)	3.3	V
I_CPU	4.5	mA (TYP)

Using the contributions above the total combined current consumption is calculated as follows:

- I_TOTAL_{TX} = IDDT_L + I_CPU = 28 + 4.5 mA = 32.5 mA
- I_TOTAL_{RX} = IDDR_L + I_CPU = 10.3 + 4.5 mA = 14.8 mA

11.3.2 Line Current in TX Mode

Table 11-6. Line Current in Tx Mode

Output Mode	I_CPU	IDDT_L	I_TOTAL	Unit
RFO_LF +13 dBm	4.5	28	32.5	mA (TYP)
PA_BOOST +17 dBm	4.5	90	94.5	mA (TYP)

11.3.3 Line Current in Receive Mode

Table 11-7. Line Current in Receive Mode

Frequency MHz	I_CPU	IDDR_L	I_TOTAL	Unit
915	4.5	10.3	14.8	mA (TYP)
868	4.5	10.3	14.8	mA (TYP)
433	4.5	11.5	15.8	mA (TYP)

11.3.4 Standby Current

Table 11-8. Standby Current Table

State	CPU Mode	I_CPU	TRX Mode	IDDSL	TOTAL	Units
IDLE	ACTIVE	4.5	SLEEP	0.0002	4.5	mA
STANDBY	STANDBY	1.2	SLEEP	0.2	1.4	uA
SLEEP	SLEEP	590	SLEEP	200	790	nA
DO NOT USE	OFF	-	ALL	-		

11.3.5 Transmitter Output Power

Table 11-9. Transmitter Output Power in LoRa Mode

Frequency (MHz)	Output Port	Typical Output Power (dBm)
915	PA_BOOST	17
915	RFO_HF	13
868	PA_BOOST	17
868	RFO_HF	13
433	PA_BOOST	17
433	RFO_LF	13

11.3.6 Transmitter Phase Noise

Table 11-10. Phase Noise

Offset	Phase Noise (dBc/Hz)
10k	-103
50k	-103
400k	-115
1M	-122

11.3.7 Receiver Sensitivity

Table 11-11. Receiver Sensitivity in LoRa Mode

Frequency (MHz)	BW (kHz)	SF	Sensitivity	Unit
915	125	11	-133	dBm
868	125	11	-133	dBm
433	7.8	12	-148	dBm

Note: The above results are obtained with TCXO.

11.3.8 Blocking

Table 11-12. Blocking

Frequency (MHz)	1 MHz	2 MHz	10 MHz
915	71	76	84
868	71	76	84
433	71	72	78

11.3.9 Transmitter High Power Operation

To operate in the +20 dBm High-Power mode high voltage must be supplied to VDDANA. For some regions, additional EMI filtering may be needed at high power.

Table 11-13. High-Power Operational Parameters

Parameter	Value
RF Output Power	+20 dBm MAX
Output Port	PA_BOOST F1
VDDANA (Min.)	2.4 VDC
VDDANA (Max.)	3.6 VDC
Typical Line Current	120 mA
Max. Duty Cycle	1% MAX
VSWR	3:1 MAX

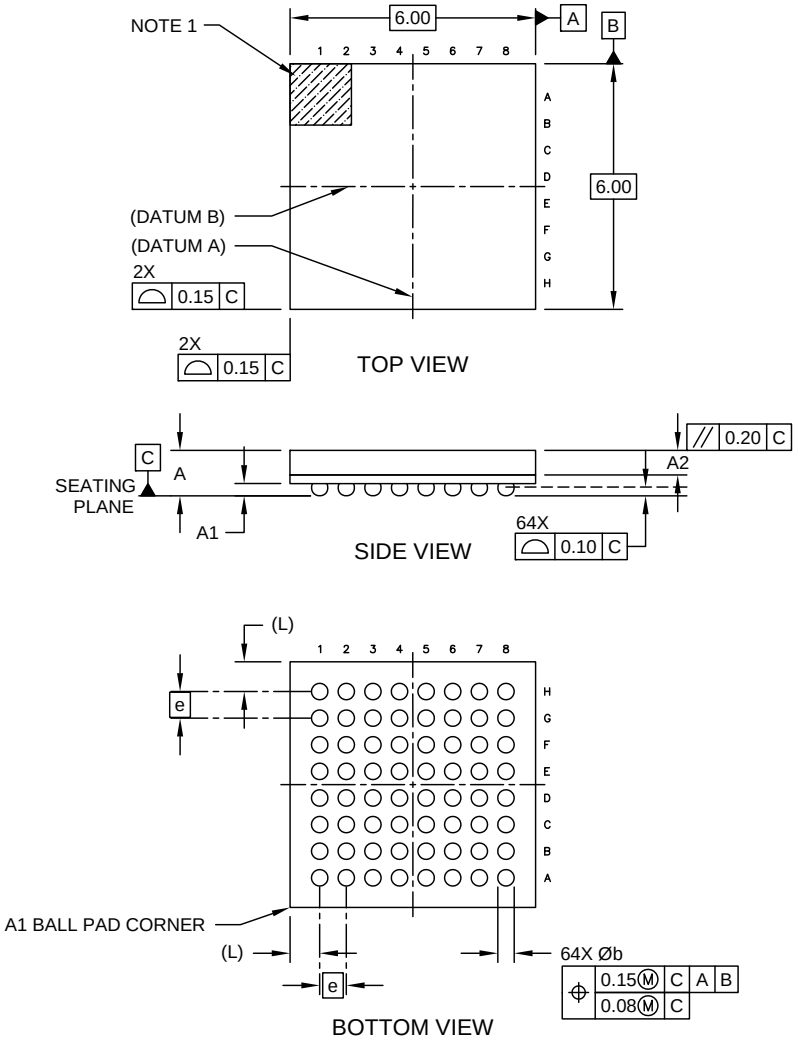
12. SAM R34/R35 Package Information

12.1 Package Drawings

Figure 12-1. Package Drawings of SAM R34/R35

64-Lead Thin, Fine Pitch Ball Grid Array Package (7JX) - 6x6 mm Body [TFBGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-443A Sheet 1 of 2

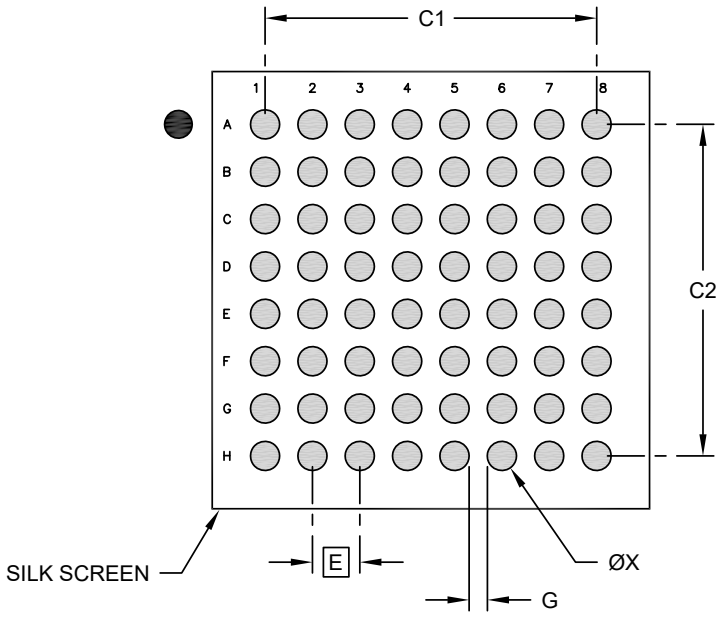
12.2 SAM R34/R35 Land Pattern

PCB layout pattern for SAM R34/R35 64-Pin BGA is shown below.

Figure 12-2. SAM R34/R35 Land Pattern

64-Lead Thin, Fine Pitch Ball Grid Array Package (7JX) - 6x6 mm Body [TFBGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		4.55	
Contact Pad Spacing	C2		4.55	
Contact Pad Diameter (X64)	X			0.40
Space Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2433A

13. Best Practices for Designers

13.1 Introduction

This chapter outlines best practices for design and review of SAM R34/R35 designs. This chapter illustrates the recommended power supply connections, how to connect external analog references, programmer, debugger, oscillator, and crystal.

13.1.1 Electromagnetic Compliance

Best practices for RF designs are beyond the scope of this document. There are several good application notes, different techniques and different opinions. Furthermore, results vary because of system factors like enclosures, PCBA design, incidental resonant structures, co-existence with other RF energy sources, regulatory and regional requirements. The designer must balance these factors and verify with laboratory measurements. Testing emissions early in the design cycle is strongly encouraged. Typical best practices include 4-layer PCB construction, generous ground planes and stitching vias for noise suppression and counterpoise, separation of RF and digital ground-domains, controlled-impedance transmission lines and passive components rated for radio frequency operation. Baseband techniques include placing decoupling capacitors very close to the power pins and an RC-filter on the RESET pin; in addition, a pull-up resistor on the SWCLK pin is critical for reliable operations.

13.2 Power Supply

The SAM R34/R35 supports a single or dual power supply from 1.8 to 3.6 VDC. The same voltage must be applied to both VDDIN and VDDANA.

The internal voltage regulator has four different modes:

- Linear mode: this mode does not require any external inductor. This is the default mode when CPU and peripherals are running
- Low Power (LP) mode: This is the default mode used when the chip is in Standby mode
- Shutdown mode: When the chip is in Backup mode, the internal regulator is turned off

Selecting between Switching mode and Linear mode can be done by software on the fly, but the power supply must be designed according to which mode is to be used.

13.2.1 Power Supply Connections

The following figures show the recommended power supply connections for Switched/Linear mode, Linear mode only and with battery backup.

Figure 13-1. Power Supply Connection for Switching/Linear Mode

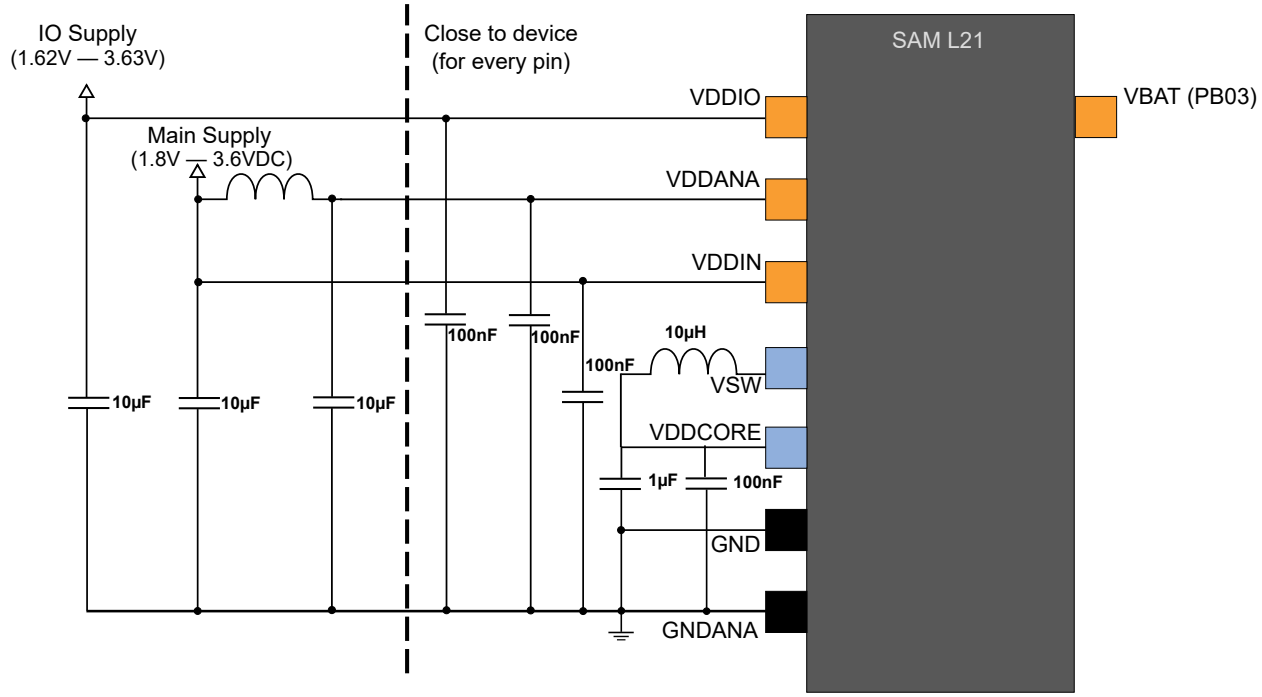


Figure 13-2. Power Supply Connection for Linear Mode Only

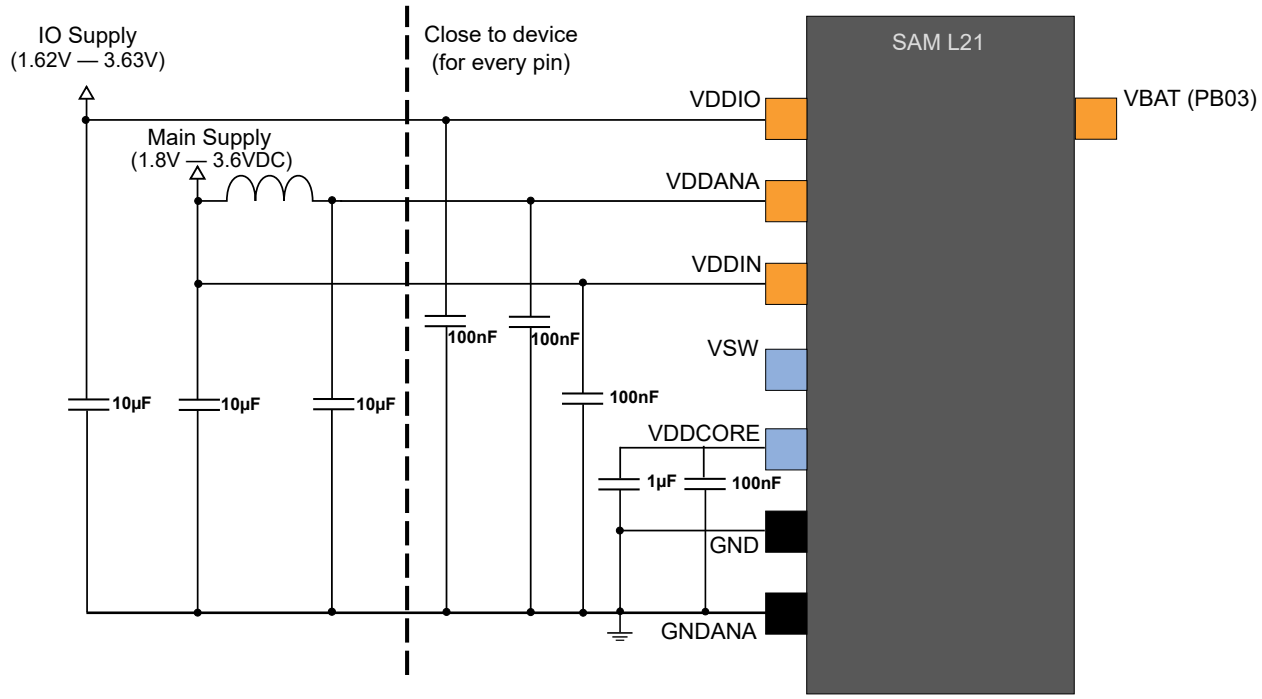


Figure 13-3. Power Supply Connection for Battery Backup

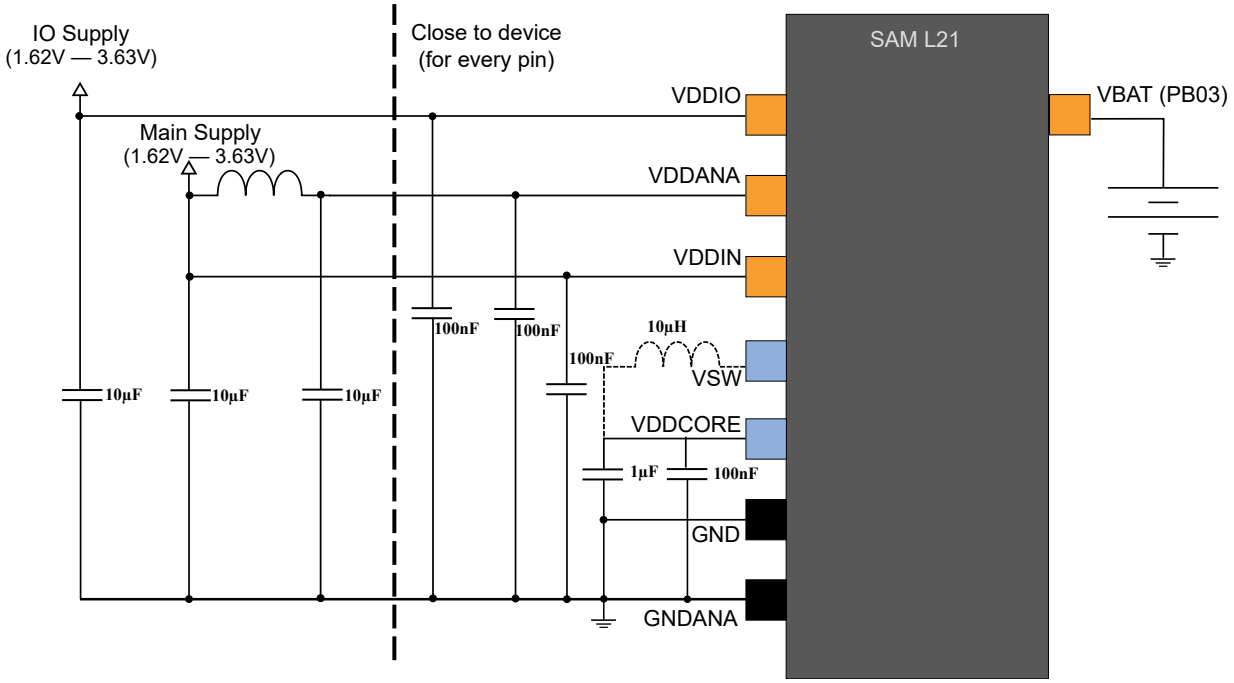


Table 13-1. Power Supply Connections, V_{DDCORE} or V_{SW} From Internal Regulator

Signal Name	Recommended Pin Connection	Description
V_{DDIO}	1.8 to 3.6 VDC Decoupling/filtering capacitors 100nF(1)(2) and 10µF(1) Decoupling/filtering inductor 10µH(1)(3)	Digital supply voltage
V_{DDANA}	1.8 to 3.6 VDC Decoupling/filtering capacitors 100nF(1)(2) and 10µF(1) Ferrite bead(4) prevents the V_{DD} noise interfering with V_{DDANA}	Analog supply voltage
V_{DDIN}	1.8 to 3.6 VDC Decoupling/filtering capacitors 100nF(1)(2) and 10µF(1) Decoupling/filtering inductor 10µH(1)(3)	Digital supply voltage
V_{BAT}	1.8 to 3.5 VDC when connected	External battery supply input
V_{DDCORE}	0.9V to 1.2V typical Decoupling/filtering capacitors 100nF(1)(2) and 1µF(1)	Linear Regulator mode: Core supply voltage output/ external decoupling pin Switched Regulator mode: Core supply voltage input, must be connected to V_{SW} via inductor

.....continued		
Signal Name	**Recommended Pin Connection**	**Description**
V_{SW}	Switching Regulator mode: 10 µH inductor with saturation current above 150mA and DCR<1Ω Linear Regulator mode: Not connected	On-Chip Switching mode regulator output
GND		Ground
GND_{ANA}		Ground for the analog power domain

1. These values are only given as a typical example.

2. Decoupling capacitors should be placed close to the device for each supply pin pair in the signal group, low ESR capacitors should be used for better decoupling.

3. An inductor should be added between the external power and the V_{DD} for power filtering.

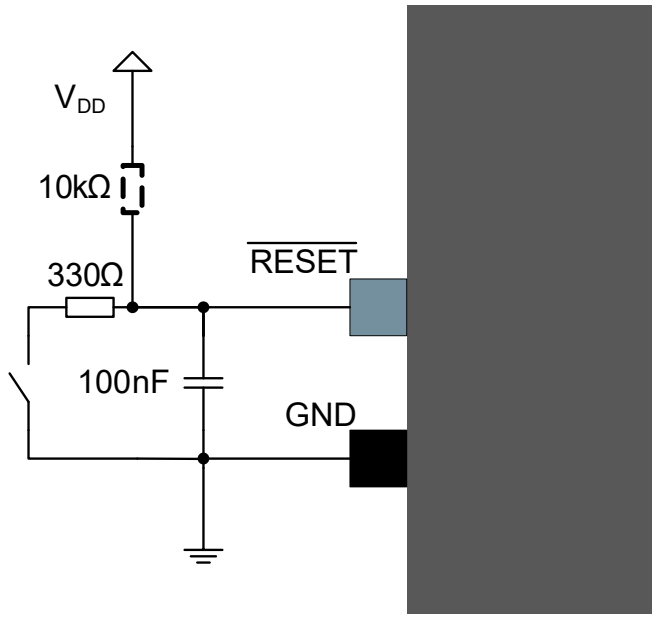
4. A ferrite bead has better filtering performance compared to standard inductor at high frequencies. A ferrite bead can be added between the main power supply (V_{DD}) and V_{DDANA} to prevent digital noise from entering the analog power domain. The bead should provide enough impedance (e.g. 50Ω at 20MHz and 220Ω at 100MHz) to separate the digital and analog power domains. Make sure to select a ferrite bead designed for filtering applications with a low DC resistance to avoid a large voltage drop across the ferrite bead.

13.3 External Reset Circuit

The external Reset circuit is connected to the $\overline{RESET}$ pin when the external Reset function is used. The circuit is not necessary when the $\overline{RESET}$ pin is not driven LOW externally by the application circuitry.

The reset switch can also be removed, if a manual reset is not desired. The $\overline{RESET}$ pin itself has an internal pull-up resistor, hence it is optional to add any external pull-up resistor.

Figure 13-4. External Reset Circuit Schematic



A pull-up resistor makes sure that the reset does not go low and unintentionally causing a device reset. An additional resistor has been added in series with the switch to safely discharge the filtering capacitor, i.e. preventing a current surge when shorting the filtering capacitor which again can cause a noise spike that can have a negative effect on the system.

Table 13-2. Reset Circuit Connections

Signal Name	Recommended Pin Connection	Description
$\overline{\text{RESET}}$	Reset low level threshold voltage V_{DDIO} = 1.6V - 2.0V: Below 0.33 * V_{DDIO} V_{DDIO} = 2.7V - 3.6V: Below 0.36 * V_{DDIO} Decoupling/filter capacitor 100nF(1) Pull-up resistor 10kΩ(1)(2) Resistor in series with the switch 330Ω(1)	Reset pin

1. These values are only given as a typical example.

2. The SAM R34/R35 features an internal pull-up resistor on the $\overline{\text{RESET}}$ pin, hence an external pull up is optional.

13.4 Unused or Unconnected Pins

For unused pins, the default state of the pins will give the lowest current leakage. Thus, there is no need to do any configuration of the unused pins in order to lower the power consumption.

13.5 Clocks and Crystal Oscillators

The SAM R34/R35 can be run from internal or external clock sources, or a mix of internal and external sources. An example of usage can be to use the internal 16MHz oscillator as source for the system clock and an external 32.768kHz watch crystal as clock source for the Real-Time counter (RTC).

13.5.1 External Clock Source

Figure 13-5. External Clock Source Schematic

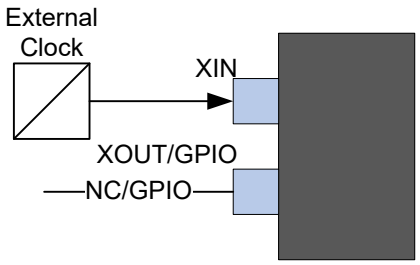
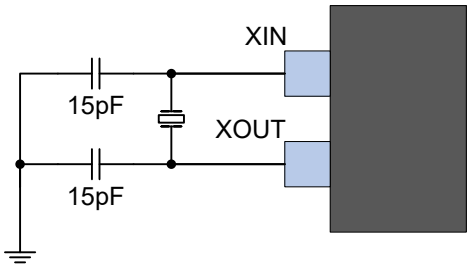


Table 13-3. External Clock Source Connections

Signal Name	Recommended Pin Connection	Description
XIN	XIN is used as input for an external clock signal	Input for inverting oscillator pin
XOUT/GPIO	Can be left unconnected or used as normal GPIO	NC/GPIO

13.5.2 Crystal Oscillator

Figure 13-6. Crystal Oscillator Schematic



The crystal should be located as close to the device as possible. Long signal lines may cause too high of a load to operate the crystal, and cause crosstalk to other parts of the system.

Table 13-4. Crystal Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN	Load capacitor 15pF(1)(2)	External crystal between 0.4 to 32MHz
XOUT	Load capacitor 15pF(1)(2)	

1. These values are only given as a typical example.

2. The capacitors should be placed close to the device for each supply pin pair in the signal group.

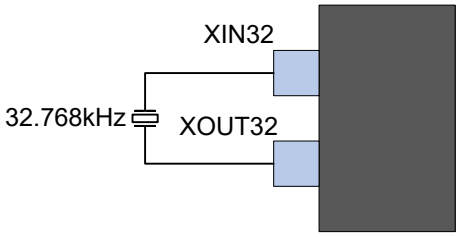
13.5.3 External Real Time Oscillator

The low frequency crystal oscillator is optimized for use with a 32.768kHz watch crystal. When selecting crystals, load capacitance and the crystal's Equivalent Series Resistance (ESR) must be taken into consideration. Both values are specified by the crystal vendor.

SAM R34/R35 oscillator is optimized for very low power consumption, hence close attention should be made when selecting crystals.

The typical parasitic load capacitance values are available in the Electrical Characteristics section. This capacitance and PCB capacitance can allow using a crystal inferior to 12.5pF load capacitance without external capacitors as shown in Figure 13-7.

Figure 13-7. External Real Time Oscillator without Load Capacitor



To improve accuracy and Safety Factor, the crystal datasheet can recommend adding external capacitors as shown in Figure 13-8.

To find suitable load capacitance for a 32.768kHz crystal, consult the crystal datasheet.

Figure 13-8. External Real Time Oscillator with Load Capacitor

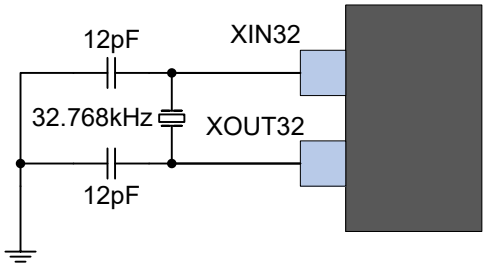


Table 13-5. External Real Time Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN32	Load capacitor 22pF(1)(2)	Timer oscillator input
XOUT32	Load capacitor 22pF(1)(2)	Timer oscillator output

1. These values are only given as typical examples.

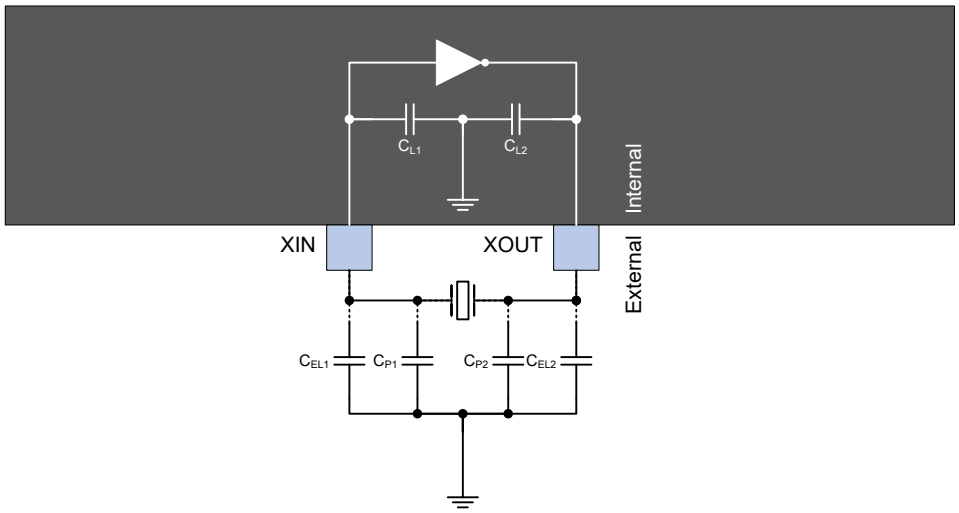
2. The capacitors should be placed close to the device for each supply pin pair in the signal group.

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

13.5.4 Calculating the Correct Crystal Decoupling Capacitor

The model shown in Figure 13-9 can be used to calculate correct load capacitor for a given crystal. This model includes internal capacitors C_{Ln}, external parasitic capacitance C_{ELn} and external load capacitance C_{Pn}.

Figure 13-9. Crystal Circuit With Internal, External and Parasitic Capacitance



Using this model the total capacitive load for the crystal can be calculated as shown in the equation below:

$$\sum C_{\text{tot}} = \frac{(C_{L1} + C_{P1} + C_{\text{EL1}})(C_{L2} + C_{P2} + C_{\text{EL2}})}{C_{L1} + C_{P1} + C_{\text{EL1}} + C_{L2} + C_{P2} + C_{\text{EL2}}}$$

where C_{tot} is the total load capacitance seen by the crystal. This value should be equal to the load capacitance value found in the crystal manufacturer datasheet.

The parasitic capacitance C_{ELn} can in most applications be disregarded as these are usually very small. If accounted for, these values are dependent on the PCB material and PCB layout.

For some crystal the internal capacitive load provided by the device itself can be enough. To calculate the total load capacitance in this case. C_{ELn} and C_{Pn} are both zero, $C_{L1} = C_{L2} = C_L$, and the equation reduces to the following:

$$\sum C_{\text{tot}} = \frac{C_L}{2}$$

See the related links for equivalent internal pin capacitance values.

13.6 Programming and Debug Ports

For programming and/or debugging the SAM R34/R35, the device should be connected using the Serial Wire Debug, SWD, interface. Currently the SWD interface is supported by several Microchip and third party programmers and debuggers, like the Atmel-ICE, SAM-ICE™ or SAM R34/R35 Xplained Pro (SAM R34/R35 evaluation kit) Embedded Debugger.

Refer to the Atmel-ICE, SAM-ICE or SAM R34/R35 Xplained Pro user guides for details on debugging and programming connections and options. For connecting to any other programming or debugging tool, refer to that specific programmer or debugger's user guide.

The SAM R34/R35 Xplained Pro evaluation board supports programming and debugging through the onboard embedded debugger, so no external programmer or debugger is needed.

Note: A pull-up resistor on the SWCLK pin is critical for reliable operation. Refer to related link for more information.

Figure 13-10. SWCLK Circuit Connections

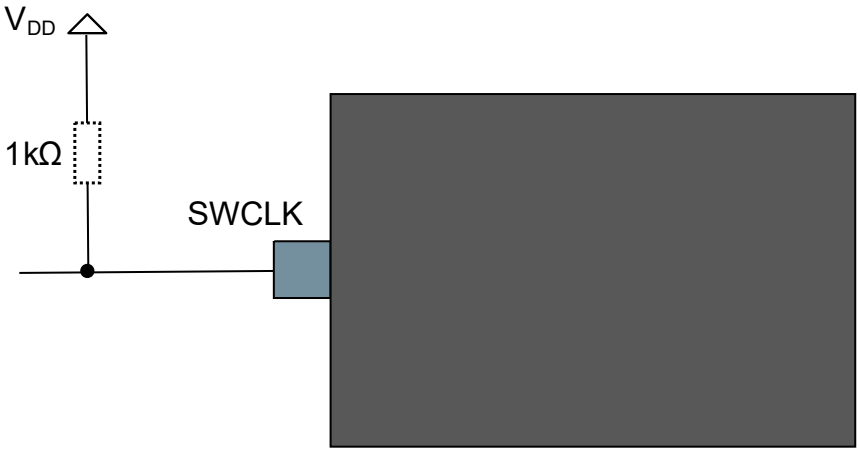


Table 13-6. SWCLK Circuit Connections

Pin Name	Description	Recommended Pin Connection
SWCLK	Serial wire clock pin	Pull-up resistor 1kΩ

13.6.1 Cortex Debug Connector (10-pin)

For debuggers and/or programmers that support the Cortex Debug Connector (10-pin) interface, the signals should be connected as shown in following figure. The signal details are described in the following table.

Figure 13-11. Cortex Debug Connector (10-pin)

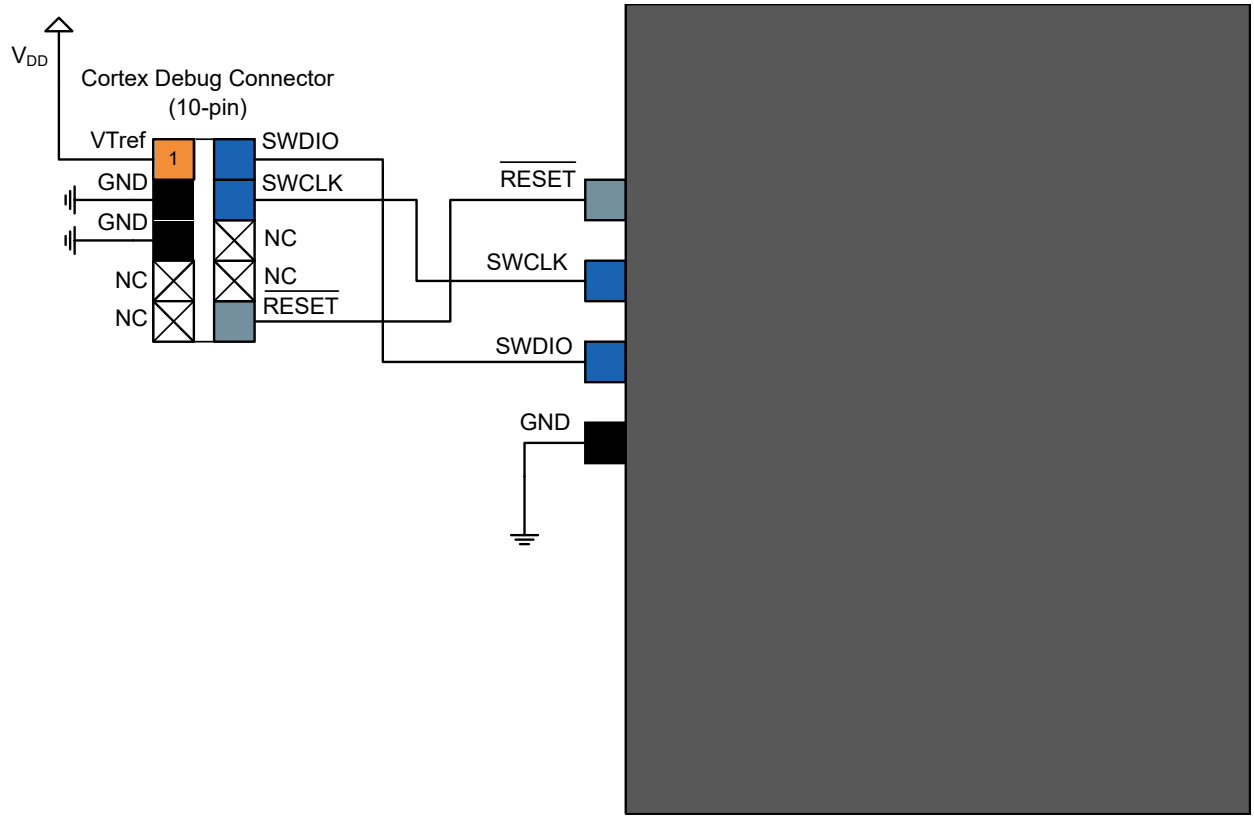


Table 13-7. Cortex Debug Connector (10-pin)

Header Signal Name	Description
SWCLK	Serial wire clock pin
SWDIO	Serial wire bidirectional data pin
$\overline{\text{RESET}}$	Target device reset pin, active low
VTref	Target voltage sense, should be connected to the device V_{DD}
GND	Ground

13.6.2 10-pin JTAGICE3 Compatible Serial Wire Debug Interface

The JTAGICE3 debugger and programmer does not support the Cortex Debug Connector (10-pin) directly, hence a special pinout is needed to directly connect the SAM R34/R35 to the JTAGICE3, alternatively one can use the JTAGICE3 squid cable and manually match the signals between the JTAGICE3 and SAM R34/R35. Figure 13-12 describes how to connect a 10-pin header that support connecting the JTAGICE3 directly to the SAM R34/R35 without the need for a squid cable. This can also be used for the Atmel-ICE AVR connector port.

The JTAGICE3 squid cable or the JTACICE3 50mil cable can be used to connect the JTAGICE3 programmer and debugger to the SAM R34/R35. Figure 13-12 illustrates the correct pinout for the JTAGICE3 50 mil, and details are given in Table 13-8.

Figure 13-12. 10-pin JTAGICE3 Compatible Serial Wire Debug Interface

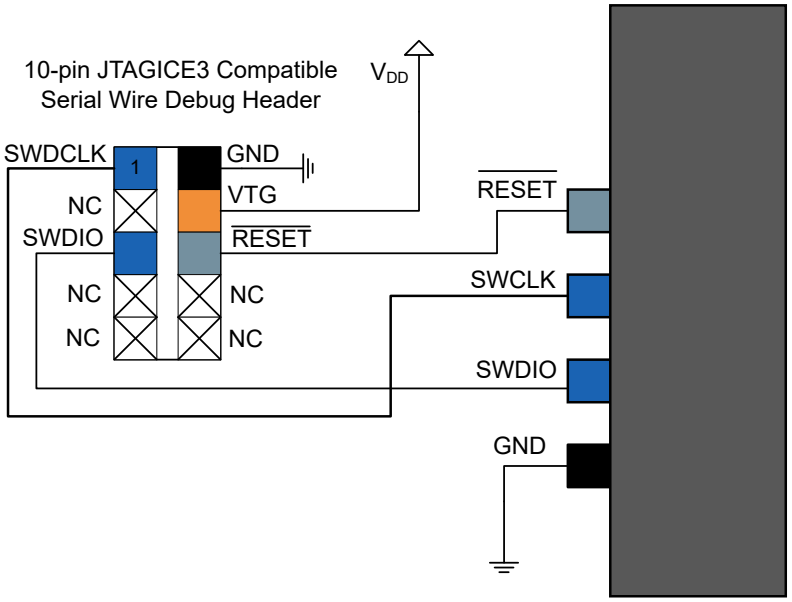


Table 13-8. 10-pin JTAGICE3 Compatible Serial Wire Debug Interface

Header Signal Name	Description
SWDCLK	Serial wire clock pin
SWDIO	Serial wire bidirectional data pin
$\overline{\text{RESET}}$	Target device reset pin, active low
VTG	Target voltage sense, should be connected to the device V_{DD}
GND	Ground

13.6.3 20-pin IDC JTAG Connector

For debuggers and/or programmers that support the 20-pin IDC JTAG Connector, e.g. the SAM-ICE, the signals should be connected as shown in Figure 13-13 with details described in Table 13-9.

Figure 13-13. 20-pin IDC JTAG Connector

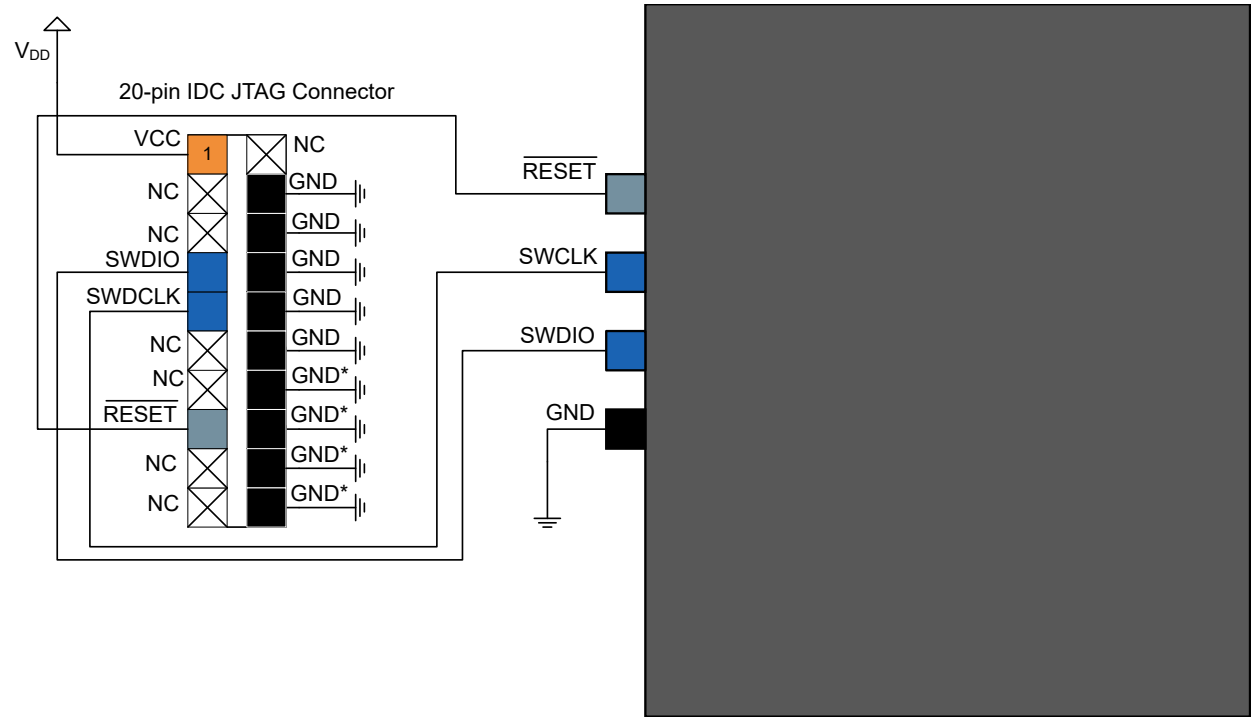


Table 13-9. 20-pin IDC JTAG Connector

Header Signal Name	Description
SWDCLK	Serial wire clock pin
SWDIO	Serial wire bidirectional data pin
$\overline{\text{RESET}}$	Target device reset pin, active low
VCC	Target voltage sense, should be connected to the device V_{DD}
GND	Ground
GND*	These pins are reserved for firmware extension purposes. They can be left unconnected or connected to GND in normal debug environment. They are not essential for SWD in general.

14. Reference Documentation

The following documents can be used for further study:

1. SAM L21 Family Data Sheet (60001477A)
2. Atmel AVR2067: Crystal Characterization for AVR RF Application Note (42068A)
3. Atmel AT02865: RF Layout with Microstrip Application Note (42131B)
4. Atmel AT11309: Advanced RF Layout with Altium Application Note (42478A)
5. Semtech SX1276 Transceiver: Semtech SX1276/77/78/79 Data Sheet rev 5

15. Document Revision History

Table 15-1. Document Revision History

Revision	Date	Section	Description
B	10/2018	11.3 Performance Characteristics	Updated with new content
		• 11.3.1 Method of Derivation • 4.3 Peripheral Key Table	Added new sections
		• Table 11-6 • Table 11-7 • Table 11-8 • Table 11-11	Updated tables
		14. Reference Documentation	Updated documents list
A	04/2018	Document	Initial release

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