SMART ARM-based Microcontroller

SAM D21E / SAM D21G /SAM D21J

DATASHEET SUMMARY

Introduction

Atmel® | SMART™ SAM D21 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D21 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer (MTB)
- Memories
  - 32/64/128/256KB in-system self-programmable Flash
  - 4/8/16/32KB SRAM Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals

This is a summary document. A complete document is available on our Web site at www.atmel.com

- Peripherals
  - 12-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Up to five 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with two compare/capture channels
    - One 8-bit TC with two compare/capture channels
    - One 32-bit TC with two compare/capture channels, by using two TCs
  - Three 24-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
    - Embedded host and device function
    - Eight endpoints
  - Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I2C up to 3.4MHz
    - SPI
    - LIN slave
  - One two-channel Inter-IC Sound (I^2S) interface
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 256-Channel capacitive touch and proximity sensing
- I/O
  - Up to 52 programmable I/O pins
- Drop in compatible with SAM D20
- Packages
  - 64-pin TQFP, QFN, UFBGA
  - 48-pin TQFP, QFN, WLCSP
  - 32-pin TQFP, QFN, WLCSP
- Operating Voltage
  - 1.62V – 3.63V

Table of Contents

1. Description

The Atmel® | SMART™ SAM D21 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D21 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D21 devices provide the following features: In-system programmable Flash, twelve-channel direct memory access (DMA) controller, 12 channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three 24-bit Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. The series provide one full-speed USB 2.0 embedded host and device interface; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 3.4MHz, SMBus, PMBus, and LIN slave; two-channel I^2S interface; up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D21 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

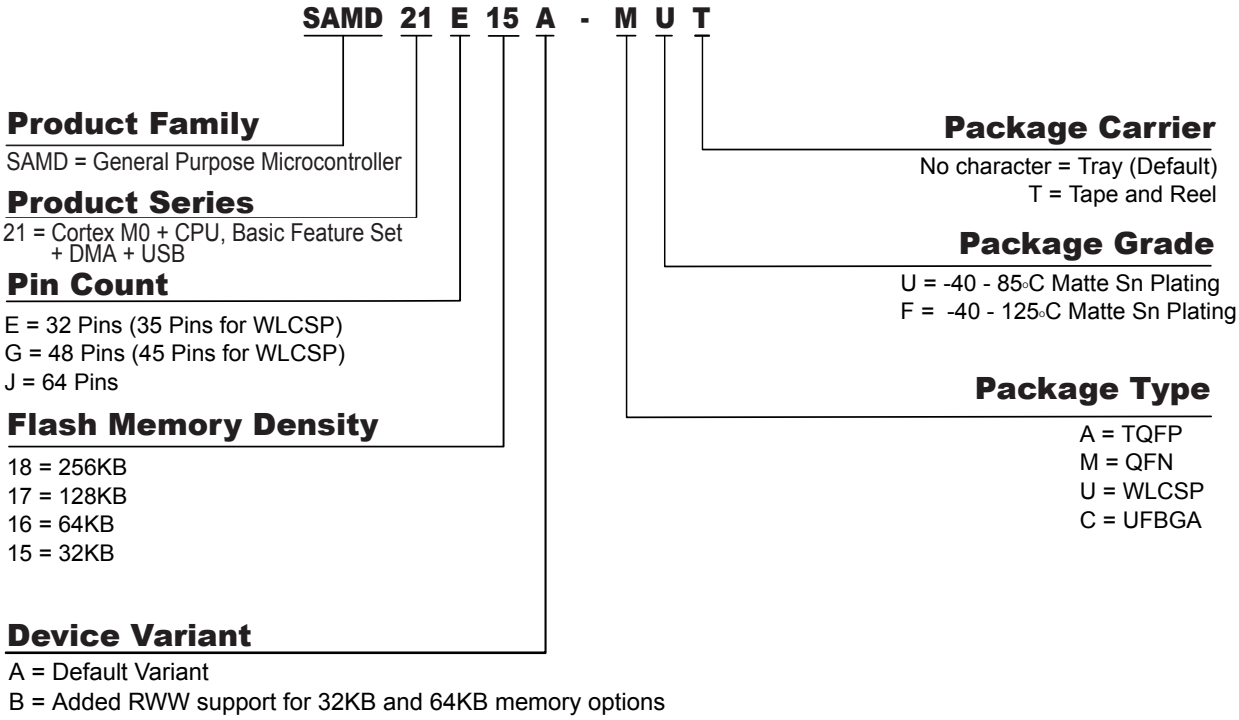
The SAM D21 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

2. Configuration Summary

	SAM D21J	SAM D21G	SAM D21E
Pins	64	48 (45 for WLCSP)	32 (35 for WLCSP)
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	256/128/64/32KB	256/128/64/32KB	256/128/64/32KB
SRAM	32/16/8/4KB	32/16/8/4KB	32/16/8/4KB
Timer Counter (TC) instances	5	3	3
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	8/4/2
DMA channels	12	12	12
USB interface	1	1	1
Serial Communication Interface (SERCOM) instances	6	6	4
Inter-IC Sound (I^2S) interface	1	1	1
Analog-to-Digital Converter (ADC) channels	20	14	10
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) X and Y lines	16x16	12x10	10x6
Maximum CPU frequency	48MHz		

	SAM D21J	SAM D21G	SAM D21E
Packages	QFN TQFP UFBGA	QFN TQFP WLCSP	QFN TQFP WLCSP
Oscillators	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 32KHz ultra-low-power internal oscillator (OSCULP32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)		
Event System channels	12	12	12
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

3. Ordering Information



3.1. SAM D21E

Table 3-1. Device Variant A

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E15A-AU	32K	4K	TQFP32	Tray
ATSAMD21E15A-AUT				Tape & Reel
ATSAMD21E15A-AF				Tray
ATSAMD21E15A-AFT				Tape & Reel
ATSAMD21E15A-MU			QFN32	Tray
ATSAMD21E15A-MUT				Tape & Reel
ATSAMD21E15A-MF				Tray
ATSAMD21E15A-MFT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E16A-AU	64K	8K	TQFP32	Tray
ATSAMD21E16A-AUT				Tape & Reel
ATSAMD21E16A-AF				Tray
ATSAMD21E16A-AFT				Tape & Reel
ATSAMD21E16A-MU			QFN32	Tray
ATSAMD21E16A-MUT				Tape & Reel
ATSAMD21E16A-MF				Tray
ATSAMD21E16A-MFT				Tape & Reel
ATSAMD21E17A-AU	128K	16K	TQFP32	Tray
ATSAMD21E17A-AUT				Tape & Reel
ATSAMD21E17A-AF				Tray
ATSAMD21E17A-AFT				Tape & Reel
ATSAMD21E17A-MU			QFN32	Tray
ATSAMD21E17A-MUT				Tape & Reel
ATSAMD21E17A-MF				Tray
ATSAMD21E17A-MFT				Tape & Reel
ATSAMD21E18A-AU	256K	32K	TQFP32	Tray
ATSAMD21E18A-AUT				Tape & Reel
ATSAMD21E18A-AF				Tray
ATSAMD21E18A-AFT				Tape & Reel
ATSAMD21E18A-MU			QFN32	Tray
ATSAMD21E18A-MUT				Tape & Reel
ATSAMD21E18A-MF				Tray
ATSAMD21E18A-MFT				Tape & Reel

Table 3-2. Device Variant B

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21E15B-AU	32K	4K	TQFP32	Tray
ATSAMD21E15B-AUT				Tape & Reel
ATSAMD21E15B-AF				Tray
ATSAMD21E15B-AFT				Tape & Reel
ATSAMD21E15B-MU			QFN32	Tray
ATSAMD21E15B-MUT				Tape & Reel
ATSAMD21E15B-MF				Tray
ATSAMD21E15B-MFT				Tape & Reel
ATSAMD21E15B-UUT			WLCSP35	Tape & Reel
ATSAMD21E16B-AU	64K	8K	TQFP32	Tray
ATSAMD21E16B-AUT				Tape & Reel
ATSAMD21E16B-AF				Tray
ATSAMD21E16B-AFT				Tape & Reel
ATSAMD21E16B-MU			QFN32	Tray
ATSAMD21E16B-MUT				Tape & Reel
ATSAMD21E16B-MF				Tray
ATSAMD21E16B-MFT				Tape & Reel
ATSAMD21E16B-UUT	64K	8K	WLCSP35	Tape & Reel

3.2. SAM D21G

Table 3-3. Device Variant A

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21G15A-AU	32K	4K	TQFP48	Tray
ATSAMD21G15A-AUT				Tape & Reel
ATSAMD21G15A-AF				Tray
ATSAMD21G15A-AFT				Tape & Reel
ATSAMD21G15A-MU			QFN48	Tray
ATSAMD21G15A-MUT				Tape & Reel
ATSAMD21G15A-MF				Tray
ATSAMD21G15A-MFT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21G16A-AU	64K	8K	TQFP48	Tray
ATSAMD21G16A-AUT				Tape & Reel
ATSAMD21G16A-AF				Tray
ATSAMD21G16A-AFT				Tape & Reel
ATSAMD21G16A-MU			QFN48	Tray
ATSAMD21G16A-MUT				Tape & Reel
ATSAMD21G16A-MF				Tray
ATSAMD21G16A-MFT				Tape & Reel
ATSAMD21G17A-AU	128K	16K	TQFP48	Tray
ATSAMD21G17A-AUT				Tape & Reel
ATSAMD21G17A-AF				Tray
ATSAMD21G17A-AFT				Tape & Reel
ATSAMD21G17A-MU			QFN48	Tray
ATSAMD21G17A-MUT				Tape & Reel
ATSAMD21G17A-MF				Tray
ATSAMD21G17A-MFT				Tape & Reel
ATSAMD21G17A-UUT			WLCSP45	Tape & Reel
ATSAMD21G18A-AU	256K	32K	TQFP48	Tray
ATSAMD21G18A-AUT				Tape & Reel
ATSAMD21G18A-AF				Tray
ATSAMD21G18A-AFT				Tape & Reel
ATSAMD21G18A-MU			QFN48	Tray
ATSAMD21G18A-MUT				Tape & Reel
ATSAMD21G18A-MF				Tray
ATSAMD21G18A-MFT				Tape & Reel
ATSAMD21G18A-UUT			WLCSP45	Tape & Reel

Table 3-4. Device Variant B

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21G15B-AU	32K	4K	TQFP48	Tray
ATSAMD21G15B-AUT				Tape & Reel
ATSAMD21G15B-AF				Tray
ATSAMD21G15B-AFT				Tape & Reel
ATSAMD21G15B-MU			QFN48	Tray
ATSAMD21G15B-MUT				Tape & Reel
ATSAMD21G15B-MF				Tray
ATSAMD21G15B-MFT				Tape & Reel
ATSAMD21G16B-AU	64K	8K	TQFP48	Tray
ATSAMD21G16B-AUT				Tape & Reel
ATSAMD21G16B-AF				Tray
ATSAMD21G16B-AFT				Tape & Reel
ATSAMD21G16B-MU			QFN48	Tray
ATSAMD21G16B-MUT				Tape & Reel
ATSAMD21G16B-MF				Tray
ATSAMD21G16B-MFT				Tape & Reel

3.3. SAM D21J

Table 3-5. Device Variant A

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21J15A-AU	32K	4K	TQFP64	Tray
ATSAMD21J15A-AUT				Tape & Reel
ATSAMD21J15A-AF				Tray
ATSAMD21J15A-AFT				Tape & Reel
ATSAMD21J15A-MU			QFN64	Tray
ATSAMD21J15A-MUT				Tape & Reel
ATSAMD21J15A-MF				Tray
ATSAMD21J15A-MFT				Tape & Reel

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21J16A-AU	64K	8K	TQFP64	Tray
ATSAMD21J16A-AUT				Tape & Reel
ATSAMD21J16A-AF				Tray
ATSAMD21J16A-AFT				Tape & Reel
ATSAMD21J16A-MU			QFN64	Tray
ATSAMD21J16A-MUT				Tape & Reel
ATSAMD21J16A-MF				Tray
ATSAMD21J16A-MFT				Tape & Reel
ATSAMD21J16A-CU			UFBGA64	Tray
ATSAMD21J16A-CUT				Tape & Reel
ATSAMD21J17A-AU	128K	16K	TQFP64	Tray
ATSAMD21J17A-AUT				Tape & Reel
ATSAMD21J17A-AF				Tray
ATSAMD21J17A-AFT				Tape & Reel
ATSAMD21J17A-MU			QFN64	Tray
ATSAMD21J17A-MUT				Tape & Reel
ATSAMD21J17A-MF				Tray
ATSAMD21J17A-MFT				Tape & Reel
ATSAMD21J17A-CU			UFBGA64	Tray
ATSAMD21J17A-CUT				Tape & Reel
ATSAMD21J18A-AU	256K	32K	TQFP64	Tray
ATSAMD21J18A-AUT				Tape & Reel
ATSAMD21J18A-AF				Tray
ATSAMD21J18A-AFT				Tape & Reel
ATSAMD21J18A-MU			QFN64	Tray
ATSAMD21J18A-MUT				Tape & Reel
ATSAMD21J18A-MF				Tray
ATSAMD21J18A-MFT				Tape & Reel
ATSAMD21J18A-CU			UFBGA64	Tray
ATSAMD21J18A-CUT				Tape & Reel

Table 3-6. Device Variant B

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21J15B-AU	32K	4K	TQFP64	Tray
ATSAMD21J15B-AUT				Tape & Reel
ATSAMD21J15B-AF				Tray
ATSAMD21J15B-AFT				Tape & Reel
ATSAMD21J15B-MU			QFN64	Tray
ATSAMD21J15B-MUT				Tape & Reel
ATSAMD21J15B-MF				Tray
ATSAMD21J15B-MFT				Tape & Reel
ATSAMD21J16B-AU	64K	8K	TQFP64	Tray
ATSAMD21J16B-AUT				Tape & Reel
ATSAMD21J16B-AF				Tray
ATSAMD21J16B-AFT				Tape & Reel
ATSAMD21J16B-MU			QFN64	Tray
ATSAMD21J16B-MUT				Tape & Reel
ATSAMD21J16B-MF				Tray
ATSAMD21J16B-MFT				Tape & Reel
ATSAMD21J16B-CU			UFBGA64	Tray
ATSAMD21J16B-CUT				Tape & Reel

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM D21 variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

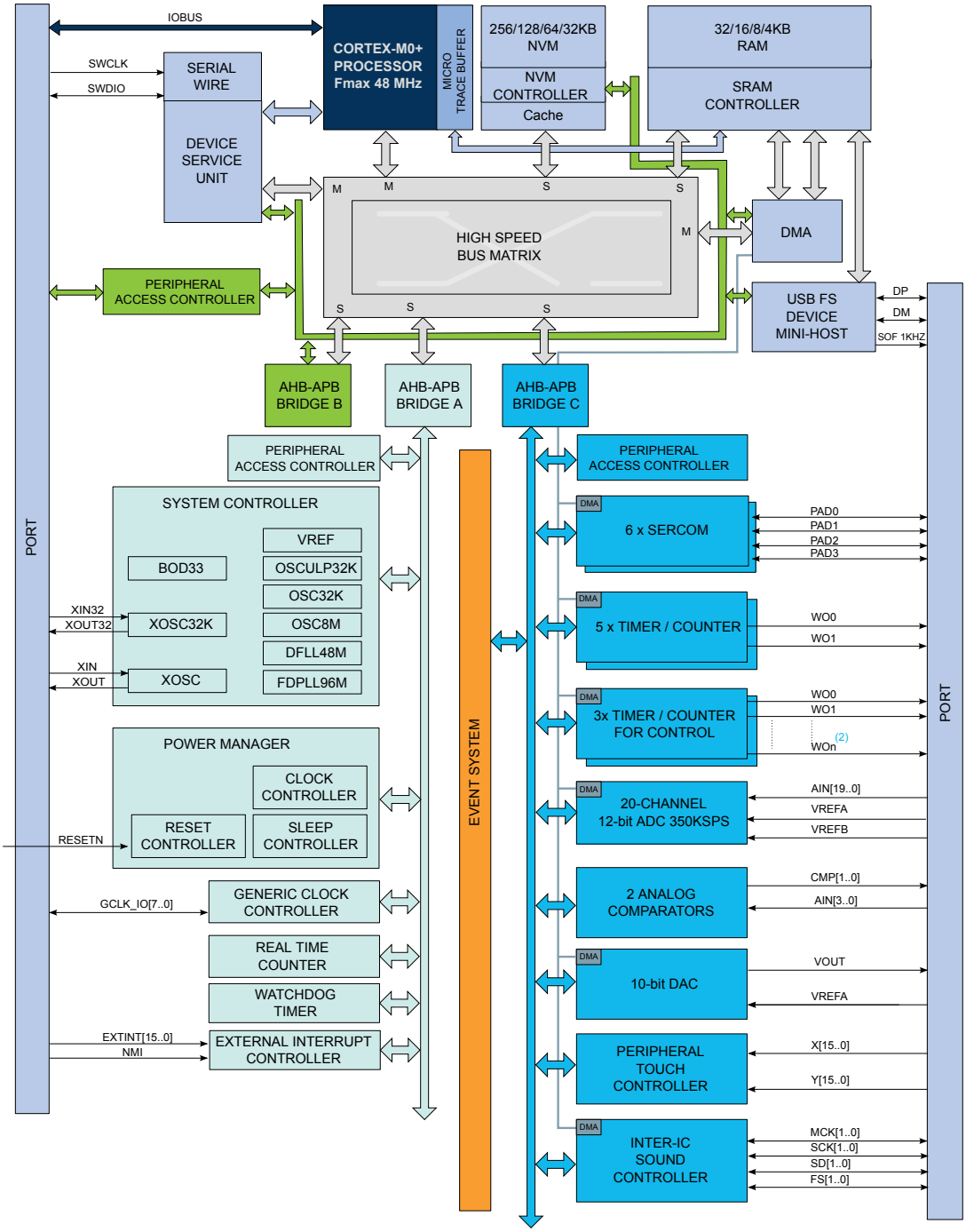
Table 3-7. SAM D21 Device Identification Values

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD21J18A	0x00	0x10010000
SAMD21J17A	0x01	0x10010001
SAMD21J16A	0x02	0x10010002
SAMD21J15A	0x03	0x10010003
Reserved	0x04	
SAMD21G18A	0x05	0x10010005
SAMD21G17A	0x06	0x10010006

Device Variant	DID.DEVSEL	Device ID (DID)
SAMD21G16A	0x07	0x10010007
SAMD21G15A	0x08	0x10010008
Reserved	0x09	
SAMD21E18A	0x0A	0x1001000A
SAMD21E17A	0x0B	0x1001000B
SAMD21E16A	0x0C	0x1001000C
SAMD21E15A	0x0D	0x1001000D
Reserved	0x0E	
SAMD21G18A (WLCSP)	0x0F	0x1001000F
SAMD21G17A (WLCSP)	0x10	0x10010010
Reserved	0x11 - 0x1F	
SAMD21J16B	0x20	0x10011420
SAMD21J15B	0x21	0x10011421
Reserved	0x22	
SAMD21G16B	0x23	0x10011423
SAMD21G15B	0x24	0x10011424
Reserved	0x25	
SAMD21E16B	0x26	0x10011426
SAMD21E15B	0x27	0x10011427
Reserved	0x28-0x54	
SAMD21E16B (WLCSP)	0x55	0x10011455
SAMD21E15B (WLCSP)	0x56	0x10011456
Reserved	0x57-0xFF	

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4. Block Diagram

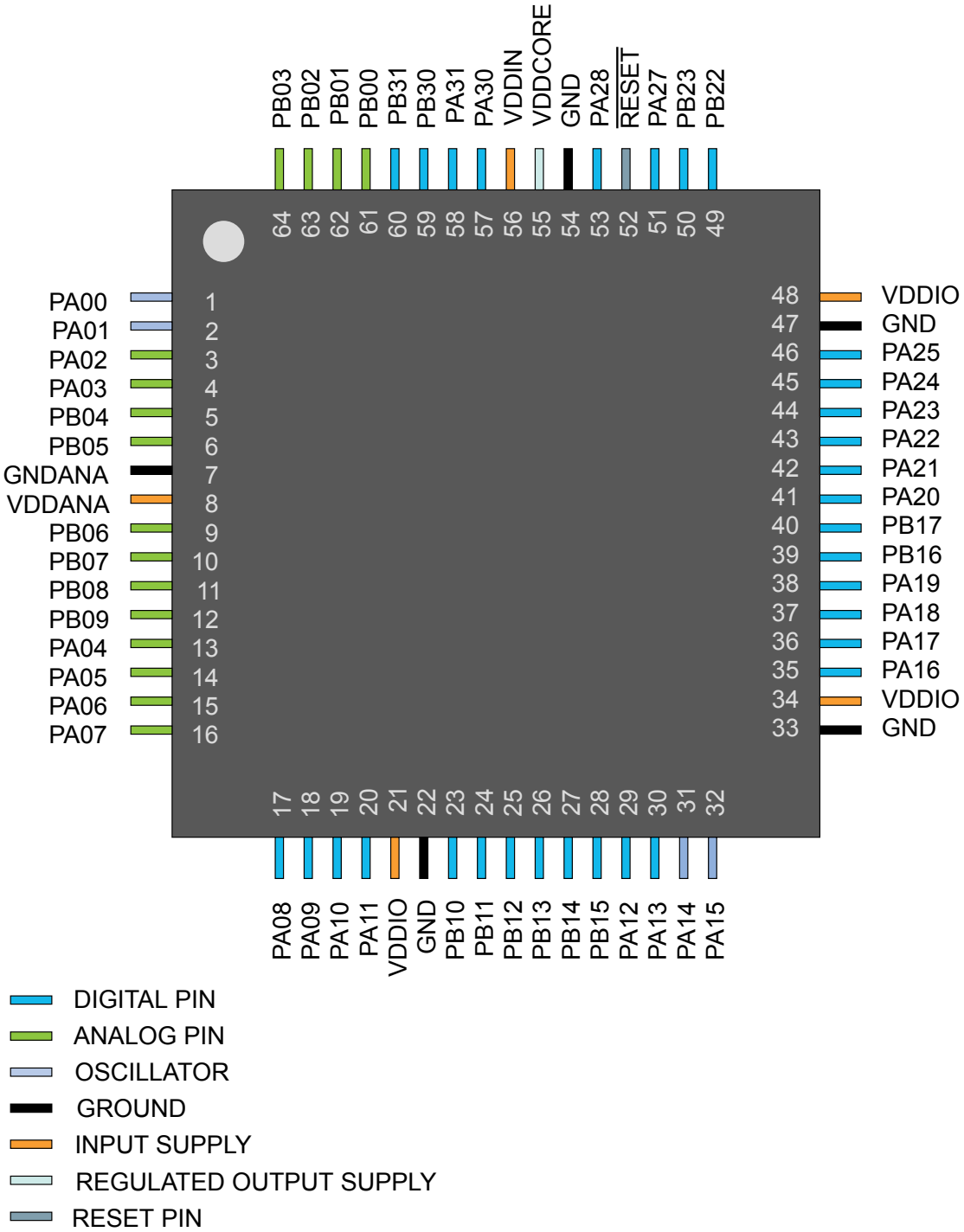


1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to the Configuration Summary for details.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines. Refer to the TCC Configuration for details.

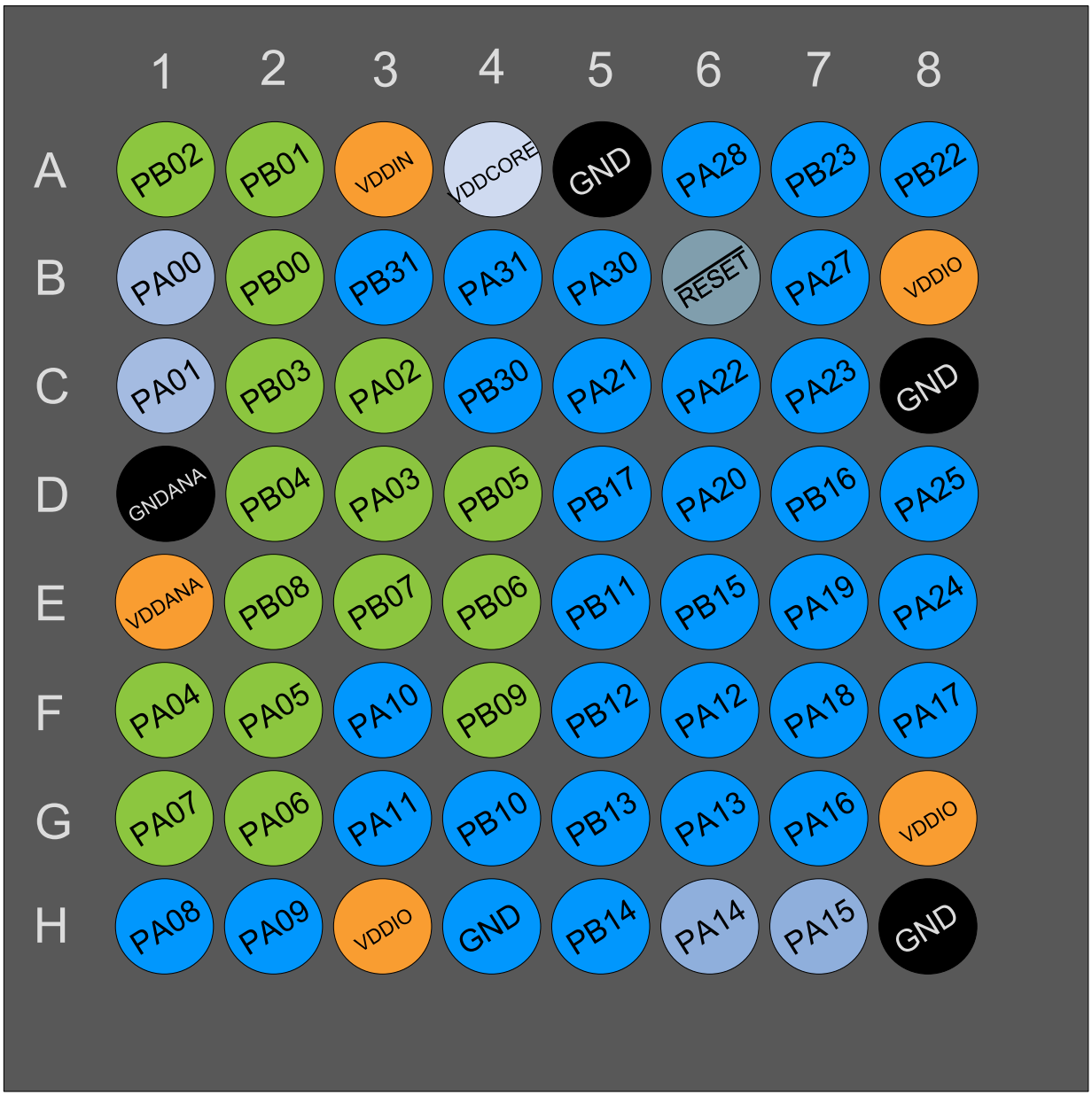
5. Pinout

5.1. SAM D21J

5.1.1. QFN64 / TQFP64



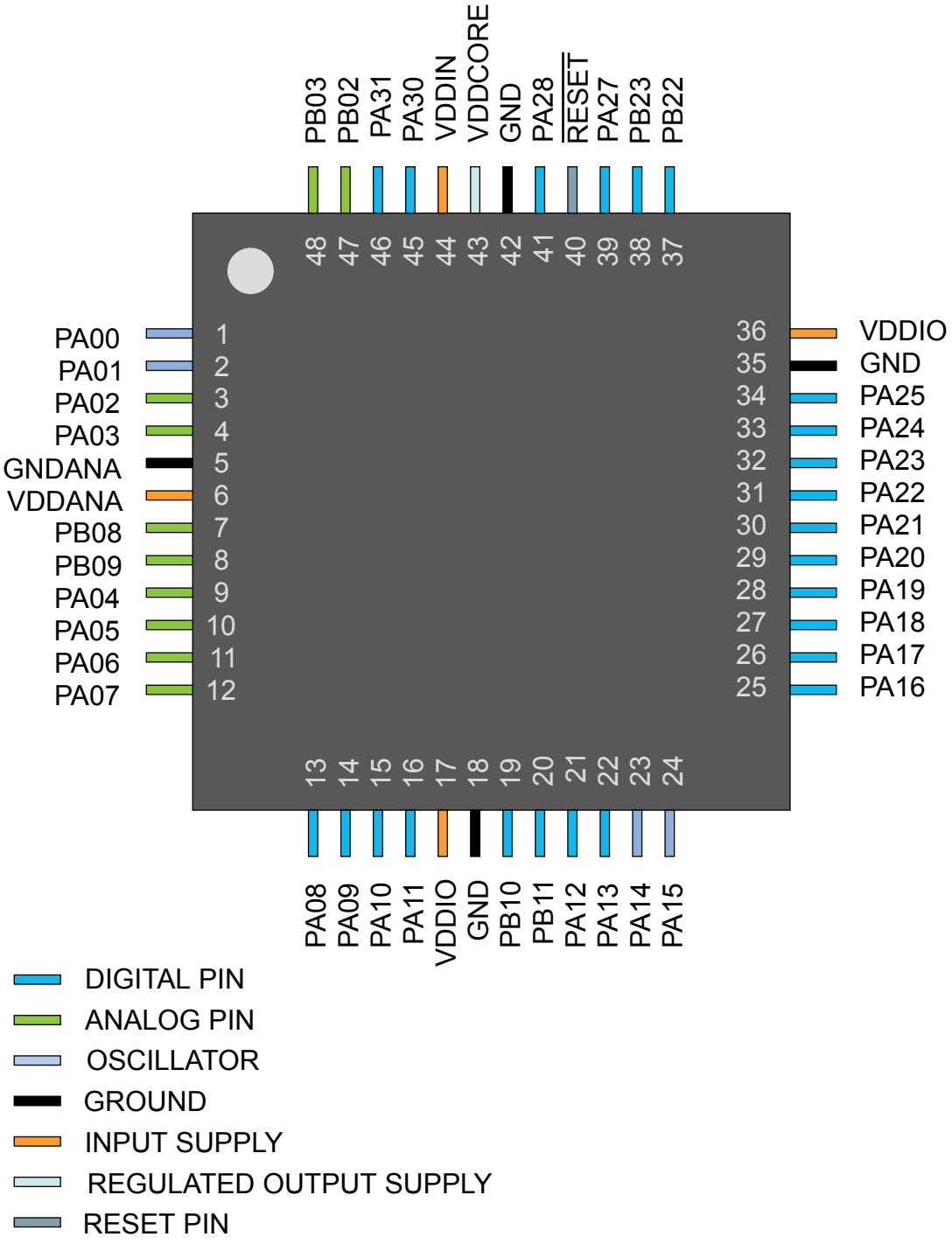
5.1.2. UFBGA64



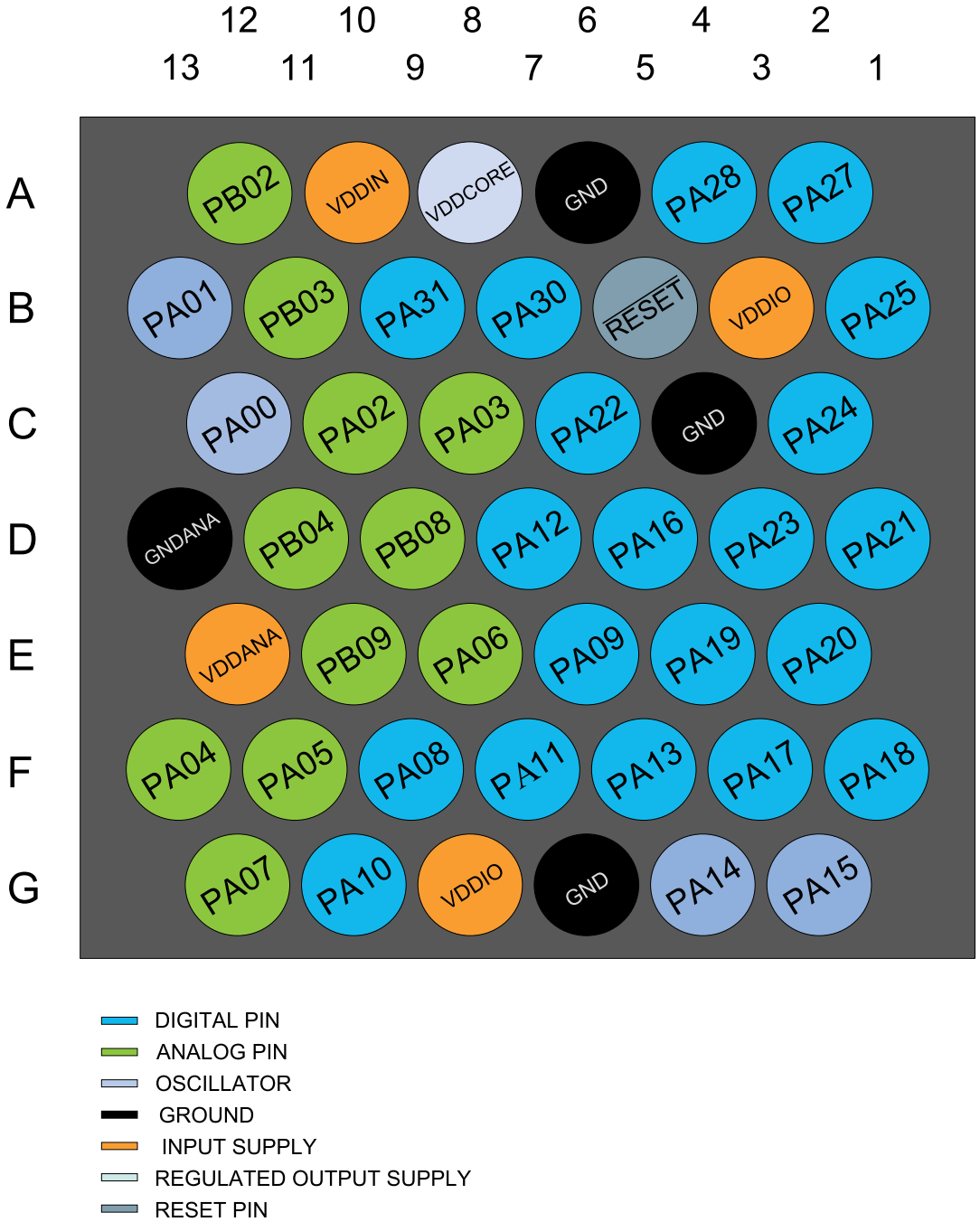
- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

5.2. SAM D21G

5.2.1. QFN48 / TQFP48

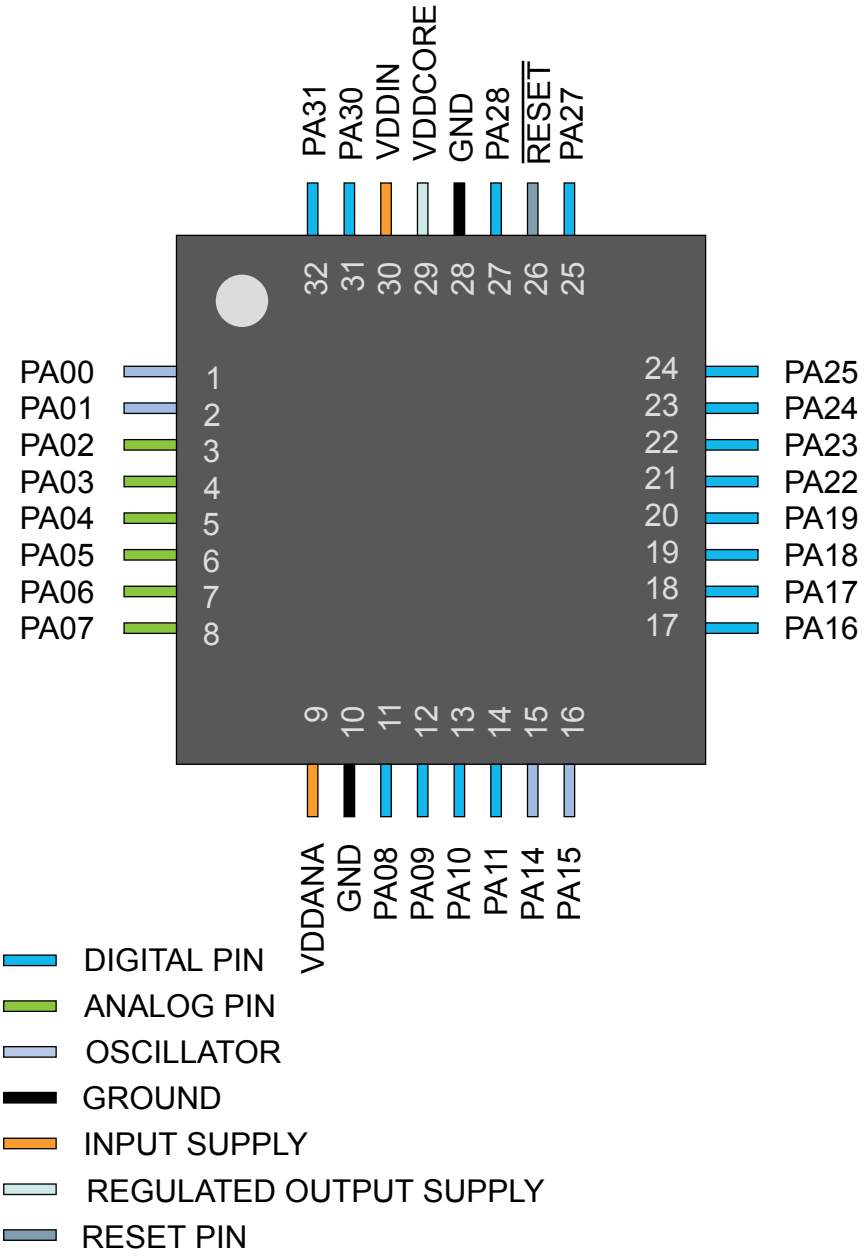


5.2.2. WLCSP45

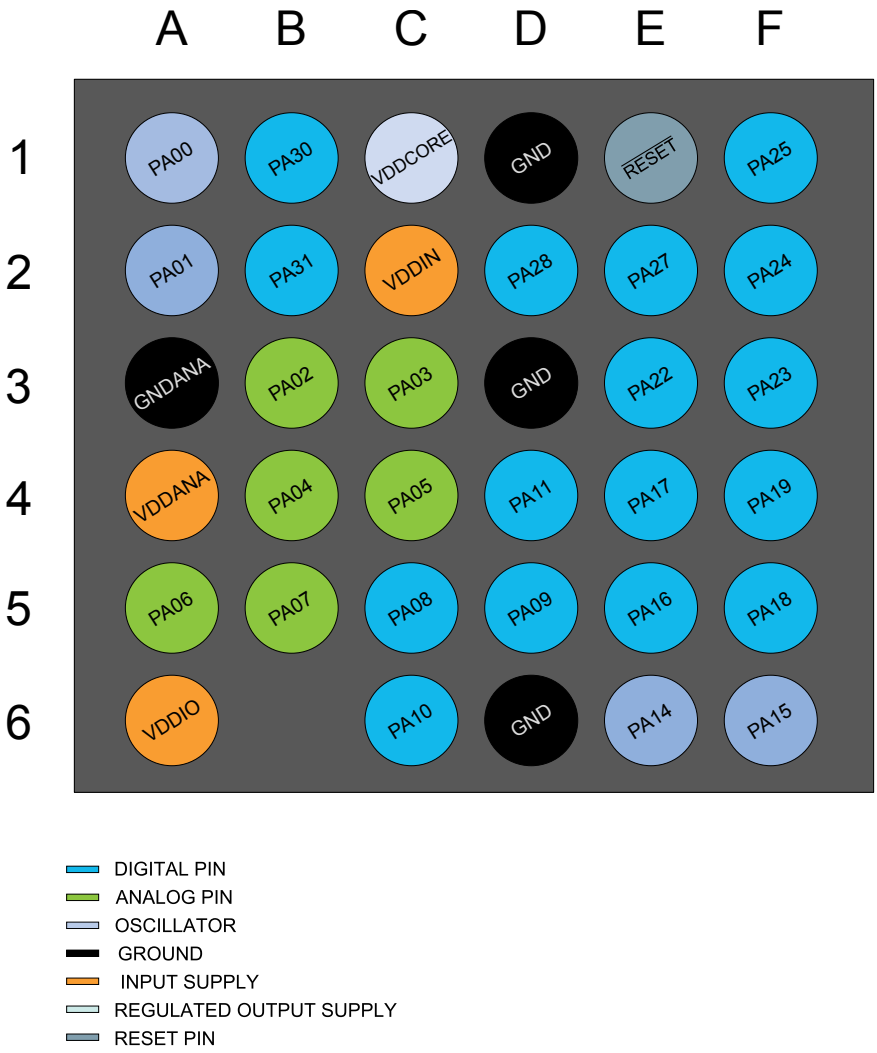

12 10 8 6 4 2
13 11 9 7 5 3 1
A
B
C
D
E
F
G
PB02 VDDIN VDDCORE GND PA28 PA27
PA01 PB03 PA31 PA30 RESET VDDIO PA25
PA00 PA02 PA03 PA22 GND PA24
GNDANA PB04 PB08 PA12 PA16 PA23 PA21
VDDANA PB09 PA06 PA09 PA19 PA20
PA04 PA05 PA08 PA11 PA13 PA17 PA18
PA07 PA10 VDDIO GND PA14 PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

5.3. SAM D21E

5.3.1. QFN32 / TQFP32

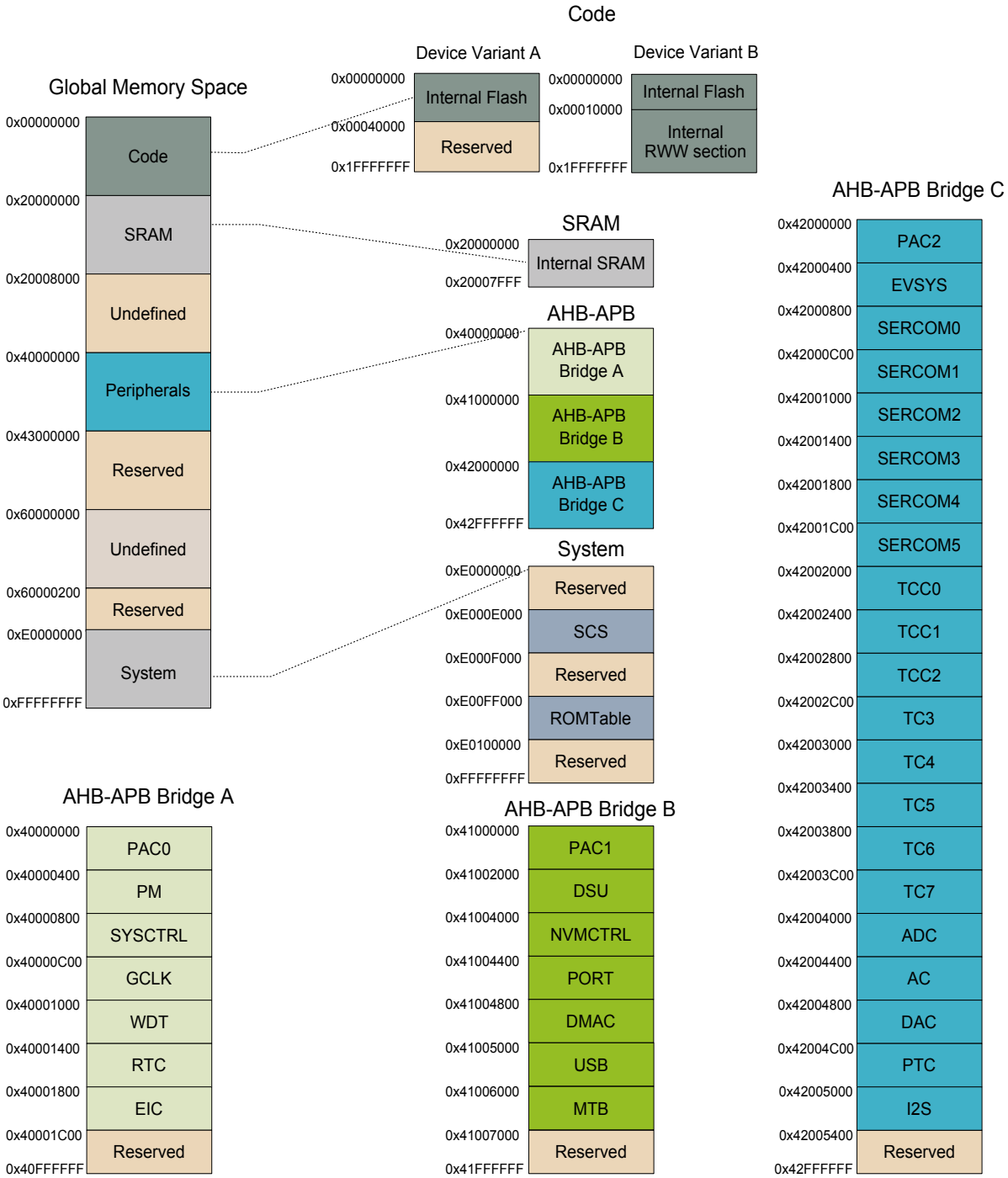


5.3.2. WLCSP35


A B C D E F
1 2 3 4 5 6
PA00 PA30 VDDCORE GND RESET PA25
PA01 PA31 VDDIN PA28 PA27 PA24
GNDANA PA02 PA03 GND PA22 PA23
VDDANA PA04 PA05 PA11 PA17 PA19
PA06 PA07 PA08 PA09 PA16 PA18
VDDIO PA10 GND PA14 PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

6. Product Mapping

Figure 6-1. Atmel SAM D21 Product Mapping



This figure represents the full configuration of the Atmel® SAM D21 with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the Configuration Summary for details.

7. Processor And Architecture

7.1. Cortex M0+ Processor

The SAM D21 implements the ARM® Cortex®-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The ARM Cortex-M0+ implemented is revision r0p1. For more information refer to http://www.arm.com.

7.1.1. Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration

Features	Configurable option	Device configuration
Interrupts	External interrupts 0-32	28
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Absent(1)
Memory Protection Unit	Not present or 8-region	Not present
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

Note:

1. All software run in privileged mode only.

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores.

7.1.2. Cortex-M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Timer (SysTick)

  - The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to Nested Vector Interrupt Controller and the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (www.arm.com).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (www.arm.com).

7.1.3. Cortex-M0+ Address Map

Table 7-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000 (see also Product Mapping)	Micro Trace Buffer (MTB)

7.1.4. I/O Interface

7.1.4.1. Overview

Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed. Refer to *CPU Local Bus* for more information.

7.1.4.2. Description

Direct access to PORT registers.

7.2. Nested Vector Interrupt Controller

7.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM D21 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (www.arm.com).

7.2.2. Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear

(INTFLAG) register. The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR). For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 7-3. Interrupt Line Mapping (Continued)

Peripheral Source	NVIC Line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager	0
SYSCTRL – System Control	1
WDT – Watchdog Timer	2
RTC – Real Time Counter	3
EIC – External Interrupt Controller	4
NVMCTRL – Non-Volatile Memory Controller	5
DMAC - Direct Memory Access Controller	6
USB - Universal Serial Bus	7
EVSYS – Event System	8
SERCOM0 – Serial Communication Interface 0	9
SERCOM1 – Serial Communication Interface 1	10
SERCOM2 – Serial Communication Interface 2	11
SERCOM3 – Serial Communication Interface 3	12
SERCOM4 – Serial Communication Interface 4	13
SERCOM5 – Serial Communication Interface 5	14
TCC0 – Timer Counter for Control 0	15
TCC1 – Timer Counter for Control 1	16
TCC2 – Timer Counter for Control 2	17
TC3 – Timer Counter 3	18
TC4 – Timer Counter 4	19
TC5 – Timer Counter 5	20
TC6 – Timer Counter 6	21
TC7 – Timer Counter 7	22

Peripheral Source	NVIC Line
ADC – Analog-to-Digital Converter	23
AC – Analog Comparator	24
DAC – Digital-to-Analog Converter	25
PTC – Peripheral Touch Controller	26
I2S - Inter IC Sound	27

7.3. Micro Trace Buffer

7.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2. Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

7.4. High-Speed Bus System

7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

7.4.2. Configuration

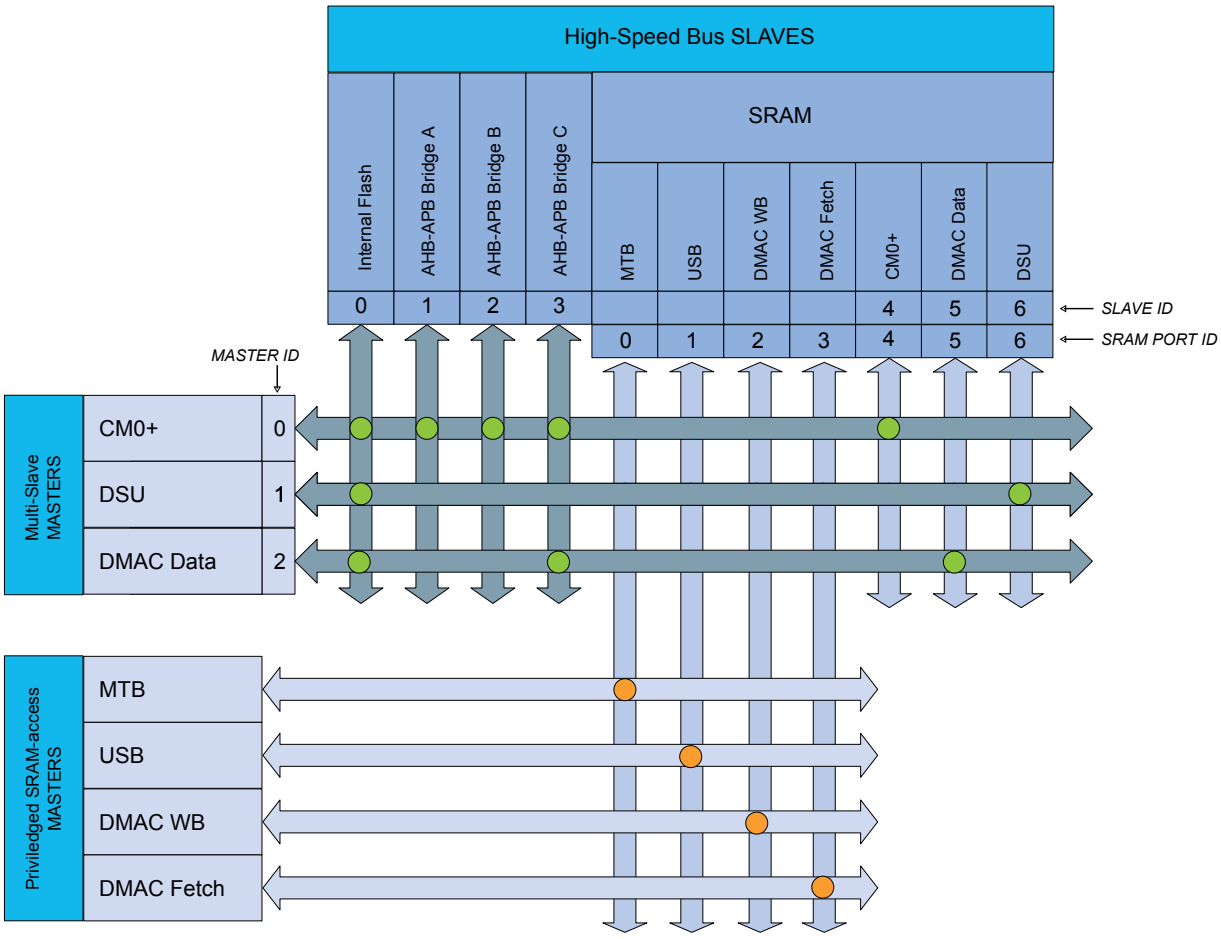


Table 7-4. Bus Matrix Masters

Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1

Table 7-5. Bus Matrix Slaves

Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
AHB-APB Bridge A	1
AHB-APB Bridge B	2
AHB-APB Bridge C	3
SRAM Port 4 - CM0+ Access	4
SRAM Port 5 - DMAC Data Access	5
SRAM Port 6 - DSU Access	6

Table 7-6. SRAM Port Connection

SRAM Port Connection	Port ID	Connection Type
MTB - Micro Trace Buffer	0	Direct
USB - Universal Serial Bus	1	Direct
DMAC - Direct Memory Access Controller - Write-Back Access	2	Direct
DMAC - Direct Memory Access Controller - Fetch Access	3	Direct
CM0+ - Cortex M0+ Processor	4	Bus Matrix
DMAC - Direct Memory Access Controller - Data Access	5	Bus Matrix
DSU - Device Service Unit	6	Bus Matrix

7.4.3. SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, the different masters can be configured to have a given priority for different type of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration is shown in Table. Quality of Service.

Table 7-7. Quality of Service

Value	Name	Description
00	DISABLE	Background (no sensitive operation)
01	LOW	Sensitive Bandwidth
10	MEDIUM	Sensitive Latency
11	HIGH	Critical Latency

If a master is configured with QoS level 0x00 or 0x01 there will be minimum one cycle latency for the RAM access.

The priority order for concurrent accesses are decided by two factors. First the QoS level for the master and then a static priority given by table nn-mm (table: SRAM port connection) where the lowest port ID has the highest static priority.

The MTB has fixed QoS level 3 and the DSU has fixed QoS level 1.

The CPU QoS level can be written/read at address 0x41007110, bits [1:0]. Its reset value is 0x0.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see Product Mapping).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBx_AHB) must be enabled. See *PM – Power Manager* for details.

Figure 7-1. APB Write Access.

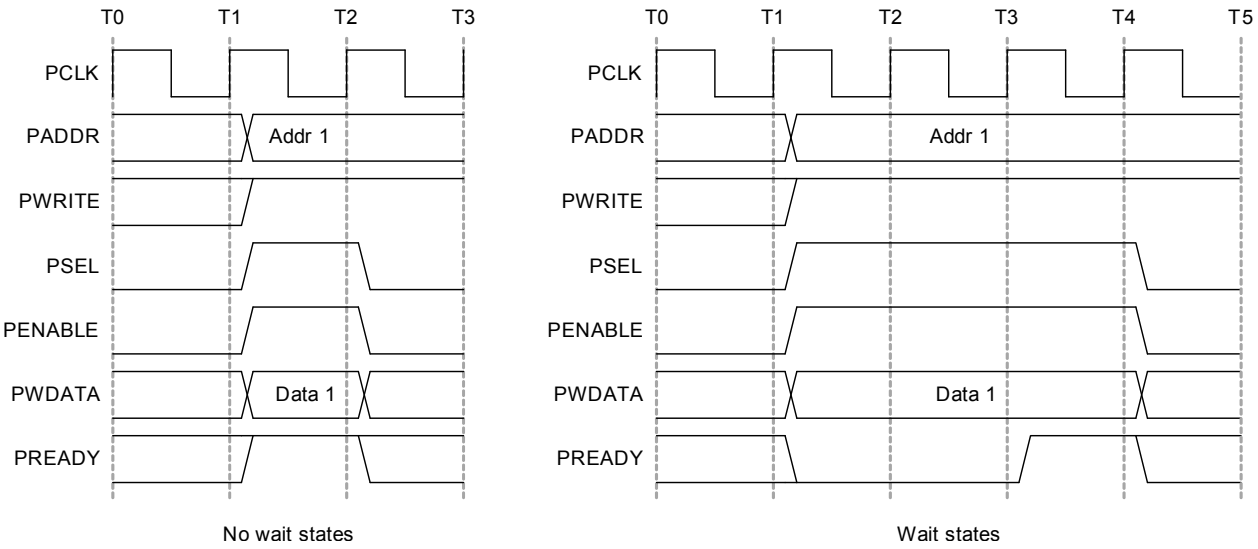
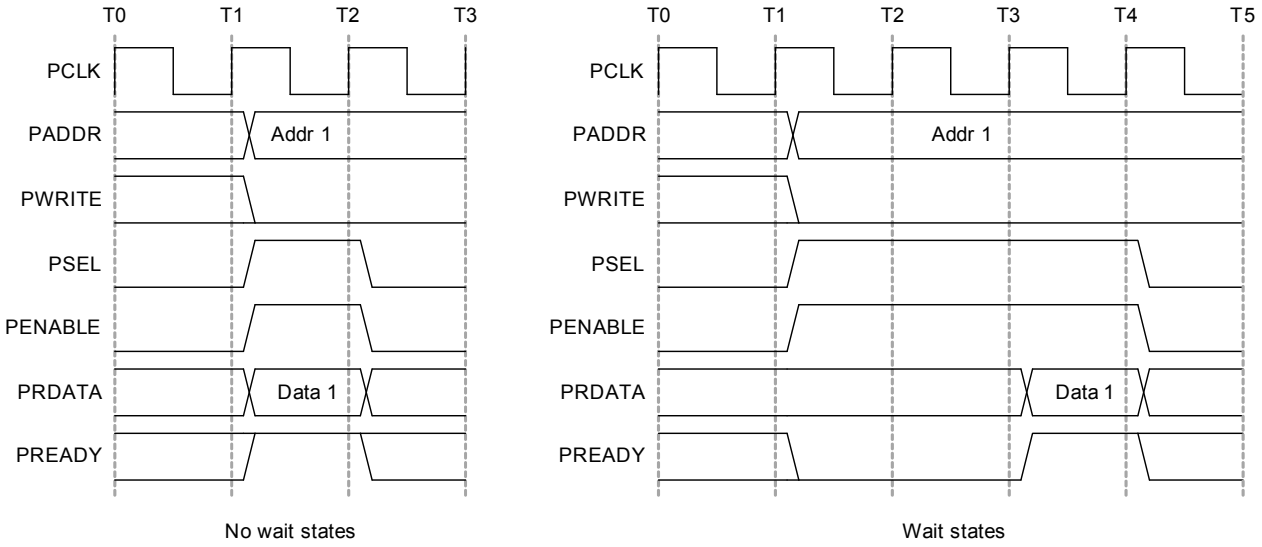


Figure 7-2. APB Read Access.



7.6. PAC - Peripheral Access Controller

7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled are reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

Write-protect registers allow the user to disable a selected peripheral's write-protection without doing a read-modify-write operation. These registers are mapped into two I/O memory locations, one for clearing and one for setting the register bits. Writing a one to a bit in the Write Protect Clear register (WPCLR) will clear the corresponding bit in both registers (WPCLR and WPSET) and disable the write-protection for the corresponding peripheral, while writing a one to a bit in the Write Protect Set (WPSET) register will set the corresponding bit in both registers (WPCLR and WPSET) and enable the write-protection for the corresponding peripheral. Both registers (WPCLR and WPSET) will return the same value when read.

If a peripheral is write-protected, and if a write access is performed, data will not be written, and the peripheral will return an access error (CPU exception).

The PAC also offers a safety feature for correct program execution, with a CPU exception generated on double write-protection or double unprotection of a peripheral. If a peripheral n is write-protected and a write to one in WPSET[n] is detected, the PAC returns an error. This can be used to ensure that the application follows the intended program flow by always following a write-protect with an unprotect, and vice versa. However, in applications where a write-protected peripheral is used in several contexts, e.g., interrupts, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulate the write-protection status, or when the interrupt handler needs to unprotect the peripheral, based on the current protection status, by reading WPSET.

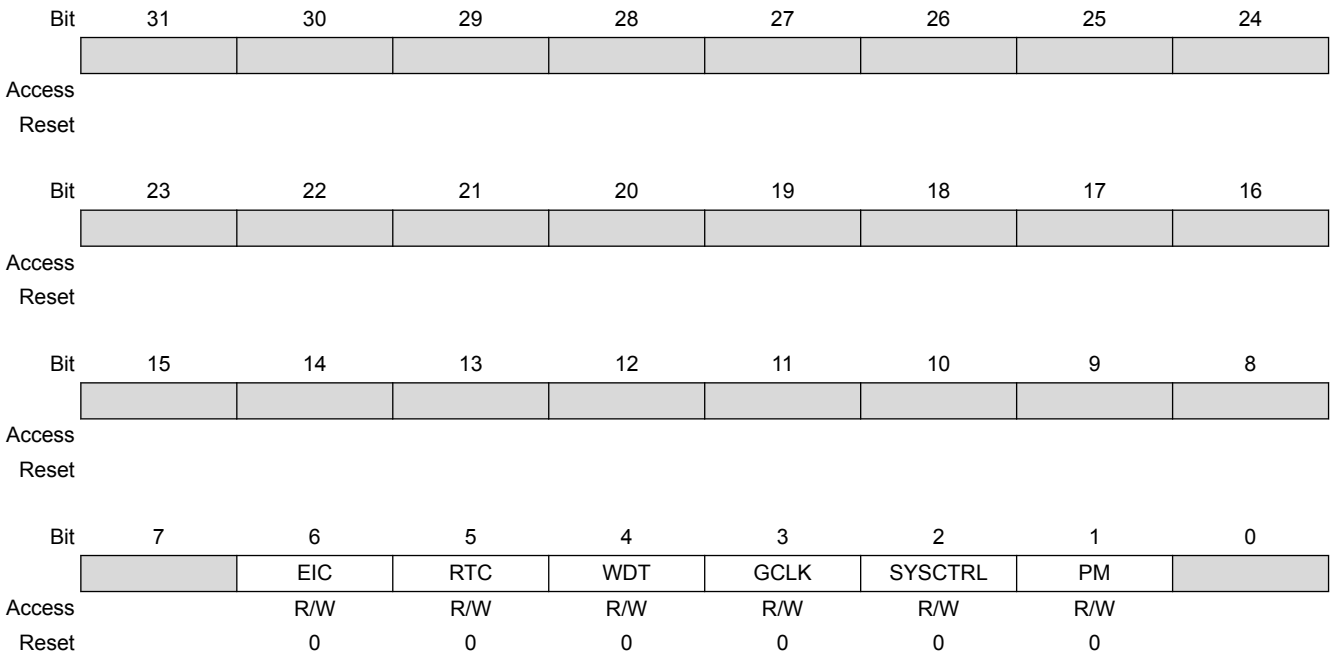
7.6.2. Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

7.6.2.1. PAC0 Register Description

Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000000
Property: –



Bit 6 – EIC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

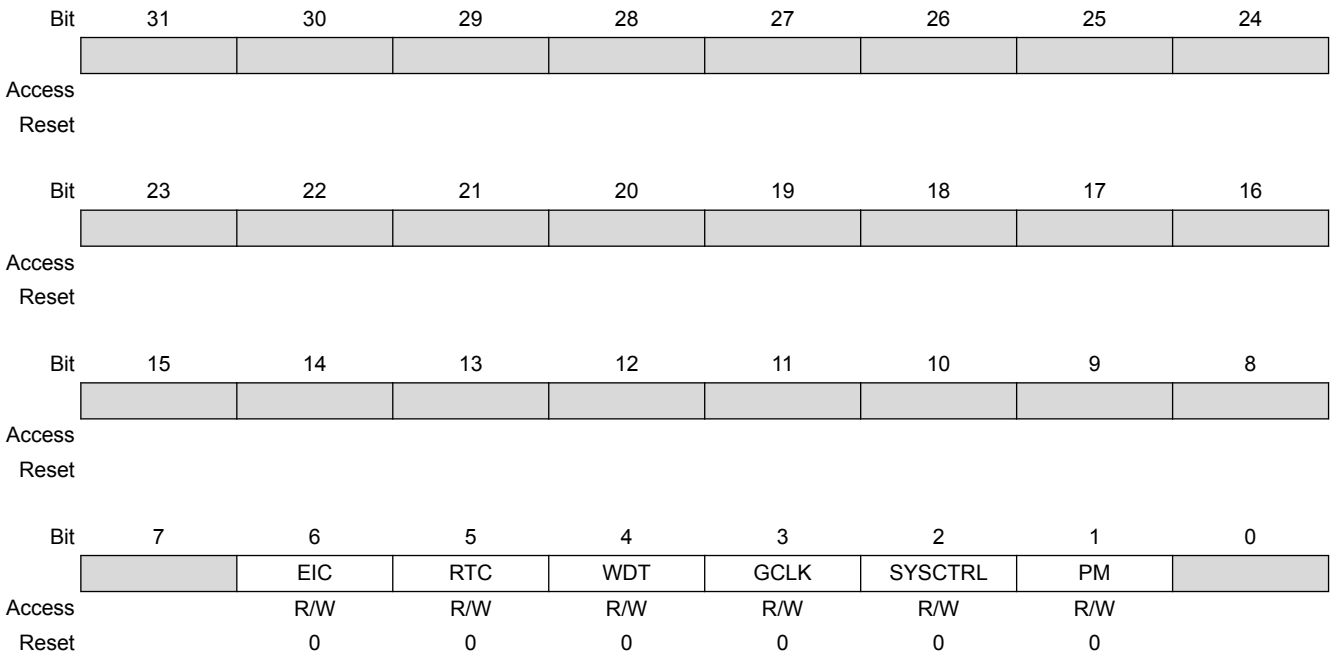
Bit 1 – PM
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000000
Property: –



Bit 6 – EIC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – RTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – PM
Writing a zero to these bits has no effect.

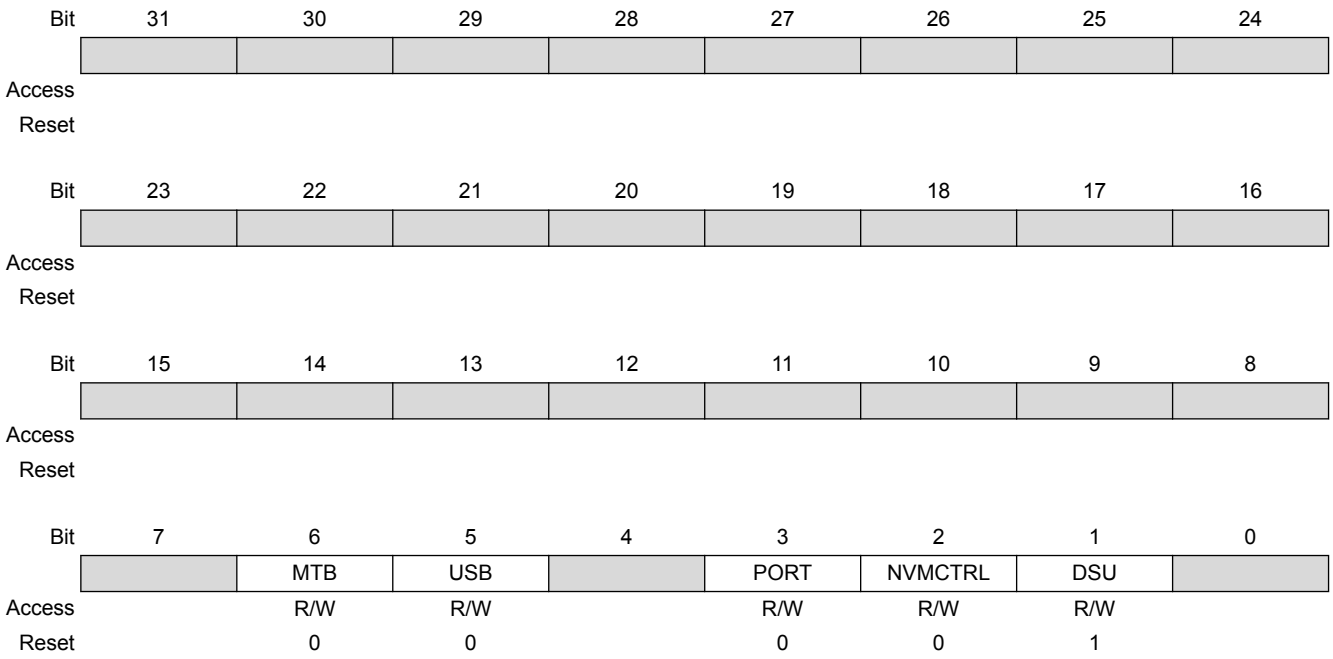
Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.6.2.2. PAC1 Register Description

Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x000002
Property: –



Bit 6 – MTB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – USB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

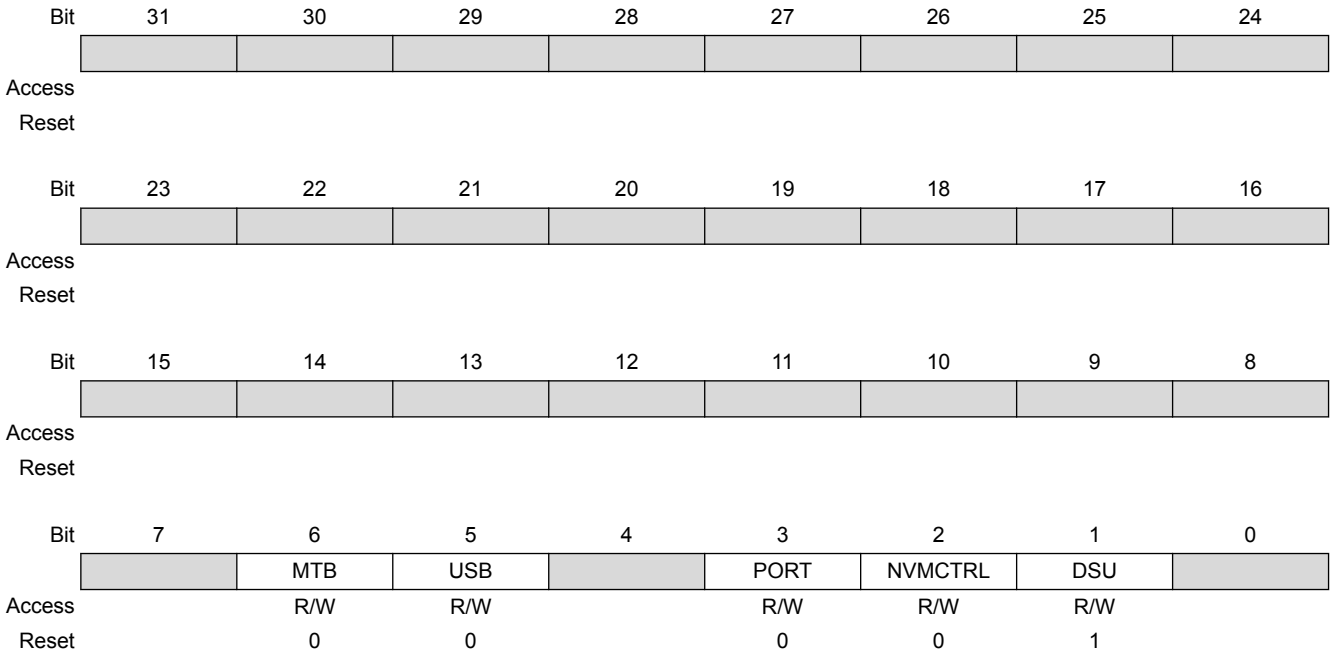
Bit 1 – DSU
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000002
Property: –



Bit 6 – MTB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 5 – USB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

7.6.2.3. PAC2 Register Description

Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
				I2S	PTC	DAC	AC	ADC
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
						TCC2	TCC1	TCC0
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
							EVSYS	
Access							R/W	
Reset							0	

Bit 20 – I2S
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 19 – PTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 8, 9, 10 – TCC0, TCC1, TCC2
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – EVSYS
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
				I2S	PTC	DAC	AC	ADC
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
						TCC2	TCC1	TCC0
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
							EVSYS	
Access							R/W	
Reset							0	

Bit 20 – I2S
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 19 – PTC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 18 – DAC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 17 – AC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 16 – ADC
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bits 8, 9, 10 – TCC0, TCC1, TCC2
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – EVSYS
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

8. Packaging Information

8.1. Thermal Considerations

Related Links

Junction Temperature on page 44

8.1.1. Thermal Resistance Data

The following Table summarizes the thermal resistance data depending on the package.

Table 8-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	64.7°C/W	23.1°C/W
48-pin TQFP	63.6°C/W	12.2°C/W
64-pin TQFP	60.9°C/W	12.2°C/W
32-pin QFN	40.9°C/W	15.2°C/W
48-pin QFN	32.0°C/W	10.9°C/W
64-pin QFN	32.5°C/W	10.7°C/W
35-ball WLCSP	41.8°C/W	2.26°C/W

8.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

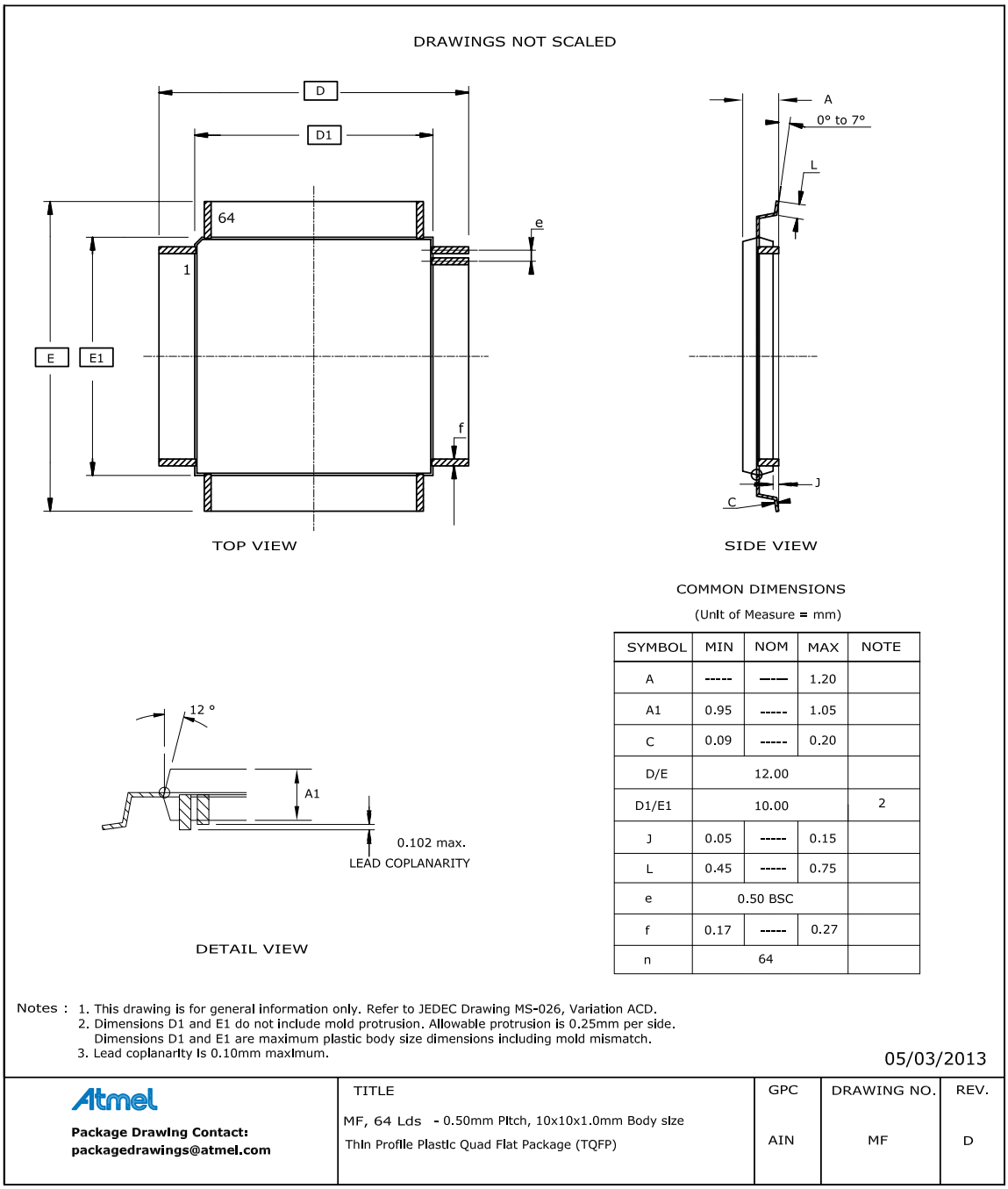
From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Related Links

Thermal Considerations on page 44

8.2. Package Drawings

8.2.1. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	GPC AIN	DRAWING NO. MF	REV. D

Table 8-2. Device and Package Maximum Weight

300	mg

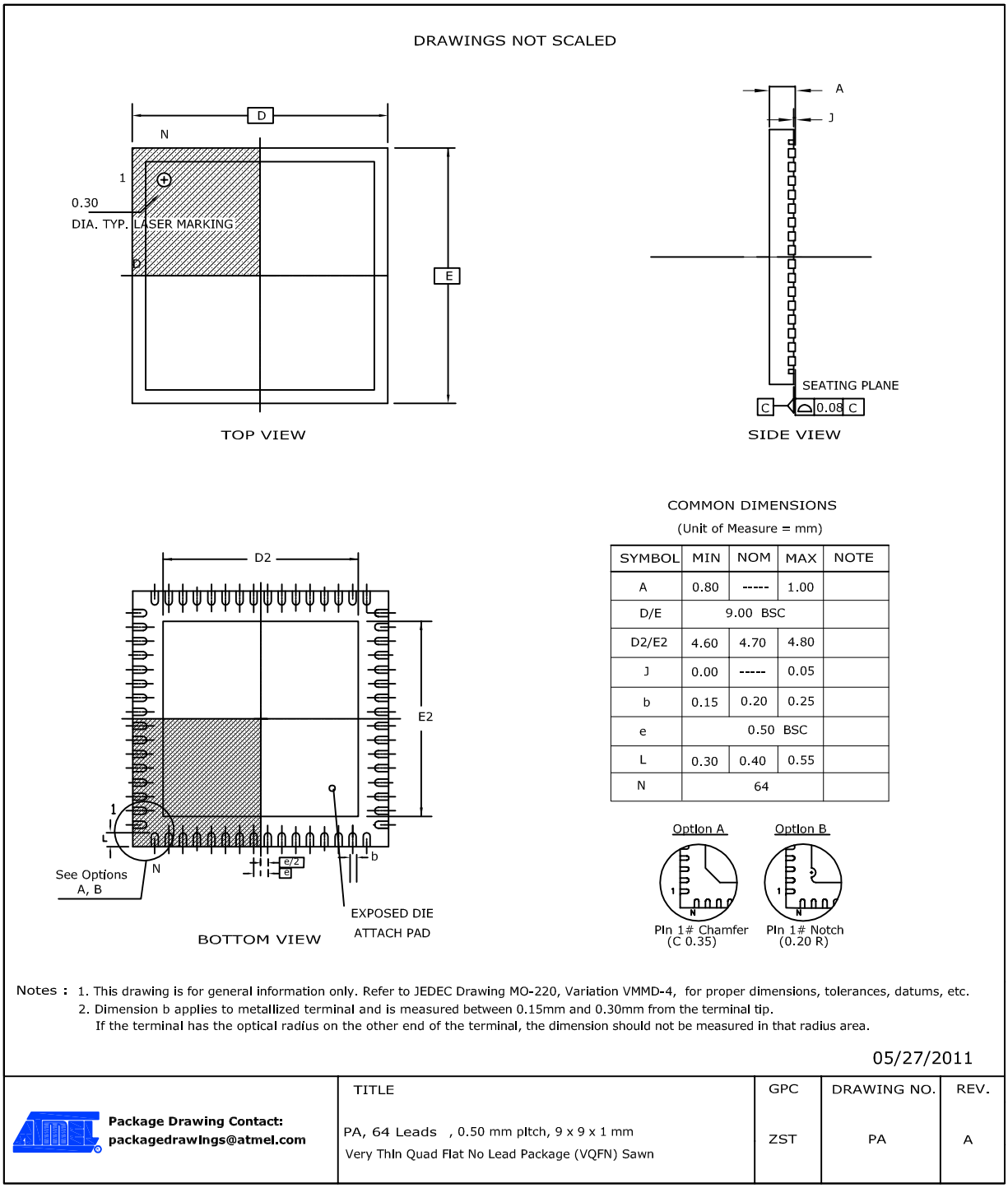
Table 8-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.2. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-5. Device and Package Maximum Weight

200	mg

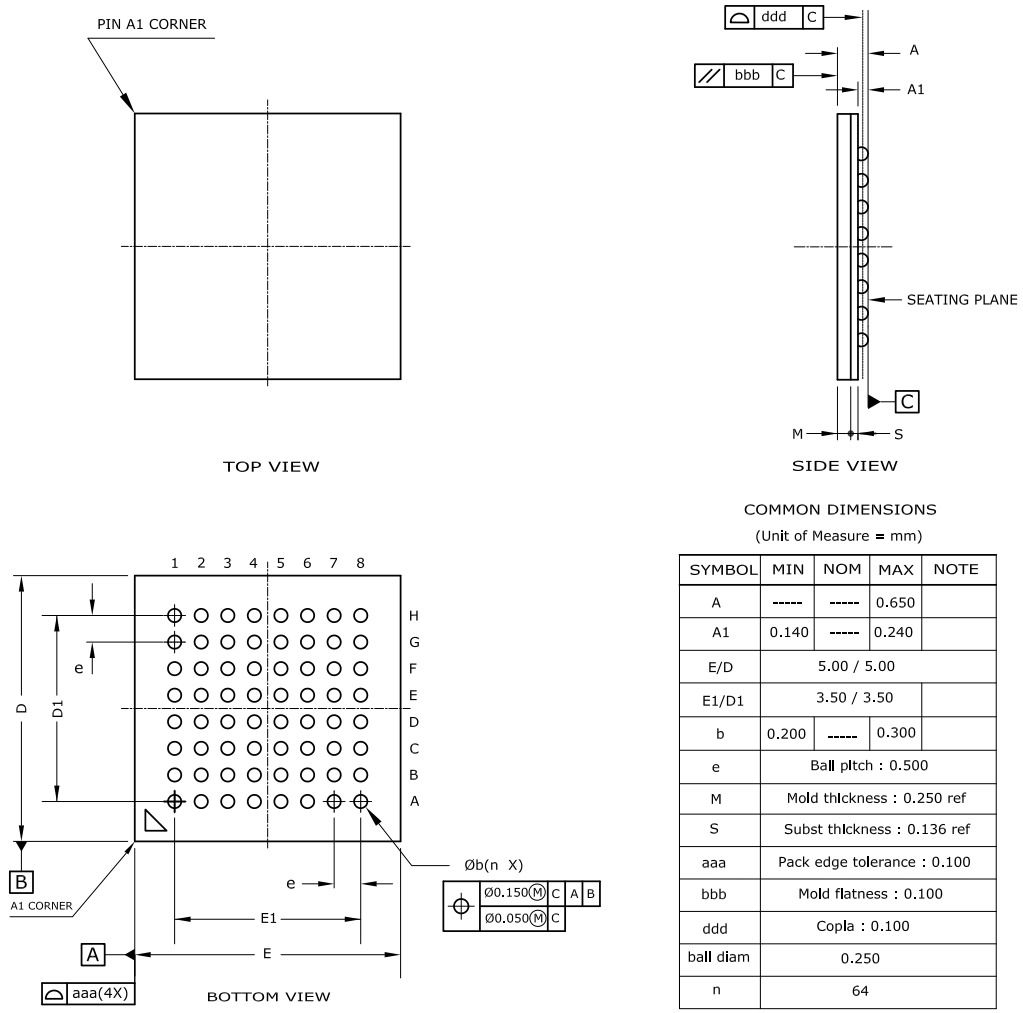
Table 8-6. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 8-7. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.3. 64-ball UFBGA



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	0.650	
A1	0.140	-----	0.240	
E/D	5.00 / 5.00			
E1/D1	3.50 / 3.50			
b	0.200	-----	0.300	
e	Ball pitch : 0.500			
M	Mold thickness : 0.250 ref			
S	Subst thickness : 0.136 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Copla : 0.100			
ball diam	0.250			
n	64			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 8-8. Device and Package Maximum Weight

27.4	mg

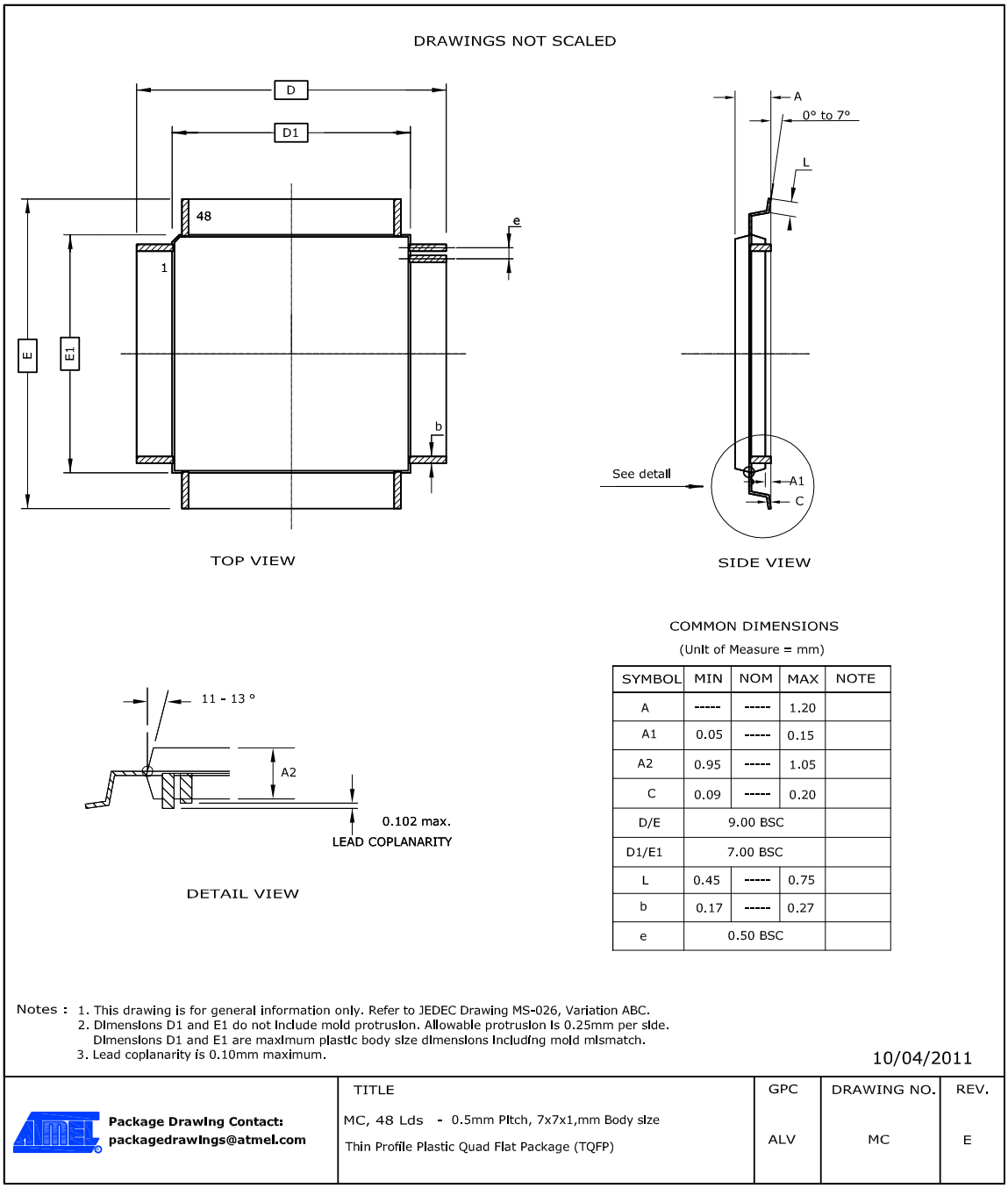
Table 8-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E8

8.2.4. 48 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		9.00 BSC		
D1/E1		7.00 BSC		
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e		0.50 BSC		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	ALV	MC	E

Table 8-11. Device and Package Maximum Weight

140	mg

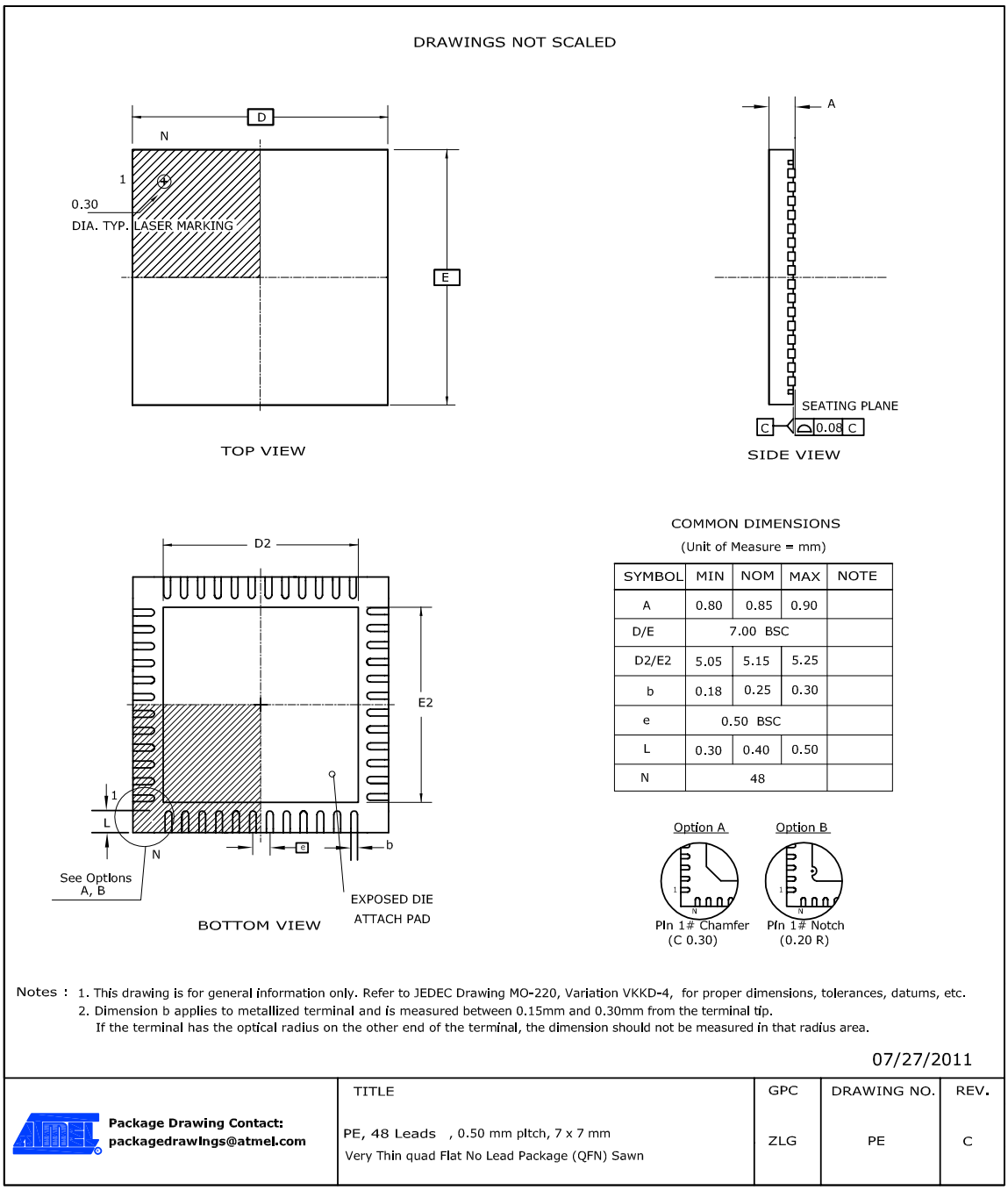
Table 8-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.5. 48 pin QFN



SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
D/E		7.00 BSC		
D2/E2	5.05	5.15	5.25	
b	0.18	0.25	0.30	
e		0.50 BSC		
L	0.30	0.40	0.50	
N		48		

Note: The exposed die attach pad is not connected electrically inside the device.

Table 8-14. Device and Package Maximum Weight

140	mg

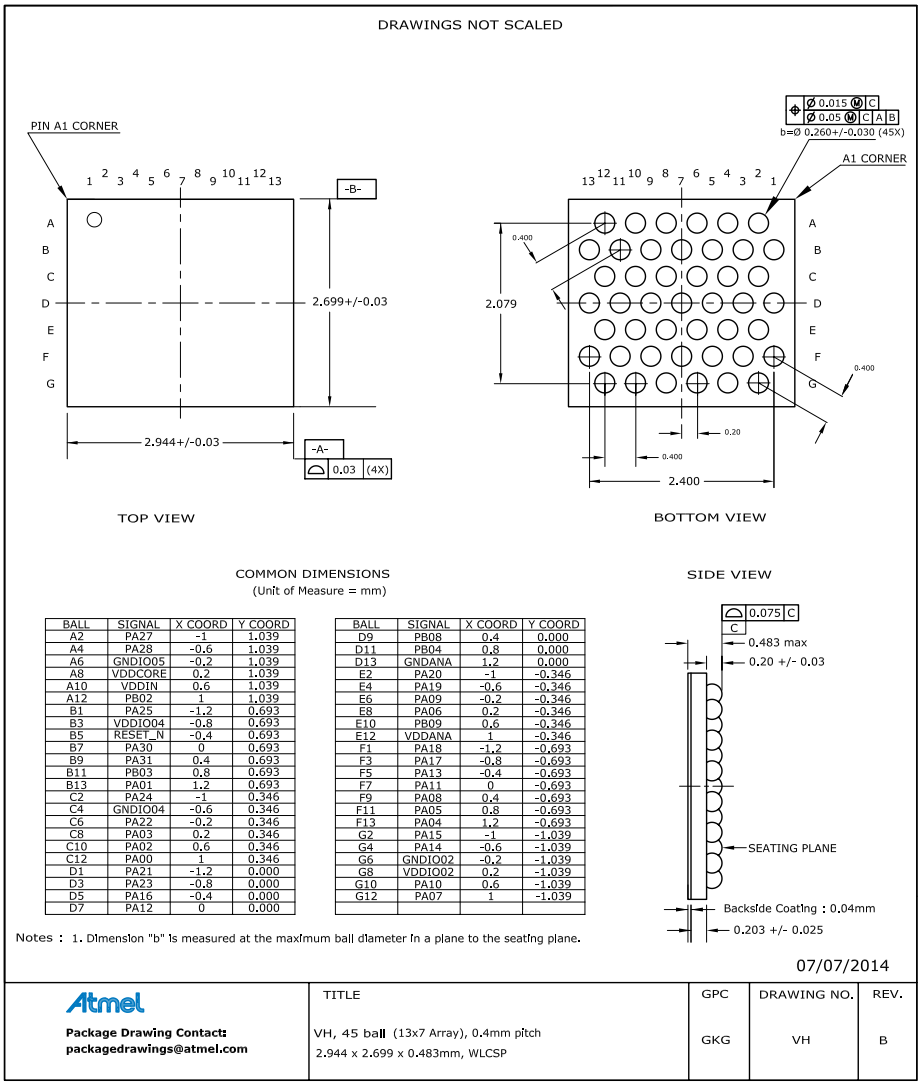
Table 8-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-16. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.6. 45-ball WLCSP



BALL	SIGNAL	X COORD	Y COORD
A2	PA27	-1	1.039
A4	PA28	-0.6	1.039
A6	GNDIO05	-0.2	1.039
A8	VDDCORE	0.2	1.039
A10	VDDIN	0.6	1.039
A12	PB02	1	1.039
B1	PA25	-1.2	0.693
B3	VDDIO04	-0.8	0.693
B5	RESET_N	-0.4	0.693
B7	PA30	0	0.693
B9	PA31	0.4	0.693
B11	PB03	0.8	0.693
B13	PA01	1.2	0.693
C2	PA24	-1	0.346
C4	GNDIO04	-0.6	0.346
C6	PA22	-0.2	0.346
C8	PA03	0.2	0.346
C10	PA02	0.6	0.346
C12	PA00	1	0.346
D1	PA21	-1.2	0.000
D3	PA23	-0.8	0.000
D5	PA16	-0.4	0.000
D7	PA12	0	0.000

BALL	SIGNAL	X COORD	Y COORD
D9	PB08	0.4	0.000
D11	PB04	0.8	0.000
D13	GNDANA	1.2	0.000
E2	PA20	-1	-0.346
E4	PA19	-0.6	-0.346
E6	PA09	-0.2	-0.346
E8	PA06	0.2	-0.346
E10	PB09	0.6	-0.346
E12	VDDANA	1	-0.346
F1	PA18	-1.2	-0.693
F3	PA17	-0.8	-0.693
F5	PA13	-0.4	-0.693
F7	PA11	0	-0.693
F9	PA08	0.4	-0.693
F11	PA05	0.8	-0.693
F13	PA04	1.2	-0.693
G2	PA15	-1	-1.039
G4	PA14	-0.6	-1.039
G6	GNDIO02	-0.2	-1.039
G8	VDDIO02	0.2	-1.039
G10	PA10	0.6	-1.039
G12	PA07	1	-1.039

Table 8-17. Device and Package Maximum Weight

7.3	mg

Table 8-18. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.2.7. 32 pin TQFP

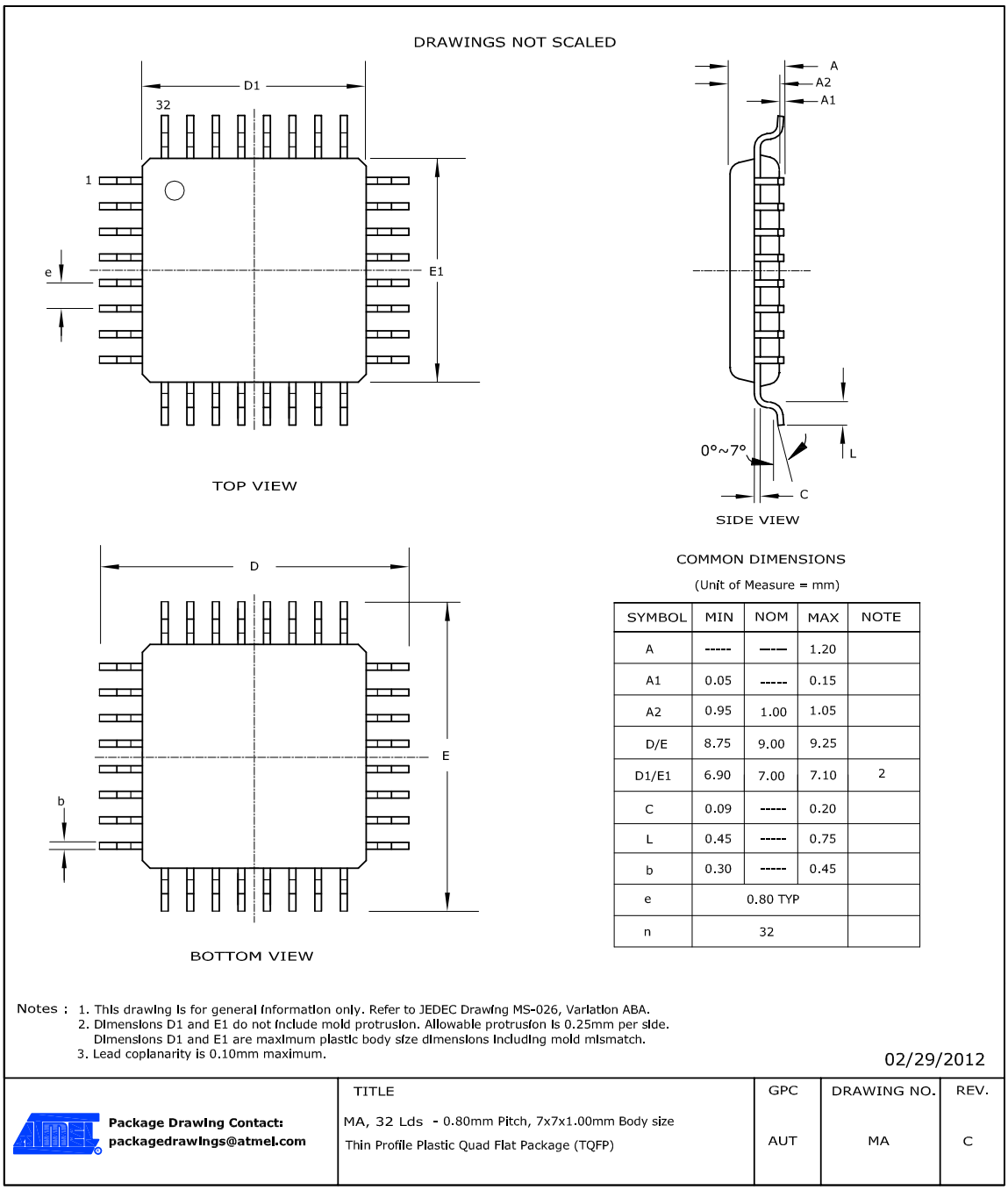


Table 8-20. Device and Package Maximum Weight

100	mg

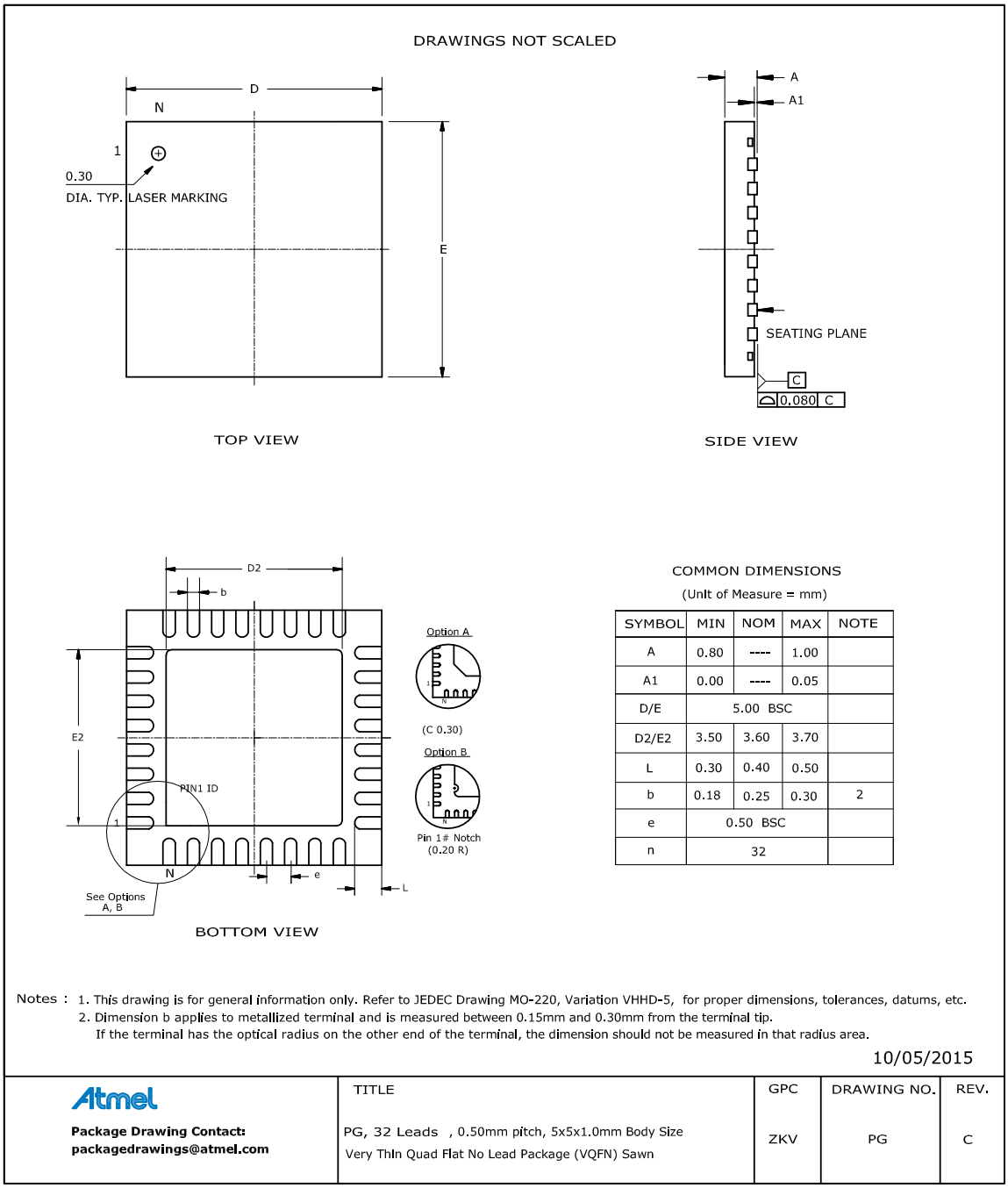
Table 8-21. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 8-22. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

8.2.8. 32 pin QFN



Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 8-23. Device and Package Maximum Weight

90	mg

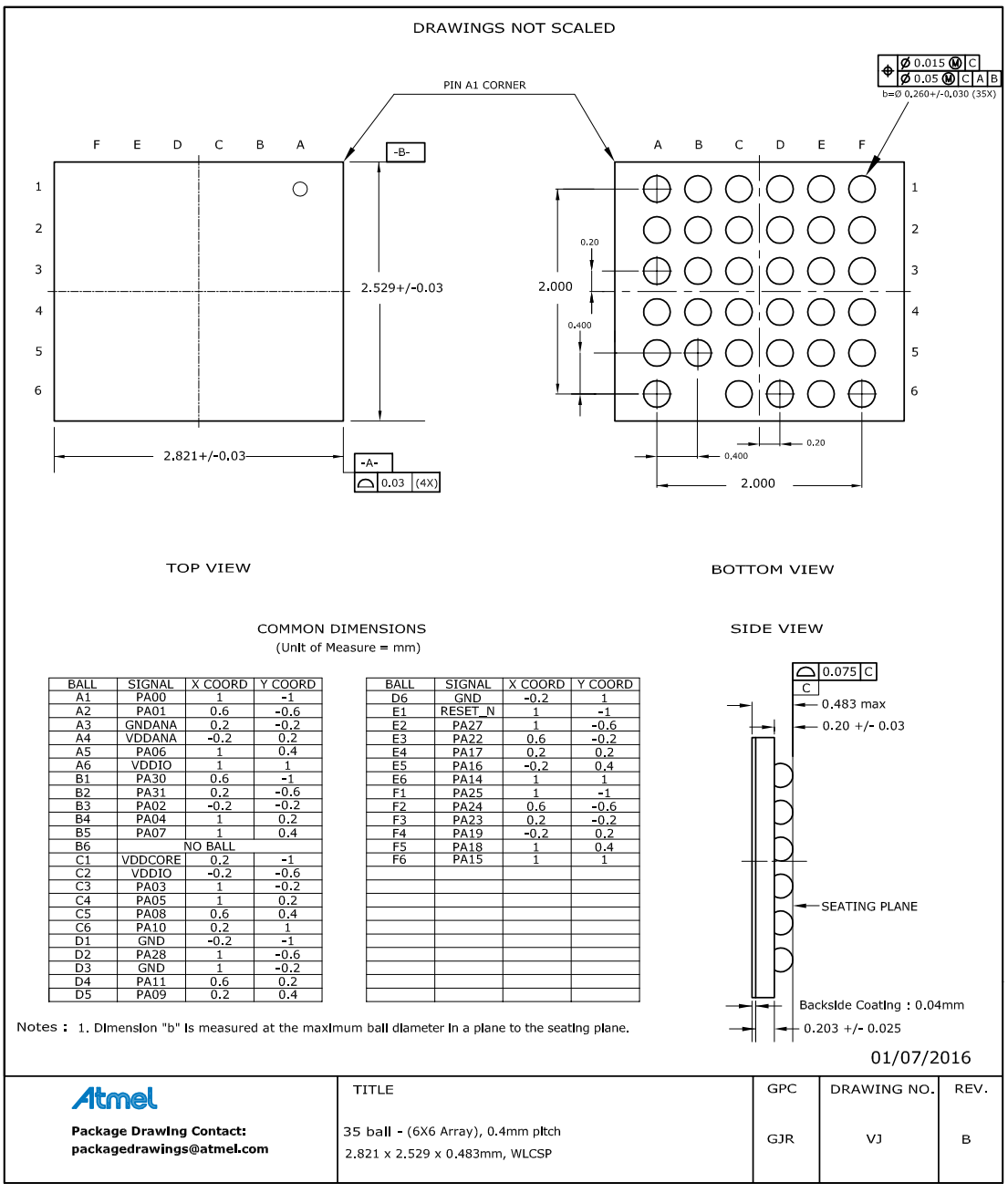
Table 8-24. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 8-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

8.2.9. 35 ball WLCSP (Device Variant B)



BALL	SIGNAL	X COORD	Y COORD
A1	PA00	1	-1
A2	PA01	0.6	-0.6
A3	GNDANA	0.2	-0.2
A4	VDDANA	-0.2	0.2
A5	PA06	1	0.4
A6	VDDIO	1	1
B1	PA30	0.6	-1
B2	PA31	0.2	-0.6
B3	PA02	-0.2	-0.2
B4	PA04	1	0.2
B5	PA07	1	0.4
B6	NO BALL		
C1	VDDCORE	0.2	-1
C2	VDDIO	-0.2	-0.6
C3	PA03	1	-0.2
C4	PA05	1	0.2
C5	PA08	0.6	0.4
C6	PA10	0.2	1
D1	GND	-0.2	-1
D2	PA28	1	-0.6
D3	GND	1	-0.2
D4	PA11	0.6	0.2
D5	PA09	0.2	0.4

BALL	SIGNAL	X COORD	Y COORD
D6	GND	-0.2	1
E1	RESET_N	1	-1
E2	PA27	1	-0.6
E3	PA22	0.6	-0.2
E4	PA17	0.2	0.2
E5	PA16	-0.2	0.4
E6	PA14	1	1
F1	PA25	1	-1
F2	PA24	0.6	-0.6
F3	PA23	0.2	-0.2
F4	PA19	-0.2	0.2
F5	PA18	1	0.4
F6	PA15	1	1

Table 8-26. Device and Package Maximum Weight

6.2	mg

Table 8-27. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 8-28. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E1

8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-29.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.

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