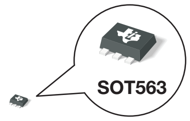


Easy-to-Use, Low-Power, 1°C, Low-Supply TEMPERATURE RANGE MONITOR in MicroPackage

Check for Samples: TMP303A, TMP303B

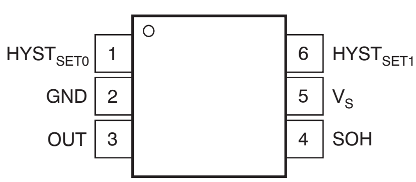
FEATURES

- **LOW POWER: 5μA (max)**
- **SOT563 PACKAGE: 1,6 x 1,6 x 0,6 mm**
- **TRIP POINT ACCURACY: ±0.2°C from –40°C to +125°C**
- **PUSH-PULL OUTPUT**
- **SELECTABLE HYSTERESIS: 1/2/5/10°C**
- **SUPPLY VOLTAGE RANGE: 1.4V to 3.6V**

APPLICATIONS

- **CELL PHONE HANDSETS**
- **PORTABLE MEDIA PLAYERS**
- **CONSUMER ELECTRONICS**
- **SERVERS**
- **POWER-SUPPLY SYSTEMS**
- **DC-DC MODULES**
- **THERMAL MONITORING**
- **ELECTRONIC PROTECTION SYSTEMS**

DRL PACKAGE
SOT563
(Top View)



DESCRIPTION

The TMP303A and TMP303B are temperature range monitors that offer design flexibility through an extra small footprint (SOT563), low power (5μA max) and low supply voltage capability (as low as 1.4V).

These devices require no additional components for operation; each can function independent of microprocessors or microcontrollers.

Trip points are preprogrammed at the factory. For applications that require different values, contact your local TI representative.

The OUT pin is a push-pull, active-high output. When the measured temperature is beyond the trip point range of 0°C to +60°C (TMP303A), and the Set Output High (SOH) pin is low, the OUT pin is high. The SOH pin is an input pin with an internal pulldown resistor. When the SOH pin is forced high, the OUT pin goes high regardless of the measured temperature.

TMP303A/B HYSTERESIS SETTINGS

$HYST_{SET1}$	$HYST_{SET0}$	HYSTERESIS (°C)
GND	GND	1
GND	V_S	2
V_S	GND	5
V_S	V_S	10

DEVICE SUMMARY

DEVICE	TRIP POINTS (°C)
TMP303A	T_L = 0, T_H = +60(1)
TMP303B	T_L = 0, T_H = +55(1)

(1) Contact TI representative for other trip points.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING
TMP303A	SOT563	DRL	OCO
TMP303B			QWM

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		TMP303A, TMP303B	UNIT
Supply Voltage, V_S – GND		+3.6	V
Input Pins, Voltage	SOH, $HYST_{SET1}$, $HYST_{SET0}$	–0.5 to V_S +0.5	V
Output Pin, Voltage	OUT	–0.5 to V_S +0.5	V
Output Pin, Current	OUT	8	mA
Operating Temperature Range		–55 to +130	°C
Storage Temperature Range		–60 to +150	°C
Junction Temperature (T_J max)		+150	°C
ESD Rating	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

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ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C and V_S = 1.4V to 3.6V, unless otherwise noted.

PARAMETER		CONDITIONS	TMP303A, TMP303B(1) MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT						
T_L, T_H Trip Point Accuracy(2)		T_A = +55°C to +60°C, V_S = 3.3V		±0.2	±1	°C
		T_A = 60°C, V_S = 1.4V to 3.6V		±0.2	±1.5	°C
vs. Supply				±0.1		°C/V
Hysteresis		See Hysteresis Settings table on front page	1		10	°C
HYSTERESIS SET INPUT						
Input Logic Levels:						
V_{IH}			0.7 × V_S		3.6	V
V_{IL}			–0.5		0.3 × V_S	V
Input Current:						
I_{IN}		0 < V_{IN} < 3.6V			1	μA
SOH INPUT						
Pulldown Resistor Value			80	100	120	kΩ
Input Logic Levels:						
V_{IH}			0.7 × V_S		3.6	V
V_{IL}			–0.5		0.3 × V_S	V
Input Current		V_{IN} = 3.6V		36		μA
OUTPUT						
Output Logic Levels						
V_{OH}		V_S > 2V, I_{OH} = 0.5mA	V_S – 0.4		V_S	V
		V_S < 2V, I_{OH} = 0.5mA	V_S – 0.2 × (V_S)		V_S	V
V_{OL}		V_S > 2V, I_{OL} = 1mA	0		0.4	V
		V_S < 2V, I_{OL} = 1mA	0		0.2 × V_S	V
POWER SUPPLY						
Specified Supply Voltage Range	V_S		1.4		3.6	V
Power-up Start-up Time		V_S > 1.4V	20	28	35	ms
Quiescent Current	I_Q	T_A = –55°C to +60°C		3.5	5	μA
		T_A = –40°C to +125°C		4	8	μA
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+130	°C
Thermal Resistance, DRL	θ_{JA}	JEDEC Low-K Board		260		°C/W

(1) 100% of all units are production tested at T_A = +25°C. Over temperature specifications are specified by design.
(2) T_L, T_H are device-specific. For example, TMP303A T_L = 0°C, T_H = 60°C; TMP303B T_L = 0°C, T_H = 55°C

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TYPICAL CHARACTERISTICS

At V_S = +3.3V and T_A = +25°C, unless otherwise noted.

TRIP ACCURACY ERROR vs TEMPERATURE

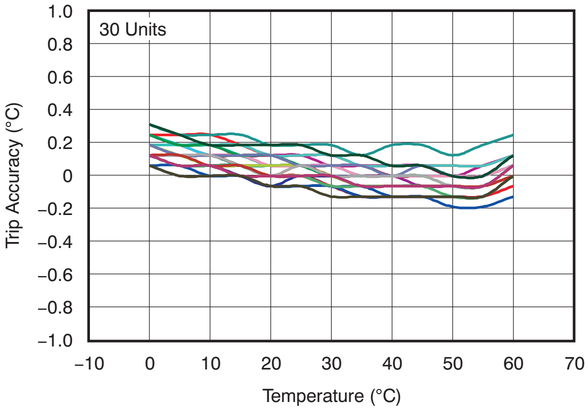

Figure 1.

QUIESCENT CURRENT vs TEMPERATURE

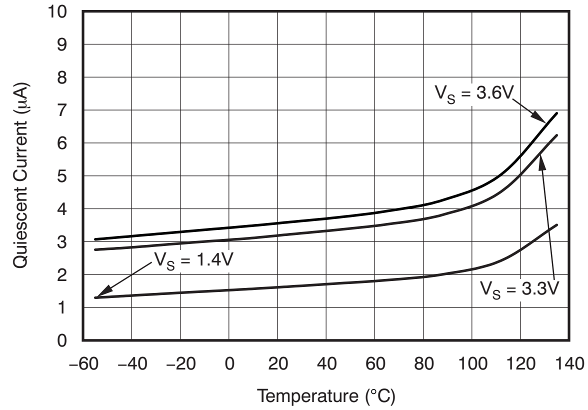

Figure 2.

TEMPERATURE STEP RESPONSE IN PERFLUORINATED FLUID AT +100°C vs TIME

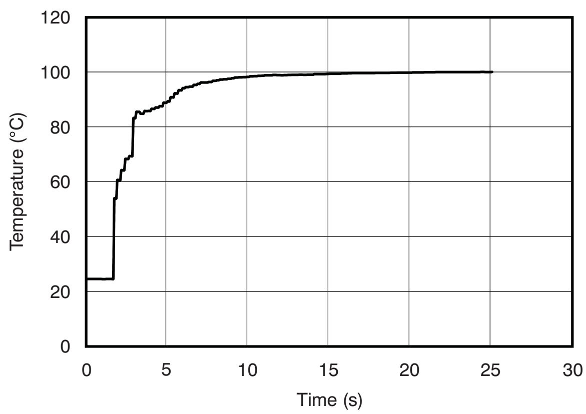

Figure 3.

THERMAL STEP RESPONSE IN AIR AT +100°C vs TIME

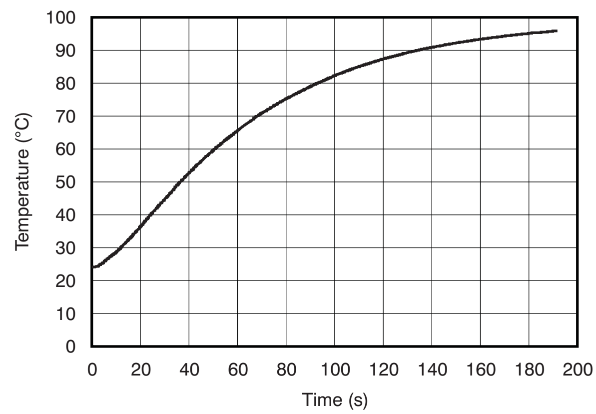

Figure 4.

TRIP THRESHOLD ACCURACY

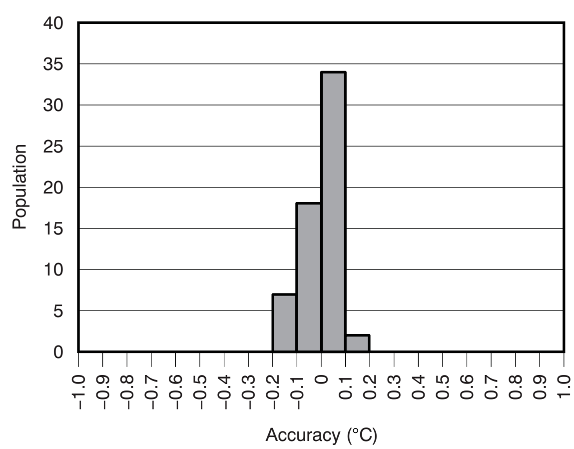

Figure 5.

POWER-UP AND POWER-DOWN TRANSIENT RESPONSE

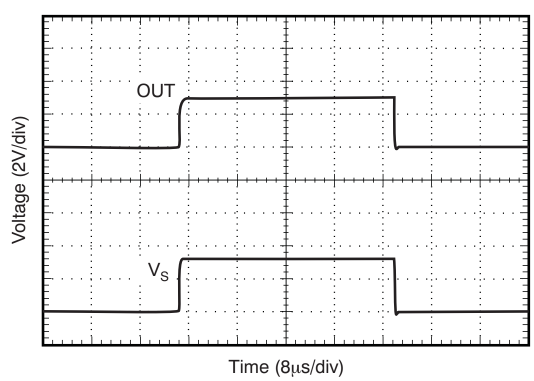

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At V_S = +3.3V and T_A = +25°C, unless otherwise noted.

POWER-UP, TRIP, AND POWER-DOWN RESPONSE

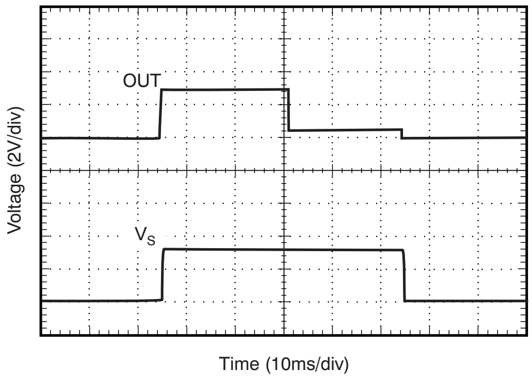

Figure 7.

OUTPUT LOGIC LEVEL LOW vs TEMPERATURE

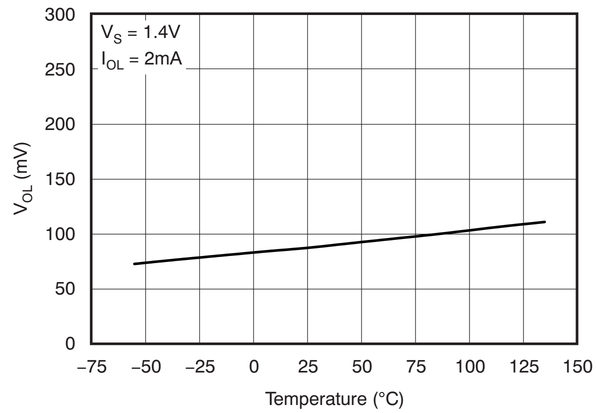

Figure 8.

OUTPUT LOGIC LEVEL HIGH vs TEMPERATURE

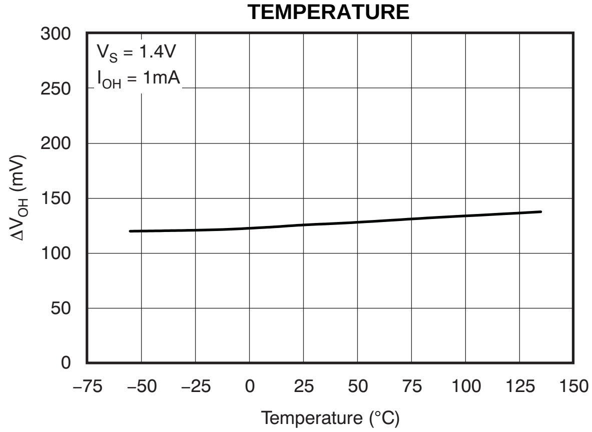

Figure 9.

APPLICATION INFORMATION

The TMP303A and TMP303B are temperature switches used in battery-powered applications that require accurate monitoring of a very specific temperature range of 0°C to +60°C (TMP303A) or 0°C to +55°C (TMP303B). This functionality is accomplished through the preset trip window and two hysteresis bits, $HYST_{SET0}$ and $HYST_{SET1}$. The preset trip window temperature thresholds are configured at the factory; for other trip points, contact a TI representative. Table 1 summarizes the bit setting versus hysteresis temperature window.

Table 1. Bit Setting vs Hysteresis Window

$HYST_{SET1}$	$HYST_{SET0}$	HYSTERESIS
GND	GND	1°C
GND	V_S	2°C
V_S	GND	5°C
V_S	V_S	10°C

Configuring the TMP303A/B

The TMP303A/B contains an active high, *push-pull* output stage and does not require a pull-up resistor to V_S for proper operation. Figure 10 shows a block diagram of the TMP303A/B.

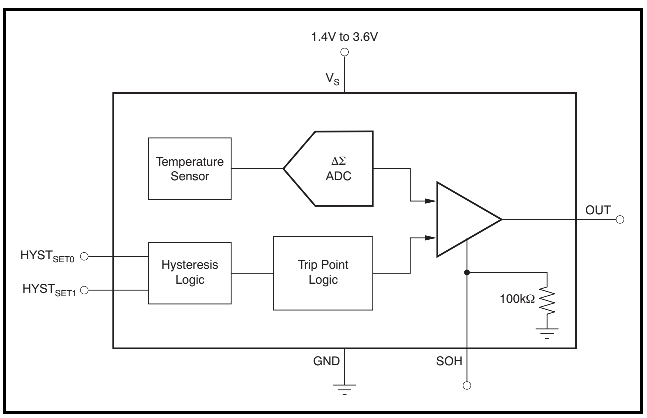

Figure 10. TMP303A/B Block Diagram

Power-supply bypassing is strongly recommended; use a 0.1µF capacitor placed as close as possible to the supply pin.

The TMP303A temperature trip window resides within the range of 0°C to 60°C. The TMP303B temperature trip window resides within the range of 0°C to 55°C. When either of these trip thresholds is crossed, the output (OUT) changes state from low to high. OUT does not return to its original low state until the temperature crosses the hysteresis threshold and returns within the range of the 0°C to 60°C (or 0°C to 55°C) window.

As an example, if the TMP303A is configured with a 10°C hysteresis window (that is, $HYST_{SET0}$ = $HYST_{SET1}$ = V_S), the output does not return to its low state until the temperature either crosses (T_L + *hysteresis*) = 10°C or (T_H – *hysteresis*) = 50°C. The Set Output High (SOH) pin is intended to add test functionality to verify the connectivity of the output (OUT) pin to the system controller or other temperature response system. The SOH pin is internally pulled down to ground with a 100kΩ resistor. If the SOH pin is grounded or left floating, it has no effect on the behavior of the TMP303A. If the SOH pin is pulled high, the TMP303A immediately forces the output high, regardless of temperature. It is very important to note that this response occurs even if the temperature falls within the 0°C to 60°C temperature window. Figure 11 illustrates this design in graphical form.

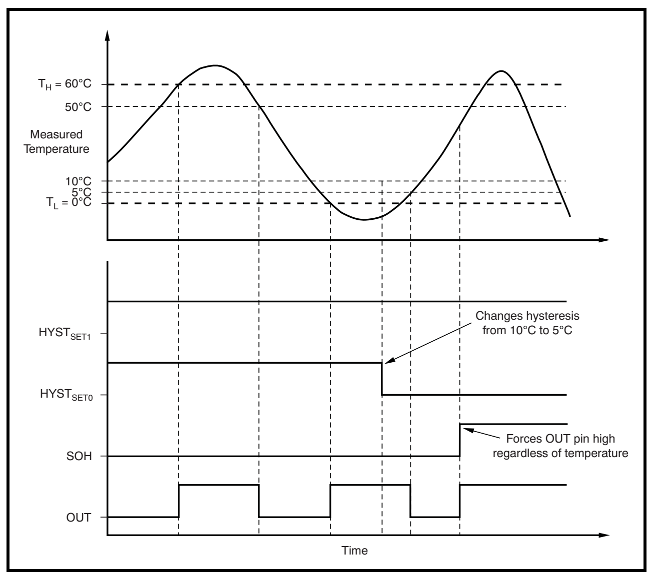

Figure 11. TMP303A Output Transfer Curves with Hysteresis Change from 10°C to 5°C and SOH Functionality

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TMP303A/B Power Up and Timing

At device power-up, the TMP303A/B exerts OUT = high, and typically requires 26ms to return to a low state only if the temperature falls within the hysteresis window set by $HYST_{SET0}$ and $HYST_{SET1}$.

The tolerance of the thermal response time is largely a result of the differences in conversion time, which varies between 20ms and 35ms; likewise, this conversion does not take place after a power cycle until the supply voltage has reached a level of at least 1.4V. This sequence is illustrated in Figure 12.

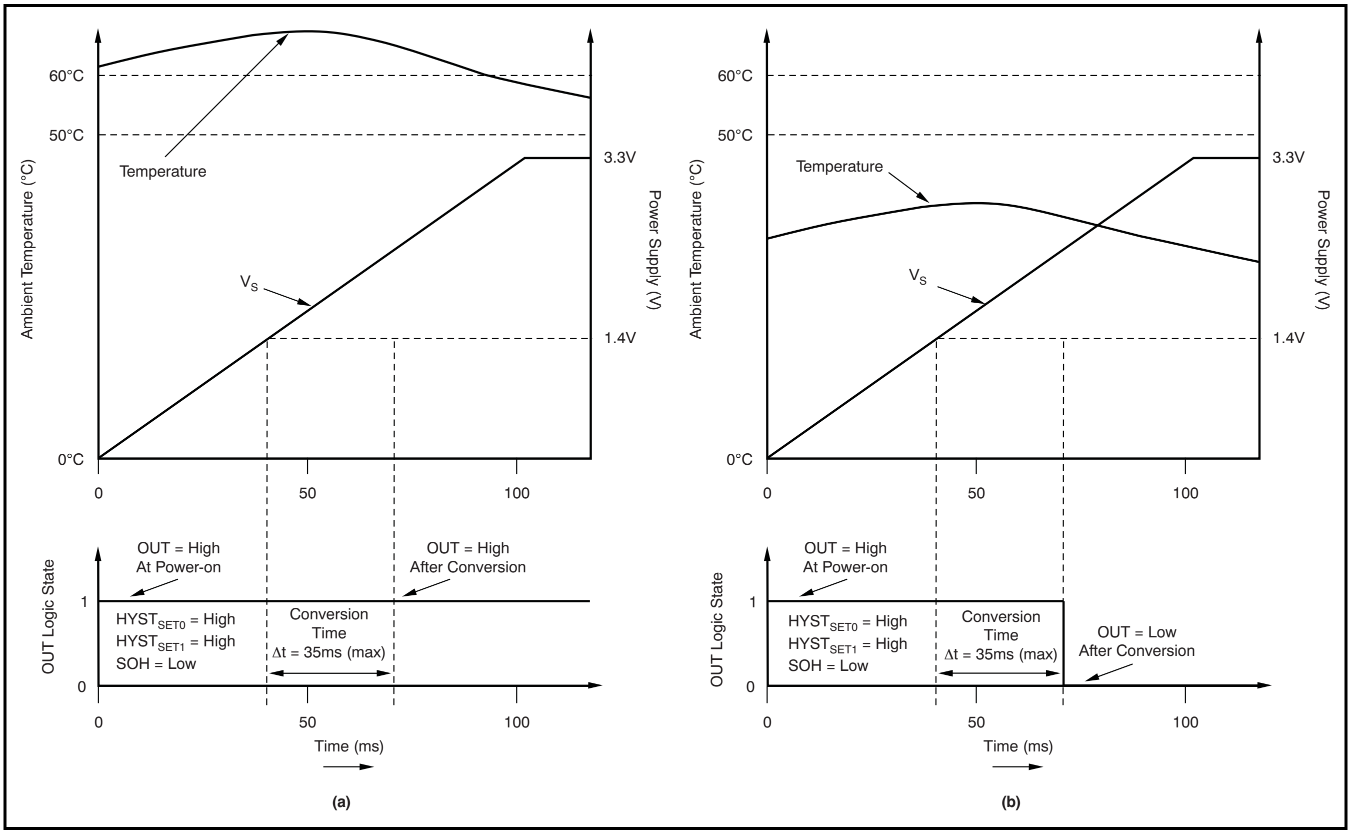

Figure 12. TMP303A Start-Up Delay vs. Output Voltage ($HYST_{SET0}$ = $HYST_{SET1}$ = V_S)

After the TMP303A/B powers up, all successive thermal response results for the device are achieved in a time frame of 0.985s to 1s. This period is the minimum time frame required for the push-pull output (OUT) to change its state from high to low (or vice-versa) while the device is active.

A maximum low output voltage is defined as a voltage level equivalent to (0.2 × V_S); likewise, a minimum high output voltage is defined as (0.8 × V_S). The timing associated with start-up time and conversion is shown in Figure 13.

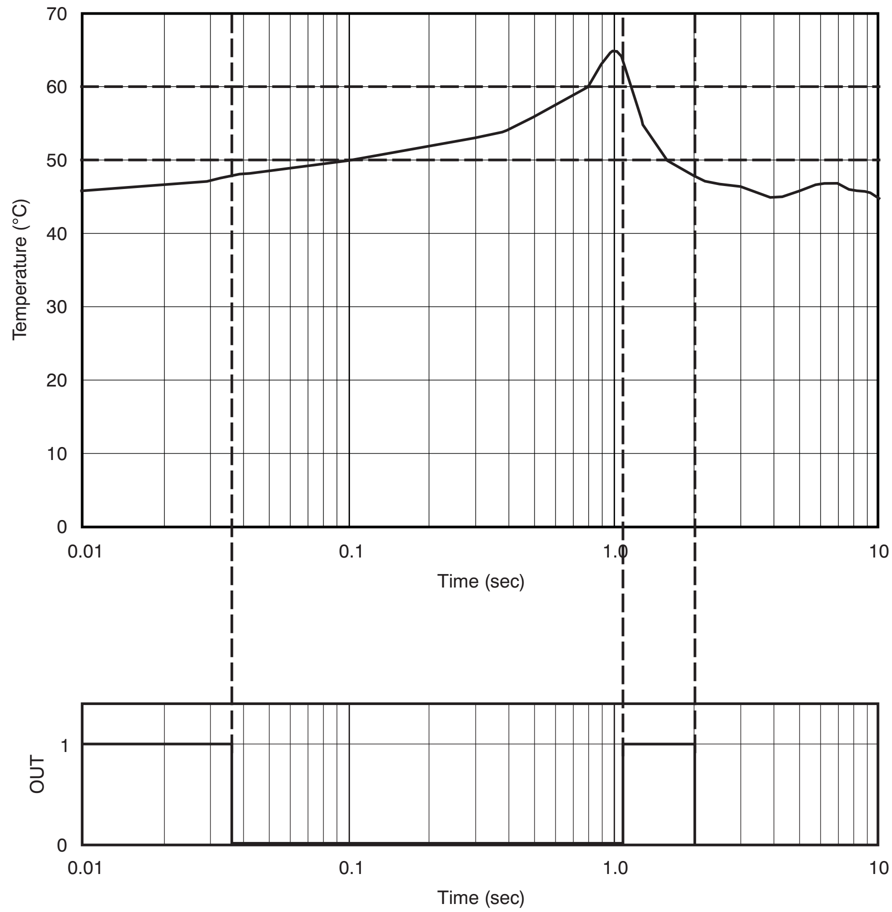

Figure 13. TMP303A Start-Up and Conversion Timing ($HYST_{SET0}$ = $HYST_{SET1}$ = V_S)

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2009) to Revision B **Page**

- Added TMP303B device to data sheet 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TMP303ADRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
TMP303ADRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
TMP303BDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
TMP303BDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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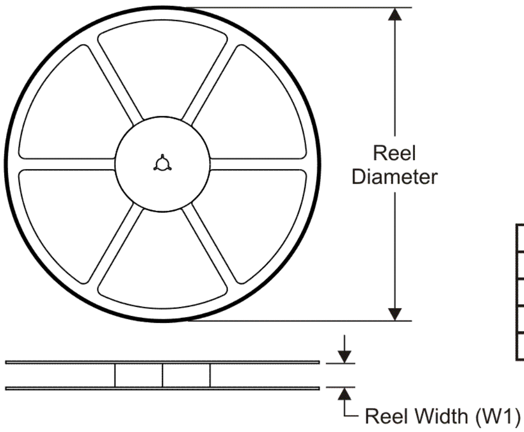
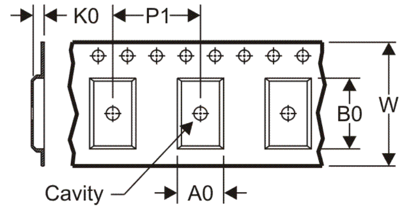
TAPE AND REEL INFORMATION

REEL DIMENSIONS

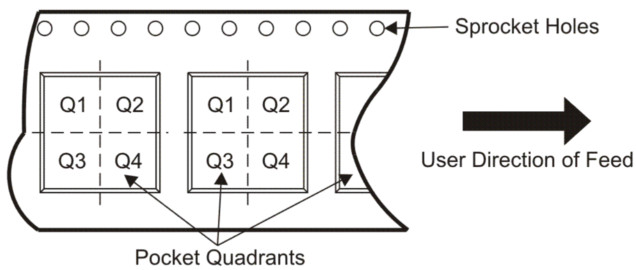


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

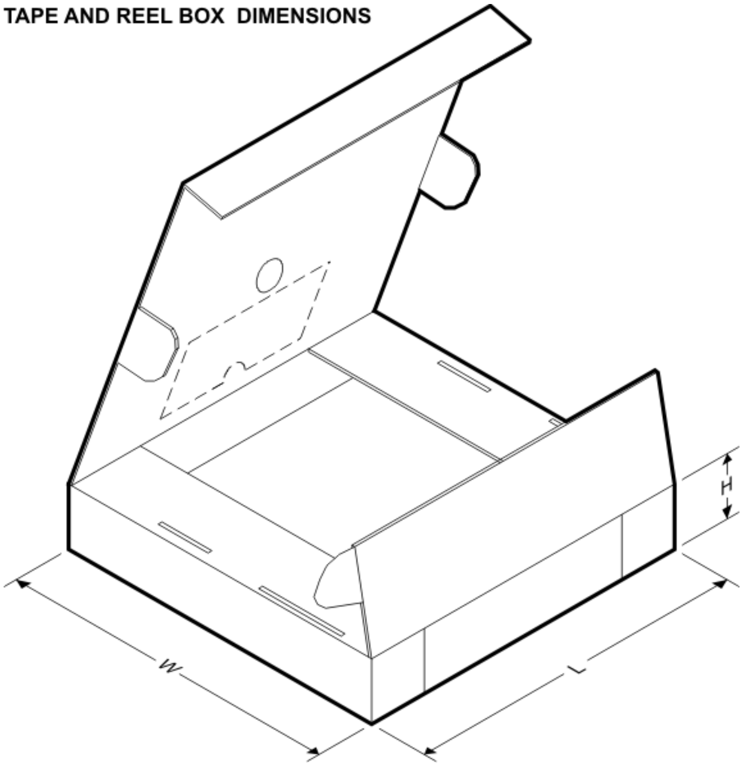
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

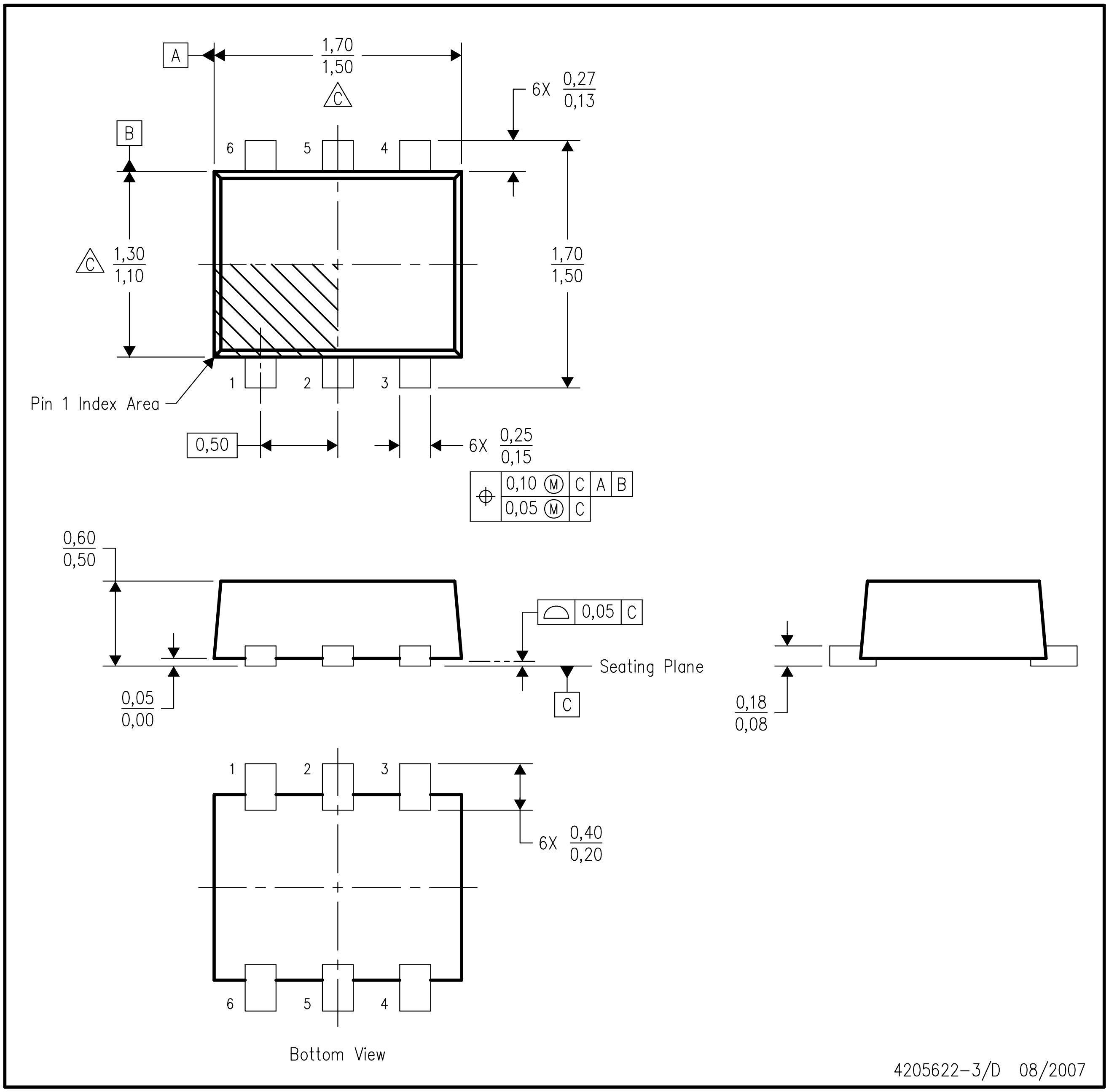
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP303ADRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP303ADRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP303BDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP303BDRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



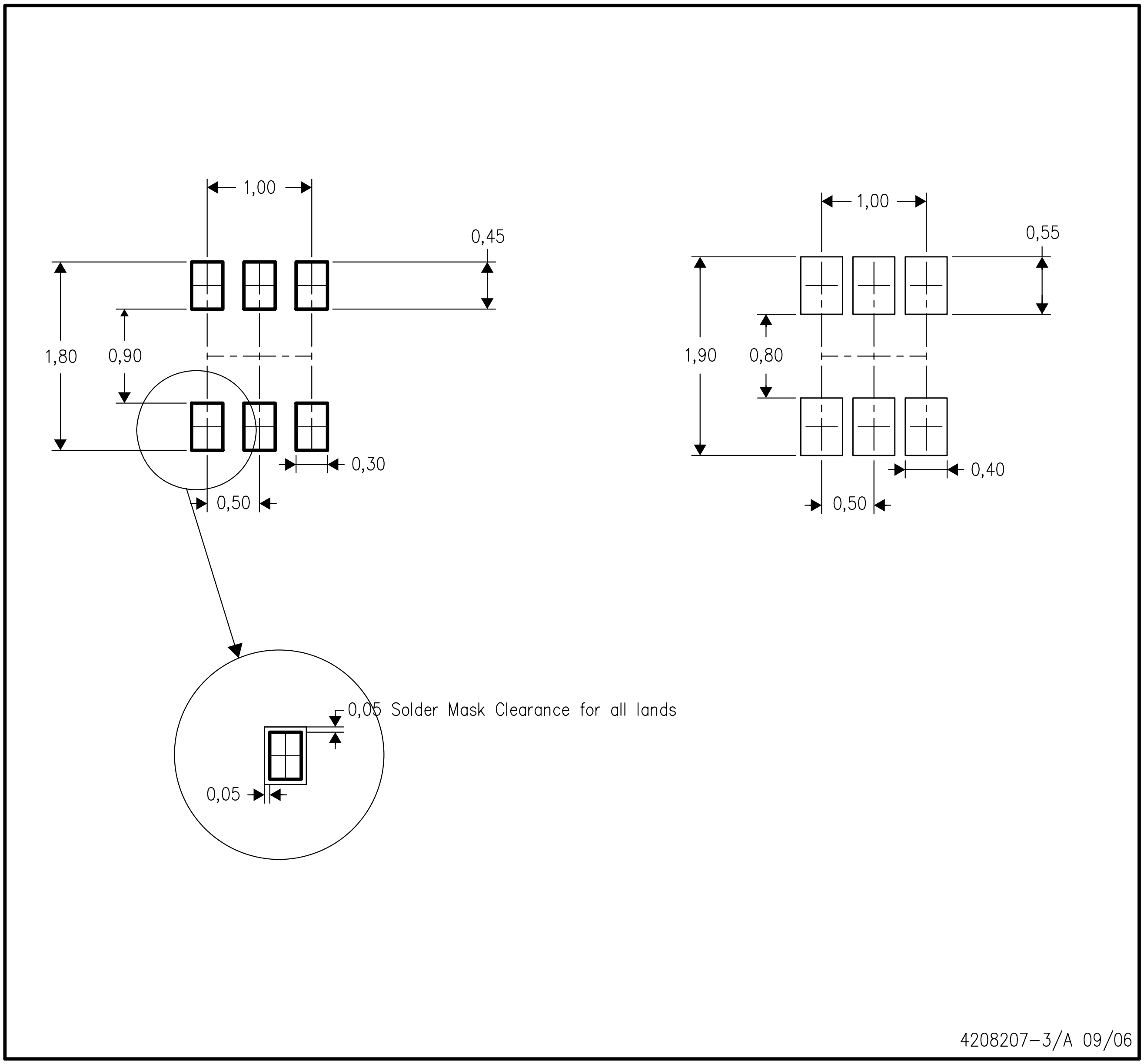
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP303ADRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP303ADRLT	SOT	DRL	6	250	202.0	201.0	28.0
TMP303BDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP303BDRLT	SOT	DRL	6	250	202.0	201.0	28.0



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N6)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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