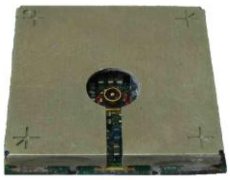
Fully Integrated GPS Receiver

ORG1408 Data Sheet



1. Introduction

ORG1408 GPS receiver module of ORG14XX series has been designed to address markets where stand alone operation, high level of integration, power consumption and design flexibility are very important.

ORG1408 GPS receiver module is a successor of the OriginGPS ORG1308 module.

Featuring OriginGPS proprietary Noise-Free Zone System™ technology the ORG1408 module offers the ultimate in high sensitivity GPS performance combined with high immunity.

The ORG14XX series module is miniature multi-channel receiver that continuously tracks all satellites in view and provides accurate positioning data in industry's standard NMEA-0183 format.

The ORG14XX series module is complete SiP (System-in-Package) featuring advanced miniature packaging technology and an ultra small footprint designed to commit unique integration features for high volume, low power and cost sensitive applications.

The ORG14XX series module incorporates new SiRFstarIV™ GPS processor.

Internal ARM CPU core and sophisticated firmware keep GPS payload off the host and allow integration in low resources embedded solutions.

The revolutionary SiRFstarIV™ architecture is optimized for how people really use location-aware products: often indoors with periods of unobstructed sky view when moving from place to place.

This new architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and ephemeris data while consuming mere microwatts of battery power.

2. Description

OriginGPS has researched and enhanced the performance of standard GPS receivers in real life applications.
Case study of the specifications of key components through involvement in R&D effort of major vendors derived in highest performance in industry's smallest footprint parts available.
These carefully selected key components resulted in higher sensitivity, faster position fix, navigation stability and operation robustness under rapid environmental changes creating hard-to-achieve laboratory performance in heavy-duty environment.

2.1 Features

- Stand alone operation
- OriginGPS Noise Free Zone System (NFZ™) technology
- Integrated SAW Filter, Voltage Regulator, I/O Buffers, TCXO and RTC
- 50Ω antenna input through miniature coaxial connector
- Active or passive antenna support
- SiRFstarIV™ GSD4e GPS processor
- L1 (1575MHz) frequency, C/A code
- 48 track verification channels
- Navigation sensitivity: -160dBm
- Tracking sensitivity: -163dBm for indoor fixes
- Fast TTFF: < 35s under Cold Start conditions
  < 1s under Hot Start conditions
- Multipath mitigation and indoor tracking
- Active jammer remover: tracks up to 8 CW interferers and removes jammers up to 80dB-Hz
- SBAS (WAAS, EGNOS, MSAS) support[1]
- Almanac Based Positioning (ABP™)[1]
- Client Generated Extended Ephemeris (CGEE™) and Server Generated Extended Ephemeris (SGEE™) for very fast TTFFs are supported through SiRFInstantFix™ and SiRFInstantFixII™
- Assisted GPS (A-GPS) support
- Automatic and user programmable power saving scenarios: ATP™, PTF™, APM™
- SiRFAware™ Micro Power Mode (MPM™) support[1]
- Low power consumption: <10mW during ATP™
- ARM7 109MHz baseband CPU
- Smart sensor I^2C master interface[1]
- UART host interface, SPI optionally[2]
- Programmable UART protocol and messages rate
- Selectable NMEA or OSP (SiRF Binary) communication standards
- Single voltage supply: wide input range 2V - 6V with UVLO
- Separate antenna DC bias supply
- Small footprint: 17mm x 17mm
- Surface Mount Device (SMD)
- Industrial operating temperature range: -40^0 to 85^0C
- Pb-Free RoHS compliant

Notes:
1. Available in module with Premium firmware only
2. Different ordering codes for SPI

2.2 Architecture

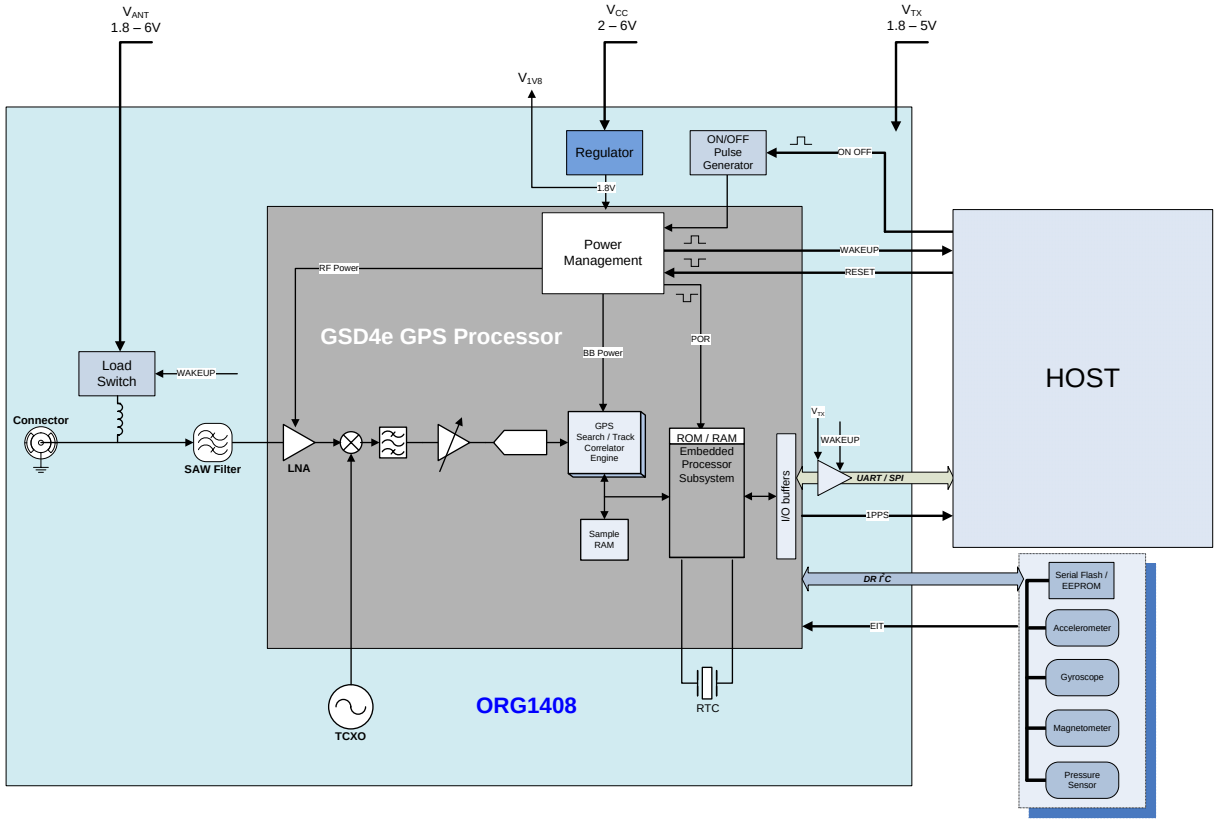


Figure 2-1: ORG1408 architecture

- **Antenna Connector**
  Signals at 1575 MHz from the GPS satellites are being delivered from receiving antenna through W.FL® standard miniature coaxial connector.
- **Load Switch**
  Load switch provides control over DC bias voltage supply for active antenna. When module is in Hibernate state no voltage is being supplied to antenna, thereby saving power.
- **Band-Pass SAW Filter**
  Band-pass SAW filter eliminates inter-modulated out-of-band signals that may corrupt GPS receiver performance.
- **Voltage Regulator**
  Voltage regulator provides stable supply for GPS processor over wide input voltage range.
  The design of this section was optimized for low ripple, low quiescent current and high PSRR.
- **TCXO (Temperature Compensated Crystal Oscillator)**
  This highly stable 16.369 MHz oscillator controls the down conversion process in RF block of the GPS processor. Highest characteristics of this component are important factors in sensitivity, fast TTFF and navigation stability.
- **RTC (Real Time Clock) crystal**
  This miniature component with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities.
- **RF Shield**
  RF enclosure avoids external interference to compromise sensitive circuitry inside the receiver. RF shield also blocks module's internal high frequency emissions from being radiated.

- **GSD4e IC**

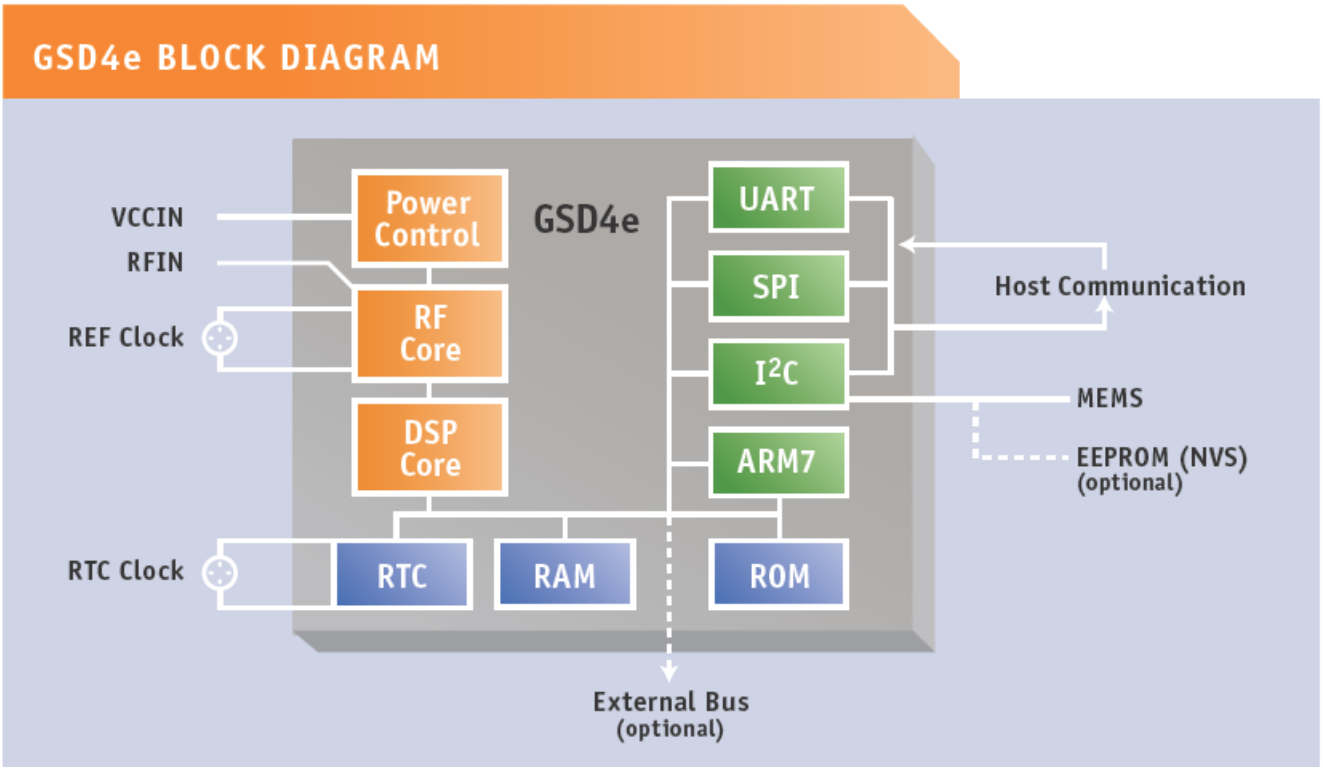


Figure 2-2: GSD4e functional block diagram

SiRFstarIV™ GSD4e is a navigation processor built on a low-power RF CMOS single-die, incorporating the baseband, integrated navigation solution software, ARM7 processor that form a complete stand alone or assisted-GPS engine.

SiRFstarIV™ GSD4e GPS processor includes the following units:

- GPS RF core incorporating LNA, down converter, fractional-N synthesizer and ADC block with selectable 2 and 4-bit quantization
- GPS DSP core incorporating more than twice the clock speed and more than double the RAM capacity relative to predecessor - market benchmarking SiRFStarIII™ GPS processor
- ARM7 microprocessor system incorporating 109MHz CPU and interrupt controller
- ROM block as code storage for PVT applications
- RAM block for data cache
- RTC block
- UART block
- SPI block
- Power control block for internal voltage domains management

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings are stress ratings only.

Stresses exceeding Absolute Maximum Ratings may damage the device.

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		V_{CC}	-	6.5	V
Antenna Supply Voltage		V_{ANT}	-	10	V
Antenna Supply Current		I_{ANT}	-	200	mA
TX Buffer Supply Voltage		V_{TX}	-	5.5	V
TX Buffer Source/Sink Current		I_{TX}	-10	10	mA
I/O Voltage		V_{IO}	-0.3	3.6	V
I/O Source/Sink Current		I_{IO}	-2	2	mA
1.8V Source Current		I_{1V8}	-	20	mA
RF Input Power	f_{IN} = 1560MHz÷1590MHz	P_{RF_IN}	-	10	dBm
	f_{IN} <1560MHz, >1590MHz		-	15	dBm
ESD Rating	All pads	$V_{(ESD)}$	-2	2	kV
Power Dissipation		P_D	-	200	mW
Storage temperature		T_{ST}	-55	125	^{0}C
Lead temperature (10 sec. @ 1mm from case)		T_{LEAD}	-	260	^{0}C

Table 3-1: Absolute maximum ratings

3.2 Recommended Operating Conditions

Functional operation above the Recommended Operating Conditions is not implied.
Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Parameter	Symbol	Mode / Pad	Test Conditions	Min	Typ	Max	Units
Power Supply Voltage	V_{CC}	V_{CC}		2.0	3.3	6.0	V
			V_{CC} falling		1.8	1.9	V
			V_{CC} rising		1.9	2.0	V
Power Supply Current (Without antenna supply current)	I_{CC}	Acquisition	-130dBm (Outdoor) V_{CC} = 2V T_{AMB} = 25^{0}C		33	43	mA
		Tracking		7		33	mA
		CPU only[1]			14		mA
		MPM™[2]			0.5		mA
		Standby[1]			0.1		mA
		Hibernate			30	50	µA
1.8V Output Voltage	V_{1V8}	V_{1V8}		1.77	1.80	1.83	V
1.8V Output Current	I_{1V8}	V_{1V8}				20	mA
TX Buffer Supply Voltage	V_{TX}	V_{TX}		1.80		5	V
TX Buffer Supply Current	I_{TX}	V_{TX}			1	10	mA
Antenna Supply Voltage	V_{ANT}	V_{ANT}		1.8		6.0	V
Antenna Supply Current	I_{ANT}	V_{ANT}				150	mA
Input Voltage Low State	V_{IL}	UART/SPI/GPIO				0.45	V
		ON_OFF				0.3	V
Input Voltage High State	V_{IH}	UART/SPI/GPIO		1.26		3.6	V
		ON_OFF		1.0		3.6	V
Output Voltage Low State	V_{OL}	UART/SPI/GPIO	I_{OL} = 4mA			0.4	V
Output Voltage High State	V_{OH}	UART	I_{OH} = -4mA	V_{TX}–0.4			V
		SPI / GPIO		1.35	1.71	1.8	V
Input Leakage Current	$I_{IN(leak)}$	UART/SPI/GPIO	V_{IN} = 1.8V or 0V	-10		10	µA
		ON_OFF	V_{IN} = 1.8V or 0V	-0.2		0.2	µA
Output Leakage Current	$I_{OUT(leak)}$	UART/SPI/GPIO	V_{IN} = 1.8V or 0V	-10		10	µA
Input Capacitance	C_{IN}	UART			4	10	pF
		SPI / GPIO			5		pF
Input Impedance	Z_{IN}	RF Input	f_0 = 1575.5 MHz		50		Ω
Input Return Loss	RL_{IN}				-8		dB
Operating Temperature[3]	T_{AMB}			-40	25	85	^{0}C
Relative Humidity	RH		-40^{0}C ≤T_{AMB}≤+85^{0}C	5		95	%

Table 3-2: Operating conditions

Notes:
1. Transitional states of ATP™ low power mode
2. Average current during SiRFAware™ Micro Power Mode
3. Operation below -30^{0}C to -40^{0}C is accepted, but TTFF may increase

4. Performance

4.1 Acquisition Times

TTFF (Time To First Fix) – is the period of time from GPS power-up till position estimation.

Hot Start

A hot start results from software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.
In this state, all of the critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

Warm Start

A warm start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in memory.
In this state, position and time data are present and valid, but ephemeris data validity has expired.

Cold Start

A cold start acquisition results when either position or time data is unknown.

Aided Start

Aiding is a method of effectively reducing the TTFF by making every start Hot or Warm.

	TTFF	Test Condition	Signal Level
Hot Start	< 1s	Outdoor	-130 dBm
Aided Start[1]	< 10s		
Warm Start	< 32s		
Cold Start	< 35s		
Signal Reacquisition	< 1s		

Table 4-1: Acquisition times

4.2 Sensitivity

	Signal Level
Tracking	-163 dBm
Navigation	-161 dBm
Aided[1]	-156 dBm
Cold Start	-148 dBm

Table 4-2: Sensitivity

Note:
1.Host-assisted device by SGEE™ or self-assisted by CGEE™ or Ephemeris Push

4.3 Power Consumption

Operation Mode	Power Consumption
Acquisition	66mW
Tracking	10-66mW
Hibernate	50µW

Table 4-3: Power consumption (without antenna)

4.4 Accuracy

		Method	Accuracy	Units	Test Conditions
Position	Horizontal	CEP (50%)	< 2.5	M	-130 dBm (Outdoor), Static
			< 2	M	-130 dBm (Outdoor), SBAS, Static
		2dRMS (95%)	< 5	M	-130 dBm (Outdoor), Static
			< 4	M	-130 dBm (Outdoor), SBAS, Static
	Vertical	VEP (50%)	< 4	M	-130 dBm (Outdoor), Static
			< 3	M	-130 dBm (Outdoor), SBAS, Static
		2dRMS (95%)	<7.5	m	-130 dBm (Outdoor), Static
			< 6	m	-130 dBm (Outdoor), SBAS, Static
Velocity	Horizontal	50%	< 0.01	m/s	-130 dBm (Outdoor), 30 m/s
Heading		50%	< 0.01	0	-130 dBm (Outdoor), 30 m/s
Time		1 PPS	< 1	µs	-130 dBm (Outdoor)

Table 4-4: Accuracy

4.5 Dynamic Constrains[1]

Velocity <	515 m/s	1,000 knots
Acceleration <	4g	
Altitude <	18,288 m	60,000 ft.

Table 4-5: Dynamic constrains

Note:
1. Standard dynamic constrains according to regulatory limitations

5. Power Management

5.1 Power States

Full Power state (Acquisition/Tracking)
The module stays in full power until a position solution is made and estimated to be reliable. During the acquisition, processing is more intense than during tracking, thus consuming more power.

CPU Only state
This is the state when the RF and DSP sections are partially powered off.
The state is entered when the satellites measurements have been acquired but the navigation solution still needs to be computed.

Standby state
This is the state when the RF and DSP sections are completely powered off and baseband clock is stopped.

Hibernate state
In this state the RF, DSP and baseband sections are completely powered off leaving only the RTC and Battery-Backed RAM running.
The module will perform Hot Start if held in Hibernate state less than 2 hours after valid position solution was acquired.

5.2 Power Saving Modes

The ORG14XX series module has three power management modes available in modules with Basic firmware – ATP™, APM™ and PTF™ and additional SiRFAware™ Micro Power Mode (MPM™) available in modules with Premium firmware, which are controlled by internal state machine. These modes provide different levels of power saving with different degradation level of position accuracy.

Adaptive Trickle Power (ATP™)

Adaptive Trickle Power (ATP™) is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
This power saving mode provides the most accurate position.
In ATP™ mode the ORG14XX module is intelligently cycled between Full Power, CPU Only and Standby states to optimize low power operation.

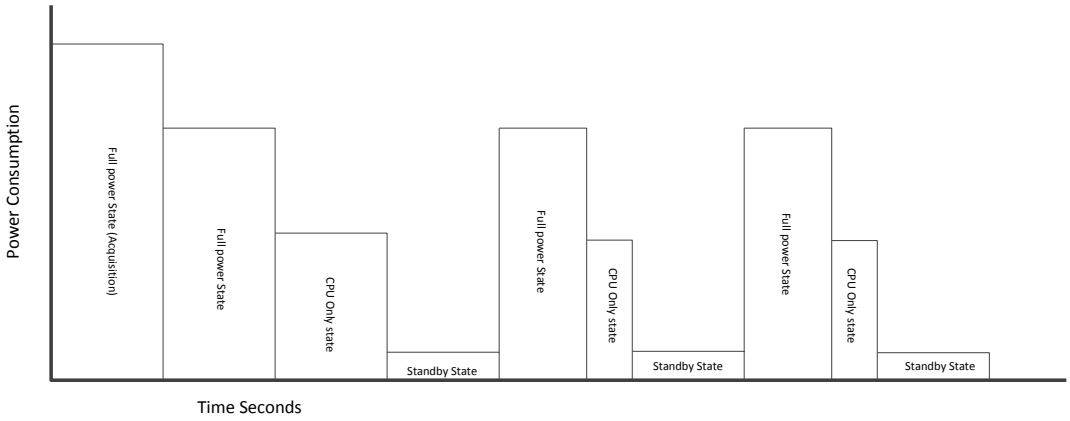


Figure 5-1: ATP™ timing

Push-to-Fix (PTF™)

Push-to-Fix (PTF™) is best suited for applications that require infrequent navigation solutions, optimizing battery life time.
In PTF™ mode the ORG14XX module is mostly in Hibernate state, waked up for Ephemeris and Almanac refresh in fixed periods of time.
The PTF™ period is 30 minutes by default but can be anywhere between 10 seconds and 2 hours. When the PTF mode is enabled the receiver will stay in Full Power state until the good navigation solution is computed.
When the application needs a position report it can toggle the ON_OFF pad to wake up the module. In this case, a new PTF™ cycle with default settings begins.

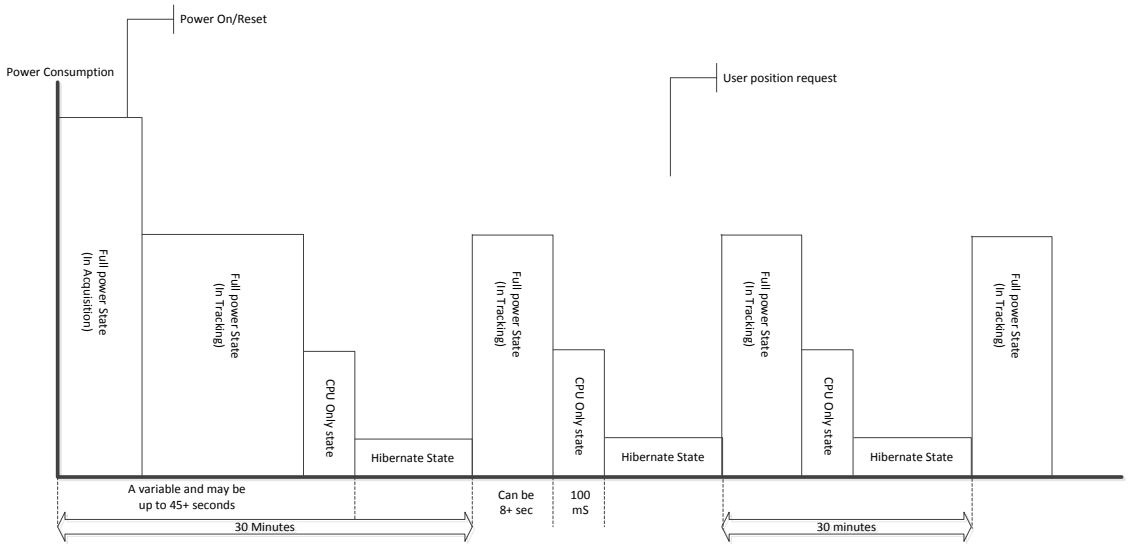


Figure 5-2: PTF™ timing

Advanced Power Management (APM™)

Advanced Power Management (APM™) is designed to give the user more options to configure the power management. The APM™ mode allows power savings while ensuring that the Quality of the Solution (QoS) in maintained when signals level drop.
In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving. The user may select between Duty Cycle Priority for more power saving and TBF (Time Between Fixes) Priority with defined or undefined maximum horizontal error.
TBF range is from 10 to 180 sec. between fixes, Power Duty Cycle range is between 5 to 100%.
Maximum position error is configurable between 1 to 160m.
The number of APM™ fixes is configurable up to 255 or set to continuous.
In APM™ mode the module is intelligently cycled between Full Power and Hibernate states.

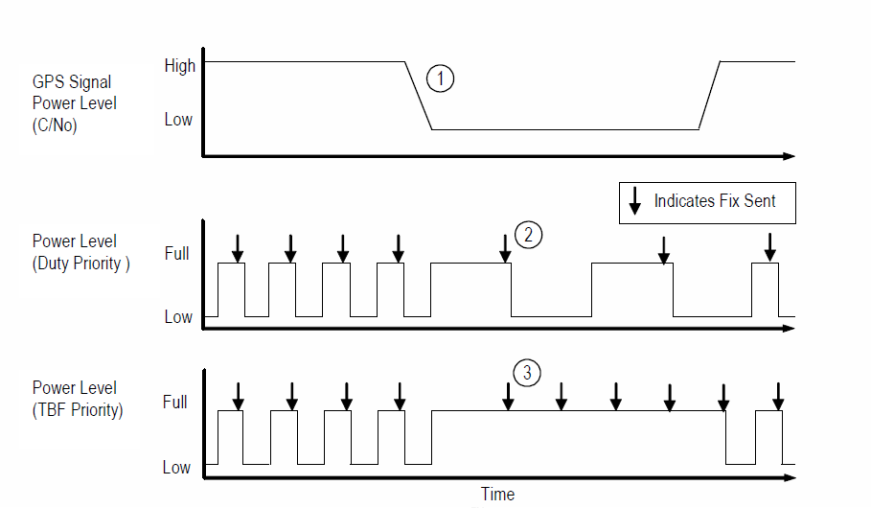


Figure 5-3: APM™ timing

1. GPS signal level drops (e.g user walks indoors)
2. Lower signal results in longer ON time. To maintain Duty Cucle, OFF time is increased.
3. Lower signal means missed fix. To maintain future TBFs, the module goes info Full Power state until signal levels improve.

SiRFAware™ Micro Power Mode (MPM™)[1]

With MPM™ SiRFAware™, the ORG14XX series module determines how much signal processing to do and how often to do it, so that the receiver is always able to do a fast hot start (TTFF < 2 s) on demand.

In this mode the receiver is configured to wake up (typically twice an hour) for 18-24 sec. to collect new Ephemeris data. Ephemeris Data Collection operation consumes the current equal to Full Power state.

Additionally, the module will wake up once every 1 to 10 min. for 250ms to update internal navigation state and GPS time calibration. Capture/Update operation consumes about 200µA.

Rest of the time the receiver remains in Hibernate state.

The host sends ON_OFF interrupt to wake up the module.

After valid fix is available, the host can turn the module back into MPM™ by re-sending the configuration message.

Average current consumption over long period during MPM™ is about 0.5mA.

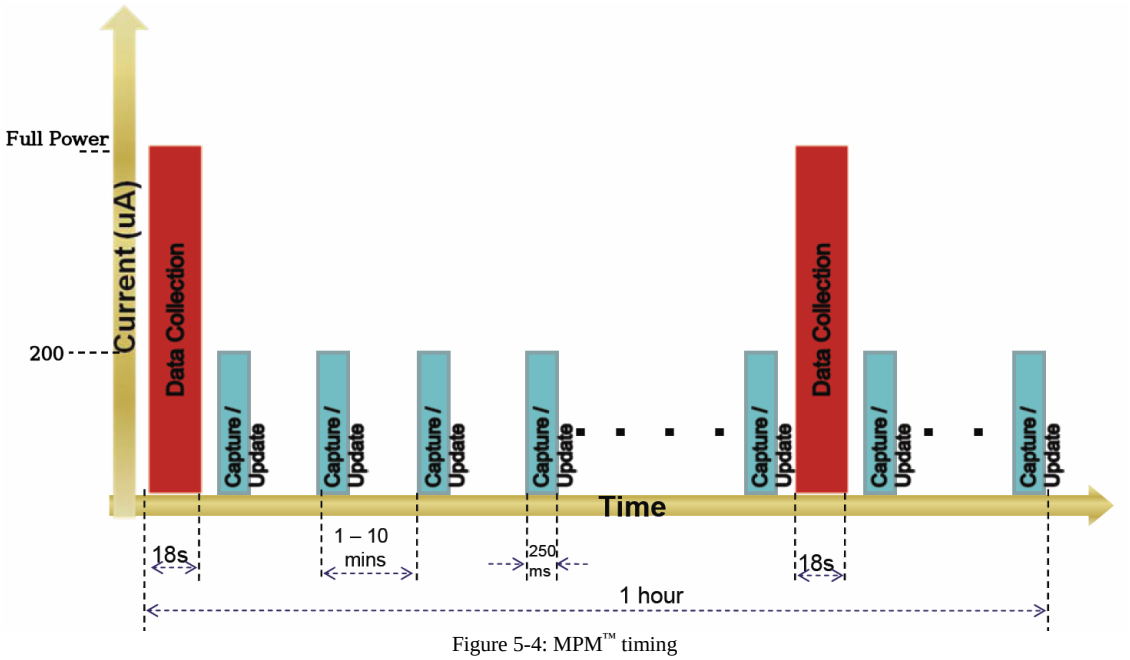


Figure 5-4: MPM™ timing

Note:
1. Not available in modules with Standard firmware

6. Extended Features

6.1 Almanac Based Positioning (ABP™)[1]

With ABP™ mode enabled, the user can get shorter Cold Start TTFF as a tradeoff with the position error.

When no sufficient Ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the SVs having their states derived from Almanac data.

Almanac data for ABP™ purposes may be stored factory set, broadcasted or pushed.

6.2 Active Jammer Remover

Jamming Remover is an embedded DSP block that detects, tracks and removes up to 8 Continuous Wave (CW) type signals of up to 80dB-Hz each.

Jamming Remover is effective only against continuous narrow band interference signals and covers GPS L1 1575Mhz frequency ±4MHz.

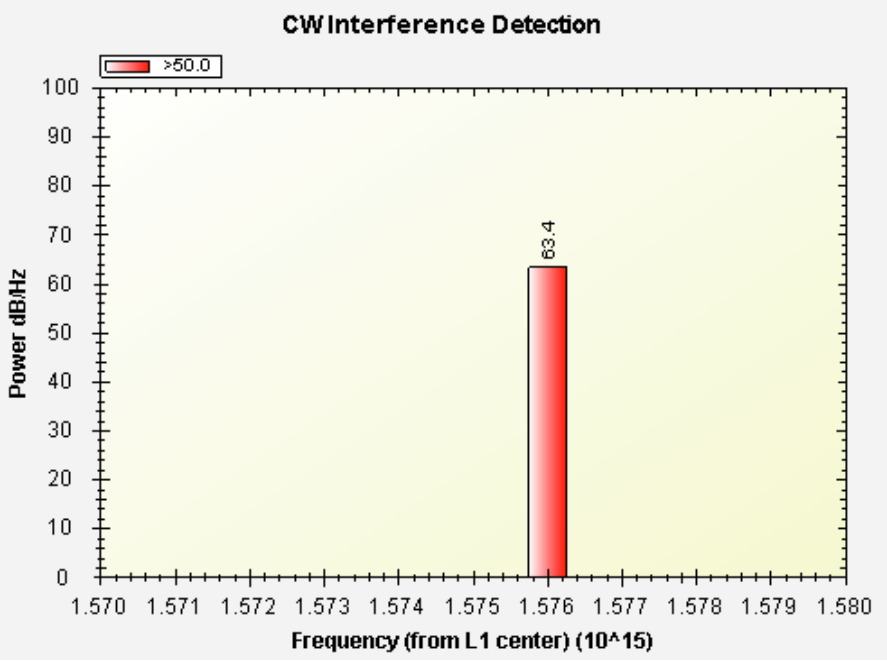


Figure 6-1: Active Jammer Detection frequency plot

6.3 Client Generated Extended Ephemeris (CGEE™)

The CGEE™ feature allows shorter TTFF by providing predicted (synthetic) ephemeris files created within a lost host system from previously received broadcast Ephemeris.

The prediction process requires good receipt of broadcast Ephemeris data for all satellites.

EE files created this way are good for up to 3 days and then expire.

The CGEE™ feature requires avoidance of power supply removal.

CGEE™ data files are stored on internal or external EEPROM or Serial Flash and managed by the receiver or storage and management is done by host.

Note:

1. Not available in modules with Standard firmware

7. Interface

7.1 Pad Assignment

Pad Number	Pad Name	Pad Description	Direction	Default	Notes
1	RX	UART Receive	Input	High	1.8 – 3.6V
2	TX	UART Transmit	Output	High	High state voltage level is set by V_{TX}
3	V_{TX}	TX Buffer Power	Power		1.8 – 5.0V
4	SCK	SPI Clock	Input	Low	1.8 – 3.6V
5	nSE	SPI Chip Select	Input	High	
6	SDO	SPI Data Out	Output	High	
7	V_{ANT}	Active Antenna Bias	Output		Leave floating for passive antenna
8	V_{CC}	System Power	Power		2 - 6V
9	V_{1V8}	1.8V Source	Power		Voltage source. Do not power this pad.
10	GND	System Ground	Power		
11	GND	System Ground	Power		
12	GND	System Ground	Power		
13	GND	System Ground	Power		
14	GND	System Ground	Power		
15	WAKEUP	Power Status	Output	Low	1.8V compatible
16	nRESET	Asynchronous Reset	Input	High	Do not drive
17	ON_OFF	Power State Control	Input	Low	1.8 – 3.6V
18	DR_SDA	Master I^2C SDA	Bi-dir	High	1.8V compatible
19	DR_SCL	Master I^2C SCL	Output	High	
20	EIT	External Interrupt	Input	High	1.8 – 3.6V
21	1PPS	UTC Time Mark	Output	Low	1.8V compatible
22	SDI	SPI Data In	Input	High	1.8 – 3.6V

Table 7-1: ORG1408 pin-out

7.2 Connectivity

7.2.1. Power

The ORG1408 module requires only one power source, which can be unregulated, i.e supplied directly from a battery, since the module has internal regulators.

Main power

V_{CC} power input is for main power supply. V_{CC} power supply range is 2 to 6V DC.
It is recommended to keep the V_{CC} power supply on all the time in order to maintain the non-volatile RTC and RAM active for fastest possible TTFF.
When the V_{CC} is powered off, settings are reset to factory default, and the receiver performs Cold Start on next power up.
Power supply current consumption varies according to the processor load and satellite acquisition.
Typical I_{CC} current is 33mA during acquisition. Peak I_{CC} current is 50 mA.
Typical I_{CC} current in Hibernate state is 50µA.
Voltage ripple below 50mV_{P-P} allowed for frequency between 100KHz and 3MHz.
Voltage ripple below 15mV_{P-P} allowed for frequency above 3MHz.
Higher voltage ripple may compromise the ORG1408 module performance.

TX power

V_{TX} power input is for integrated data output level shifter between 1.8V GPS processor domain and host.
V_{TX} power supply range is 1.8 to 3.6V DC according to required TX output voltage swing.
Typical I_{TX} current is 1mA and varies with input load of host.
V_{TX} may be externally connected to V_{CC}, while module and host I/O are in same voltage domain.
V_{TX} may be externally connected to V_{1V8}, while host I/O is in 1.8V voltage domain.
Data output level shifter is internally controlled by GPS processor and automatically turned off during low power states.

Antenna power

V_{ANT} power input is for active antenna bias through integrated low-loss load switch.
V_{ANT} power supply range is 1.8 to 10V DC according to antenna DC requirements.
Maximum I_{ANT} current is 150mA.
Load switch is internally controlled by GPS processor and antenna bias automatically turned off during low power states.
V_{ANT} may be externally connected to V_{CC}, while module and antenna are in same voltage domain.
When using passive antenna, do not apply voltage on this input.

1.8V power source

V_{1V8} power supply provides regulated 1.8V voltage source for peripheral components, like MEMS sensors connected to DR I^2C bus.
Maximum I_{1V8} continuous output current is 20mA.

Ground

Single Ground pad should be connected to the main Ground with shortest possible trace or via.

7.2.2. Host Control Interface

ON OFF input

The ON_OFF control input is used to switch the receiver between different power states.

- If the system is in Hibernate state, an ON_OFF pulse will move to Full Power mode
- If the system is in ATP™ mode, an ON_OFF pulse will move it to Full Power mode.
- If the system is in PTF™ mode, an ON_OFF pulse will initiate one PTF™ cycle.
- If the system is already in Full Power mode, an ON_OFF pulse will initiate orderly shutdown.

ON_OFF pulse requires a rising edge and high level that persists for at least 100µs in order to be detected. Resetting the ON_OFF detector requires that ON_OFF go to logic low at least 100µs.
Recommended low-high-low pulse length is 100ms.
ON_OFF interrupts with less than 1 sec intervals are not recommended.
Multiple switch bounce pulses are recommended to be filtered out.

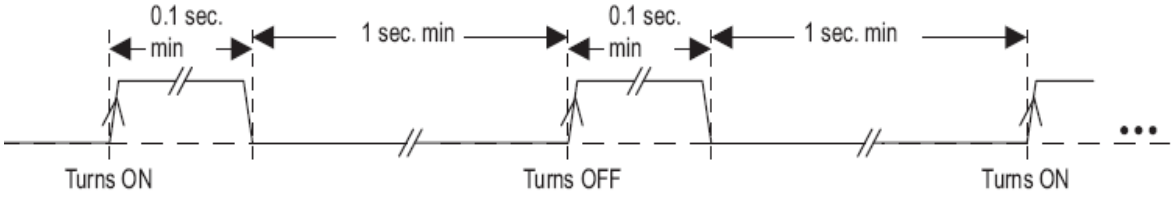


Figure 7-1: ON_OFF timing

ON_OFF input has internal pull-down resistor of 100kΩ.
ON_OFF pulse high state is 1.2 to 6V. Do not drive high permanently or pull-up this input.
Must be connected to host.

nRESET input

The Power-on-Reset (POR) is generated internally in the ORG14XX series module.
Additionally, manual reset option is available through nRESET pad.
Resetting the module clears the RTC block and configuration settings become default.
nRESET signal should be applied for at least 1µs.
nRESET input is active low and has internal pull-up resistor of 86kΩ.
Do not drive this input high. Do not connect if not in use.

WAKEUP output

The WAKEUP pad is an output from the ORG14XX series module, used to flag for power state.
A logic low on this output indicates that the module is in one of its low-power states - Hibernate or Standby.
A logic high on this output indicates that the module is in Full Power state.
In addition WAKEUP output can be used to control enable of auxiliary devices.
Wakeup output is LVCMOS 1.8V compatible. Do not connect if not in use.

1PPS output

The pulse-per-second (PPS) output provides a pulse signal for timing purposes.
Pulse length (high state) is 200ms about 1µs synchronized to full UTC second.
The UTC time message is generated and put into output FIFO 300ms after PPS.
The exact time between the PPS and UTC time message delivery depends on message rate, message queue and communication baud rate.
1PPS output is LVCMOS 1.8V compatible. Do not connect if not in use.

7.2.3. Host Data Interface

The ORG14XX series module has 2 types of interface ports to connect to host: UART and SPI. The ORG14XX series module is factory set to support UART or SPI by internal configuration straps.

UART

The module has a 4-wire UART port:

- TX used for GPS data reports. Output logic high voltage level is set by V_{TX}.
- RX used for receiver control. Input logic high voltage level is 1.45 to 3.6V.
- nCTS is optionally used for hardware flow control.
  High when host allows TX from the module. Input logic high voltage level is 1.45 to 3.6V.
- nRTS is optionally used for hardware flow control.
  High when module is ready to TX. Output logic high voltage level is 1.8V.

Operation:

The UART performs bit-by-bit transmitting and receiving in 8-bit octets when module is active. On the transmit side 1 start bit, 8 data bits and 2 stop bits followed by next character or idle line. Designers should treat computations of maximum message output capacity from ORG14XX with 11-bits per transmitted character.

On the receive side 1 start bit, 8 data bits, 1 stop bit or longer is accepted.

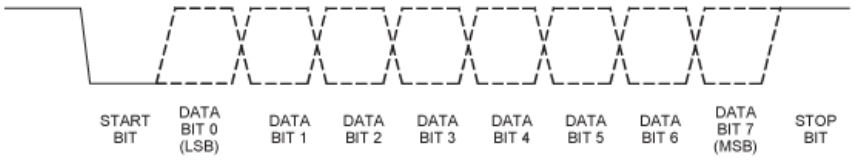


Figure 7-2: UART integrity

Because UART transmission is asynchronous and sampled by the receiver, both sides require closely match bit-rate clocks, and that data bit waveform and timing distortion at the receiver should be limited.

The default protocol is NMEA@4,800bps.

Current UART data rates in kbps are: 4.8, 9.6, 19.2, 38.4, 57.6, 115.2, 230.4, 460.8, 921.6.

The configuration for baud rates and respective protocols can be changed by commands via NMEA or OSP™ protocols.

Baud Rate (bps)	Error (%)	Baud Rate (bps)	Error (%)
4800	0.06	115200	0.24
9600	0.00	230400	1.04
19200	0.00	460800	0.60
38400	0.07	921600	2.40

Table 7-3: UART baud rate tolerance

Maximum allowed clock rate difference between ORG14XX and host is 2.0% overall.

Maximum bit-edge distortion ≤ 5% bit length. Maximum bit jitter ≤ 5% bit length.

SPI

The SPI (Serial to Peripheral Interface) is a master/slave synchronous serial bus that consists of 4 signals:

- Serial Clock (SCK) from master to slave.
- Serial Data Out (also called Master Out Slave In or MOSI) from master.
- Serial Data In (also called Master In Slave Out or MISO) from slave.
- Chip Select (CS) from master.

The host interface SPI of the ORG14XX series module is a slave mode SPI.
The four SPI pads are RX (MOSI), TX (MISO), nRTS(nCS) and nCTS(SCK).
Output logic high voltage level is set by V_{TX}. Inputs are 3.6V tolerant.
The host interface SPI features are:

- TX and RX each have independent 1024 byte FIFO buffers.
- RX and TX have independent, software specified two byte idle patterns of '0xA7 0xB4'.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.
- Supports a maximum clock of 6.8MHz.
- Default GPS data output format is NMEA standard.

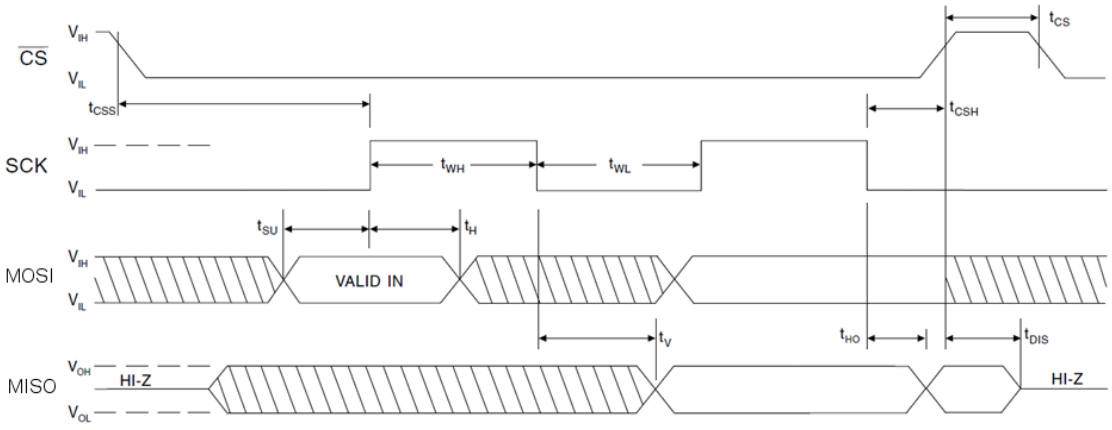


Figure 7-3: SPI timing

Symbol	Parameter	Min	Max	Units
t_{CLK}	SCK Time Period	140		ns
t_{CSS}	nCS Setup Time	0.5	1	t_{CLK}
t_{CS}	nCS High Time	1		t_{CLK}
t_{WH}	SCK High Time	0.5		t_{CLK}
t_{WL}	SCK Low Time	0.5		t_{CLK}
t_{CSH}	nCS Hold Time	0.5	1	t_{CLK}
t_{SU}	Data In Setup Time	0.5		t_{CLK}
t_H	Data In Hold Time	0.5		t_{CLK}
t_V	Output Valid	0.5		t_{CLK}
t_{HO}	Output Hold Time	0.5		t_{CLK}
t_{DIS}	Output Disable Time		0.5	t_{CLK}

Table 7-4: SPI timing

Operation:

The SPI performs bit-by-bit transmitting and receiving at the same time whenever nCS is asserted and SCK is active. In order to communicate properly with SPI device, the protocol must be agreed – specifically- SPI mode and an idle byte pattern.

Among 4 SPI modes of the clock polarity (CPOL) and clock phase (CPHA) only SPI Mode 1 <CPOL="0", CPHA ="1"> is currently supported:

- At CPOL="0" the base value of the clock is zero.
- For CPHA="1", data are read on the clock's falling edge and data are changed on a rising edge.

On power up, the first message to come out of the module is the "OK_TO_SEND" message.

It takes about 20ms from power up for the module SPI drivers to get initialized.

The slave has no way of forcing data to the master to indicate it is ready for transmission - the master must poll the client periodically.

Since the specified idle 2-byte pattern for both receive and transmit is '0xA7 0xB4', the master can transmit this idle pattern into the slave repeatedly. If the master receives idle patterns back from the slave, it indicates that the slave currently has nothing to transmit but is ready to communicate.

On the module receive side, the host is expected to transmit idle pattern when it is querying the module's transmit buffer. In this way, the volume of discarded bytes is kept nearly as low as in the UART implementation because the module hardware does not place most idle pattern bytes in its RX FIFO. Most messaging can be serviced with polling. The FIFO thresholds are placed to detect large messages requiring interrupt-driven servicing.

On the module transmit side the intent is to fill the FIFO only when it is disabled and empty.

In this condition, the module's SPI driver software loads as many queued messages as can completely fit in the FIFO. Then the FIFO is enabled.

The host is required to poll messages until idle pattern bytes are detected.

At this point the module's FIFO is empty and disabled, allowing the module's SPI driver to again respond to an empty FIFO interrupt and load the FIFO with any messages in queue.

Notes:

For SPI communication, read and write operations both require data being sent to the Slave SPI (idle bytes for reads and message data for writes). Any time data is sent to the module via the SPI bus, the Slave SPI of the module will send an equal amount of data back to the host.

These bytes must be buffered either in hardware or software, and it is up to the host to determine if the bytes received may be safely discarded (idle bytes), or should be passed on to the application handling GPS communication. Failure to properly handle data received from the SPI slave can result in corrupted GPS messages.

The external SPI master may send idle bytes and complete messages in a single transmission, provided that idle bytes shall not be inserted inside of a message.

The idle byte pattern and repeat count prevents the problem of messages lost due to normal occurrence of idle byte patterns within message data with high probability.

The external SPI master shall not send partial messages.

All transmissions from the SPI master shall be in multiples of 8 bits.

The external SPI master shall transmit the idle byte pattern when reading the SPI slave's transmit buffer when the master has no message data to transmit.

The SPI slave shall be serviced at a rate that will keep the TX FIFO empty.

7.2.4. Smart Sensors Data Interface

The ORG14XX module master mode I²C interface provides optional support for Dead Reckoning (DR) and optional code patch upload.
This bus has 2 lines, DR_SCL and DR_SDA, both are pseudo open-drain and require external pull-up resistors. Discrete EIT input is optionally used to wake up the module from Hibernate state.

Dead Reckoning (DR) I²C Interface

The DR I²C interface supports required sensor instruments for dead reckoning applications such as gyros, accelerometers, compasses or other sensors that can operate with an I²C bus.
The ORG14XX module acts as the I^2C Master and the sensor devices function in Slave mode.
This provides a very low latency data pipe for the critical sensor data so that it can be used in the Navigation Library and Kalman filter to enhance navigation performance.
The MEMS algorithms perform a sensor data fusion with the GPS signal measurements.
GPS measurements can be used to calibrate the MEMS sensors during periods of GPS navigation.
The MEMS sensors can augment GPS measurements, and can be more accurate than GPS under degraded GPS signal conditions and certain dynamics.
DR I²C interface supports:

- Common sensor formats
- Typical data lengths (command + in/data out) of several bytes
- Standard I²C bus maximum data rate 400kbps
- Minimum data rate 100kbps

In current Premium firmware implementation, MEMS sensors integration provides a pseudo "position pinning" feature to prevent position wander and heading instability.

EIT input

The EIT (External Interrupt) input is optionally used by external sensors to provide a discrete interrupt to the module when a change of state is detected.
The input is either a level triggered or an edge triggered programmable for high/ low level or rising/falling edge. The input is disabled during initial power-up or reset.
EIT interrupt input logic high state is 1.8 to 3.6V.
Do not connect to this input if the feature is not in use.

Data Storage Support

The DR I²C interface is available at boot-up for uploading data from a serial EEPROM.
Firmware updates may be provided from time to time to address ROM firmware issues as a method of performance improvement.
The DR I²C interface also supports serial flash devices used to store ARM7TDMI patch loads, including optional:

- FIFO support
- ARM7TDMI dedication to I²C interface during serial flash read or write

7.2.5. RF input

The module supports active and passive antennas. The antenna input impedance is 50Ω.
DC bias voltage for active antennas is provided via V_{ANT} pad.
Recommended active antenna NF ≤ 1.8 dB, net gain excluding cable loss 10dB ≤ G ≤ 25dB.
Leave V_{ANT} pad floating while using passive antenna.
Contact OriginGPS for passive antenna selection.

7.3 Typical Application Circuit

UART Host Interface – ordering codes R01, R02

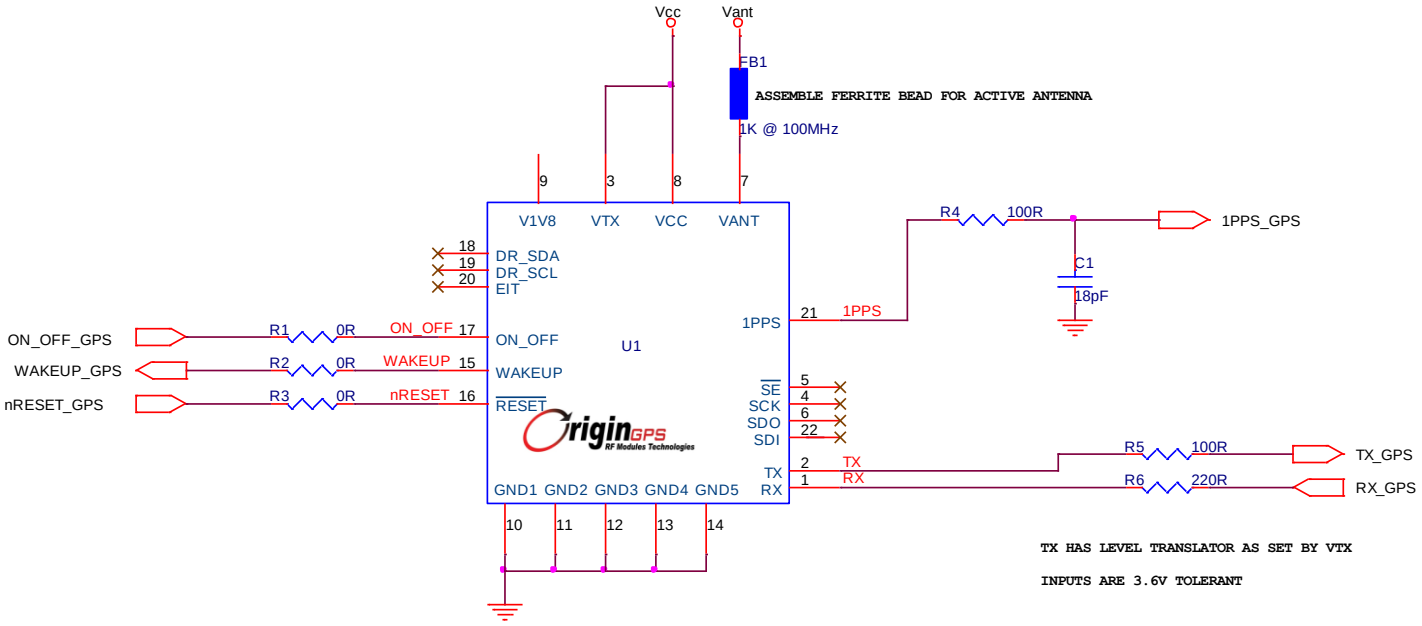


Figure 7-4: UART interface circuit

SPI Host Interface – ordering code R03

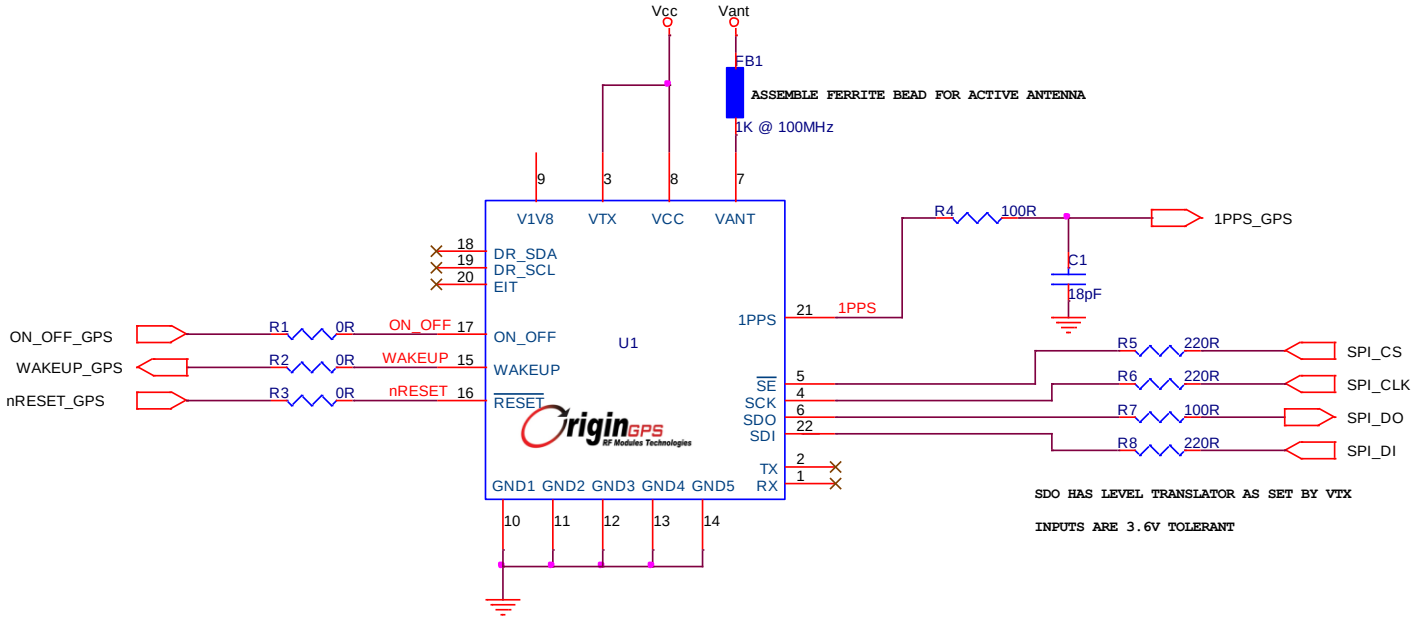


Figure 7-5: SPI interface circuit

8. PCB Layout

8.1 Footprint

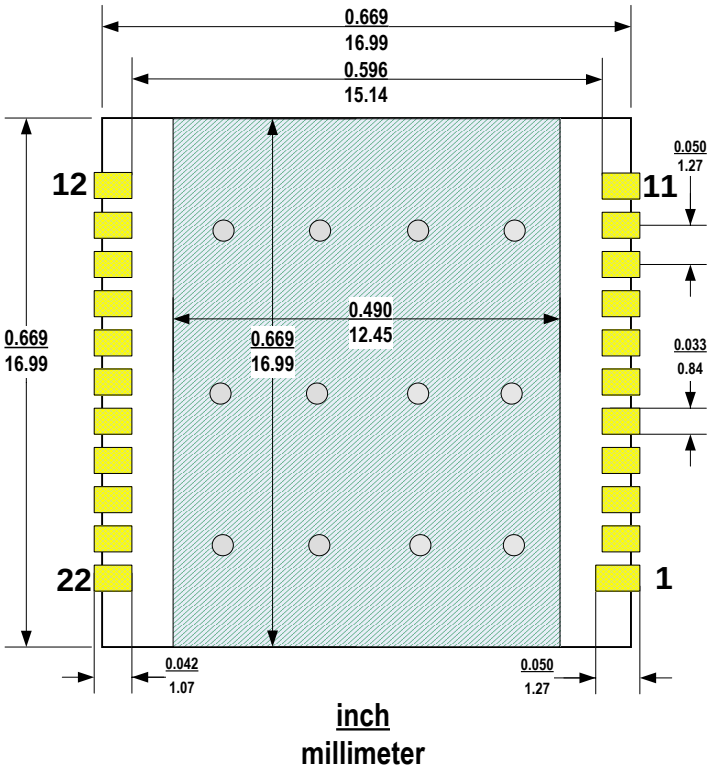


Figure 8-1: Footprint

Ground pad at the middle should be connected to main Ground plane by multiple vias.
Ground pad at the middle should be solder masked.
Silk print of module's outline is highly recommended for SMT visual inspection.

8.2 Design Restrictions

Keep out of signal or switching power traces and vias under the ORG1408 GPS module.

Signal traces to/from ORG1408 GPS module should have minimum length.

Recommended distance from adjacent active components is 3mm.

In case of adjacent high speed components, like CPU or memory, high frequency components, like transmitters, clock resonators or oscillators, metal planes, like LCD or battery enclosures, please contact OriginGPS for more precise, application specific recommendations.

9. Operation

When power is first applied, the ORG14XX series module goes into a Hibernate state while integrated RTC starts and internal FSM sequences though to “Ready-to-Start” state.
While in “Ready-to-Start” state, the module awaits a pulse to the ON_OFF input.
The host is not required to control external master nRESET since module’s internal reset circuitry handles detection of application of power.

9.1 Starting the module

Module start-up procedure depends upon the chosen ordering option.

	Boot Option 01	Boot Option 02	Boot Option 03
Ordering code	**ORG1408-xx01**	**ORG1408-xx02**	**ORG1408-xx03**
Power On State	Full Power	Hibernate	Hibernate
Host Interface	UART	UART	SPI
Interface settings on power	4,800 bps 8-N-1	4,800 bps 8-N-1	Slave
Data format on power	NMEA	NMEA	NMEA

Table 9-1: Hardware option

01 ordering code:

- The module has integrated power-up circuit that automatically asserts ON_OFF pulse 1 sec. after FSM indicates “Ready-to-Start” condition.

02 and 03 ordering codes:

- A pulse on the ON_OFF input will command the module to start.
- Since integrated RTC startup times are variable, detection of when the module is ready to accept an ON_OFF pulse requires the host to either wait for a fixed interval of 1 sec., or to monitor a pulse on module WAKEUP output that indicates FSM “Ready-to-Start”.
- Optionally, a pulse on the ON_OFF input can be asserted every second until the module starts by indicating logic high level on WAKEUP output.

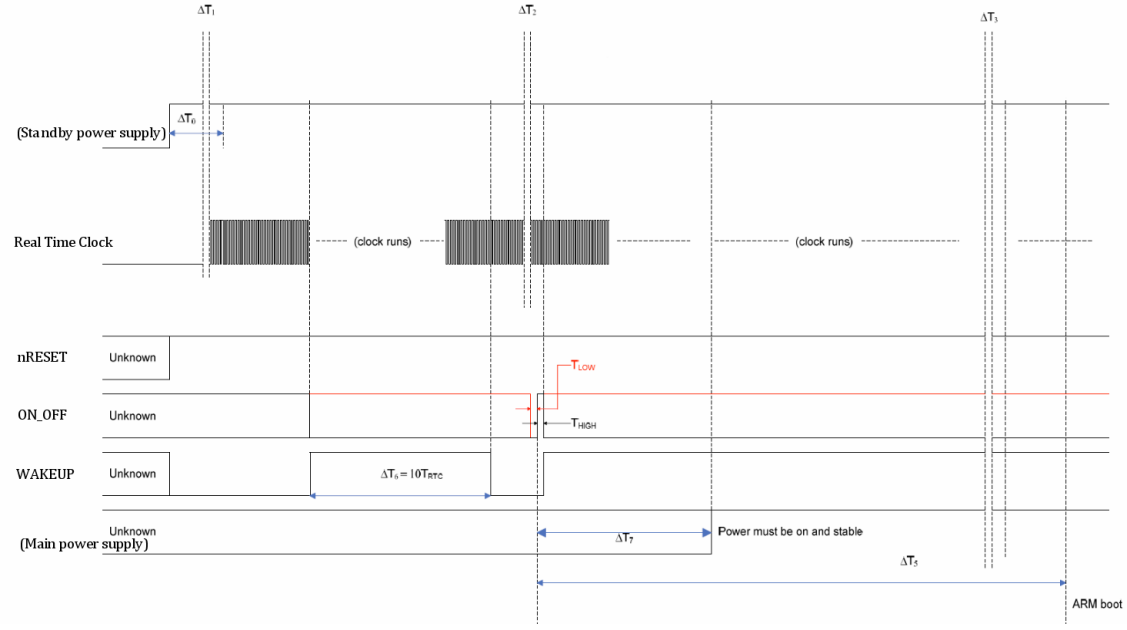


Figure 9-1: Startup timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{RTC}	RTC frequency	25^0C	-20 ppm	32768	+20 ppm	Hz
t_{RTC}	RTC tick	25^0C		30.5176		µs
ΔT_1	RTC startup time			300		ms
ΔT_0	Power stabilization		$6 \cdot t_{RTC} + \Delta T_1$	$7 \cdot t_{RTC} + \Delta T_1$	$8 \cdot t_{RTC} + \Delta T_1$	µs
ΔT_6	WAKEUP pulse	RTC running		10		t_{RTC}
ΔT_{LOW}	ON_OFF low		3			t_{RTC}
ΔT_{HIGH}	ON_OFF high		3			t_{RTC}
ΔT_3	Startup sequencing	After ON_OFF		1024		t_{RTC}
-	ON_OFF to WAKEUP high	After ON_OFF		6		t_{RTC}
ΔT_5	ON_OFF to ARM start	After ON_OFF		2130		t_{RTC}
ΔT_7	Main power source start[1]	WAKEUP high	0	30	300	t_{RTC}

Table 9-2: Startup timing

Note:
1. When power provided through dual supply.
Low quescent current power source (LDO) for Hibernate state, and high efficiency source (DC-DC) for Full Power state.
The main power supply should be able to provide current for Full Power state within 1ms after WAKEUP is high.

9.2 Verifying the module has started

The ORG14XX module WAKEUP output will go logic high indicating the GPS processor has started. System activity indication depends upon the chosen ordering option.

<u>01 and 02 ordering codes:</u>

- When active, the module will output NMEA messages at the 4800bps.
- First NMEA message after power-up is '$PSRF150,1*3E'.

<u>03 ordering code:</u>

- Since the module is SPI slave, there is no possible indication of system "ready" through SPI data interface.
- The host must initiate SPI connection approximately 1 sec. after WAKEUP output goes high.

9.3 Shutting down the module

Transferring the ORG14XX series module into Hibernate state can be initiated in two ways:

- By a pulse on the ON_OFF input when the ORG14XX module in Full Power state.
- By serial message MID205 (OSP™) or $PSRF117 (NMEA).
- Last message before Hibernate state is '$PSRF150,1*3F'.

The orderly shutdown may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls.

10.Software Functions

The module supports NMEA-0183 protocol and One Socket Protocol (OSP™).

10.1 NMEA

NMEA is generic ASCII protocol used by general purpose GNSS receivers.

NMEA Output Messages

Message	Description
$GPGGA	Time, position and fix type data
$GPGLL[1]	Latitude, longitude, UTC time of position fix and status
$GPGSA	GPS receiver operating mode, satellites used in the position solution and DOP values
$GPGSV	The number of GPS satellites in view, satellite ID, elevation, azimuth and SNR values
$GPRMC	Time, date, position, course and speed data
$GPVTG[1]	Course and speed information relative to the ground
$GPZDA[1]	1PPS timing message
$PSRF150	OK to send data to the module
$PSRF155	Extended Ephemeris Proprietary Message
$PSRF156,0x20	ECLM ACK/NACK
$PSRF156,0x21	ECLM EE Get Age response
$PSRF156,0x22	ECLM Get SGEE Age response
$PSRF156,0x23	ECLM Download Initiate Request
$PSRF156,0x24	ECLM Erase Storage File
$PSRF156,0x25	ECLM Update File Content
$PSRF156,0x26	ECLM Request File Content
$PSRF160[2]	Watchdog Timeout and Exception Condition

Table 10-1: NMEA protocol output messages

Note:

1. Not transmitted by default, can be enabled by $PSRF103 command

NMEA Input Messages

Message ID	Message	Description
$PSRF100	Set Serial Port	Set UART parameters and protocol
$PSRF101	Navigation Initialization	Parameters required for start using X/Y/Z
$PSRF103	Query/Rate Control	Query standard NMEA message and/or set output rate
$PSRF104	LLA Navigation Initialization	Parameters required for start using Lat/Lon/Alt
$PSRF105	Development Data On/Off	Development Data messages On/Off
$PSRF106	Select Datum	Selection of an alternative map datum
$PSRF107	Extended ephemeris proprietary message	
$PSRF108	Extended ephemeris proprietary message	
$PSRF110	Extended ephemeris debug	
$PSRF114,0x16	ECLM start download	
$PSRF114,0x17	ECLM file size	
$PSRF114,0x18	ECLM packet data	
$PSRF114,0x19	ECLM Get EE Age	
$PSRF114,0x1A	ECLM Get SGEE Age	
$PSRF114,0x1B	ECLM Host File Content	
$PSRF114,0x1C	ECLM Host ACK/NACK	
$PSRF117	System Turn Off	
$PSRF120	Storage Configuration Setting	

Table 10-2: NMEA protocol input messages

10.2 OSP™

OSP™ is a proprietary extension to SiRF Binary Standard protocol used by SiRF GPS processors.

OSP Binary Output Messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0 x 02	2	Measured Navigation Data			
0 x 03	3	True Tracker Data			
0 x 04	4	Measured Tracking Data			
0 x 06	6	SW Version			
0 x 07	7	Clock Status			
0 x 08	8	50 BPS Subframe Data			
0 x 09	9	Throughput			
0 x 0A	10	Error ID			
0 x 0B	11	Command Acknowledgement			
0 x 0C	12	Command No Acknowledgement			
0 x 0D	13	Visible List			
0 x 0E	14	Almanac Data			
0 x 0F	15	Ephemeris Data			
0 x 10	16	Test Mode 1			
0 x 12	18	Ok To Send			
0 x 13	19	Navigation Parameters			
0 x 14	20	Test Mode 2			
0 x 1B	27	DGPS Status			
0 x 1C	28	Nav. Lib. Measurement Data			
0 x 1E	30	Nav. Lib. SV State Data			
0 x 1F	31	Nav. Lib. Initialization Data			
0 x FF	255	Development Data			

Table 10-3: OSP binary output messages

OSP Binary Input Messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0 x 35	53	Advanced Power Management			
0 x 80	128	Initialize Data Source			
0 x 81	129	Switch to NMEA Protocol			
0 x 82	130	Set Almanac (upload)			
0 x 84	132	Software Version (Poll)			
0 x 86	134	Set Main Serial Port			
0 x 87	135	Switch Protocol			
0 x 88	136	Mode Control			
0 x 89	137	DOP Mask			
0 x 8A	138	MID_SET_DGPS_MODE			
0 x 8B	139	Elevation Mask			
0 x 8C	140	Power Mask			
0 x 8D	141	Editing Residual			
0 x 8E	142	Steady-State Detection			
0 x 8F	143	Static Navigation			
0 x 90	144	Poll Clock Status			
0 x 92	146	Poll Almanac			
0 x 93	147	Poll Ephemeris			
0 x 95	149	Set Ephemeris (upload)			
0 x 96	150	Switch Operating Mode			
0 x 97	151	Set Trickle Power Parameters			
0 x 98	152	Poll Navigation Parameters			
0 x A5	165	Set UART Configuration			
0 x A6	166	Set Message Rate			
0 x A7	167	Low Power Acquisition Parameters			
0 x A8	168	MID_POLL_CMD_PARAM			
0 x A9	169	Set Datum			
0 x AA	170	Set SBAS Parameters			
0 x AC	172	MID_DrIn	0 x 01	1	Set DrNavInit
			0 x 02	2	Set DrNavMode
			0 x 03	3	Set GyrFactCal
			0 x 04	4	Set DrSensParam
			0 x 05	5	Poll DrValid
			0 x 06	6	Poll GyrFactCal
			0 x 07	7	Poll DrSensParam
			0 x 13	19	DR Debug Information
0 x AF	175	Send Command String			
0 x B2	178	SIRF_MSG_SSB_TRACKER_IC	0 x 14	20	Patch Storage Control
			0 x 22	34	Patch Memory Load Request
			0 x 26	38	Patch Memory Exit Request
			0 x 28	40	Patch Memory Start Request
			0 x 90	144	Patch Manager Prompt
			0 x 91	145	Patch Manager Ack.
0 x CD	205	Set Generic Software Control	0 x 10	16	Software Commanded OFF
0 x D1	209	MID_QUERY_REQ			
0 x D2	210	MID_POS_REQ			

Table 10-4: OSP binary input messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0 x D3	211	MID_SET_AIDING	0 x 01	1	SET_IONO
			0 x 02	2	SET_EPH_CLOCK
			0 x 03	3	SET_ALM
			0 x 04	4	SET_ACQ_ASSIST
			0 x 05	5	SET_RT_INTEG
			0 x 06	6	SET_UTC_MODEL
			0 x 07	7	SET_GPS_TOW_ASSIST
			0 x 08	8	SET_AUX_NAV
			0 x 09	9	SET_AIDING_AVAIL
0 x D4	212	MID_STATUS_REQ	0 x 01	1	EPH_REQ
			0 x 02	2	ALM_REQ
			0 x 03	3	B_EPH_REQ
			0 x 04	4	TIME_FREQ_APPROX_POS_REQ
			0 x 05	5	CH_LOAD_REQ
			0 x 06	6	CLIENT_STATUS_REQ
			0 x 07	7	OSP_REV_REQ
			0 x 08	8	SERIAL_SETTINGS_REQ
0 x D5	213	MID_SESSION_CONTROL_REQ	0 x 01	1	SESSION_OPEN_REQ
			0 x 02	2	SESSION_CLOSE_REQ
0 x D6	214	MID_HW_CONFIG_RESP			
0xD7	215	MID_AIDING_RESP	0 x 01	1	APPROX_MS_POS_RESP
			0 x 02	2	TIME_TX_RESP
			0 x 03	3	FREQ_TX_RESP
			0 x 04	4	SET_NBA_SF1_2_3
			0 x 05	5	SET_NBA_SF4_5
0xD8	216	MID_MSG_ACK_IN	0 x 01	1	ACK_NACK_ERROR
			0 x 02	2	REJECT
0xD9	217		0 x 01	1	SENSOR_ON_OFF
0xDA	218	MID_PWR_MODE_REQ	0 x 00	0	FP_MODE_REQ
			0 x 01	1	APM_REQ
			0 x 02	2	MPM_REQ
			0 x 03	3	TP_REQ
			0 x 04	4	PTF_REQ
0xDB	219	MID_HW_CTRL_IN	0 x 01	1	VCTCXO
			0 x 02	2	ON_OFF_SIG_CONFIG
0xDC	220	MID_CW_CONTROLLER_REQ	0 x 01	1	CONFIG
			0 x 02	2	EVENT_REG
			0 x 03	3	COMMAND_SCAN
			0 x 04	4	CUSTOM_MON_CONFIG
			0 x 05	5	FFT_NOTCH_SETUP
0xE1	225	MID_SiRFOutput	0 x 06	6	STATISTICS
			0 x 07	7	Statistics with Aiding

Table 10-4: OSP binary input messages

MID (hex)	MID (dec)	Definition	Sub ID (hex)	Sub ID (dec)	Definition
0xE8	232	MID_EE_INPUT	0 x 01	1	SSB_EE_SEA_PROVIDE_EPH
			0 x 02	2	SSB_EE_POLL_STATE
			0 x 10	16	SSB_EE_FILE_DOWNLOAD
			0 x 11	17	SSB_EE_QUERY_AGE
			0 x 12	18	SSB_EE_FILE_PART
			0 x 13	19	SSB_EE_DOWNLOAD_TCP
			0 x 14	20	SSB_EE_SET_EPHEMERIS
			0 x 15	21	SSB_EE_FILE_STATUS
			0 x 16	22	ECLM Start Download
			0 x 17	23	ECLM File Size
			0 x 18	24	ECLM Packet Data
			0 x 19	25	Get EE Age
			0 x 1A	26	Get SGEE Age
			0 x 1B	27	ECLM Host File Content
			0 x 1C	28	ECLM Host ACK/NACK
			0 x 1D	29	ECLM Get NVM Header
			0 x FD	253	EE_STORAGE_CONTROL
			0 x FE	254	SSB_EE_DISABLE_EE_SECS

Table 10-4: OSP binary input messages

11.Handling Information

11.1 Product Packaging and Delivery

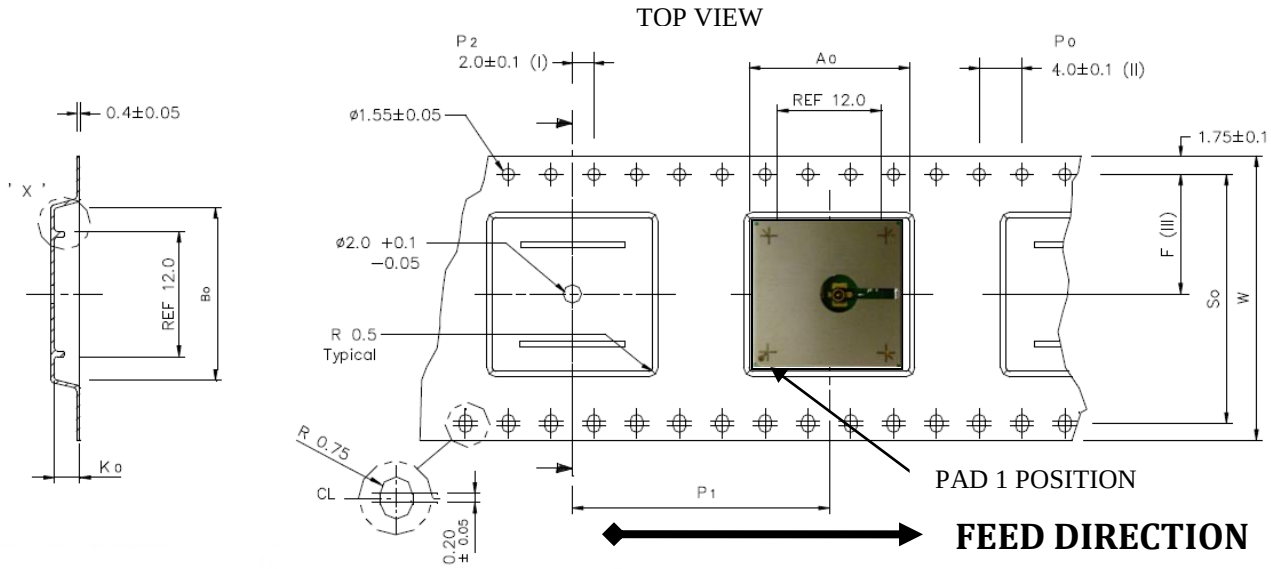


Figure 11-1: Carrier

	ORG1408
A_0	18.00 ± 0.1
B_0	18.00 ± 0.1
K_0	03.60 ± 0.1
F	14.20 ± 0.1
P_1	24.00 ± 0.1
S_0	28.40 ± 0.1
W	32.00 ± 0.3

Table 11-1: Carrier dimensions [mm]

Carrier material: Conductive Polystyrene

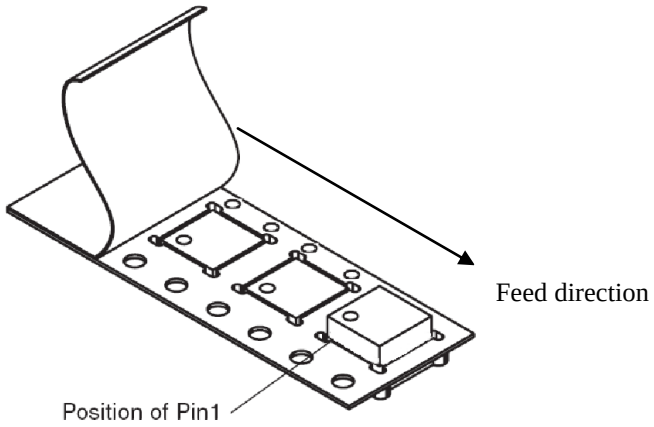


Figure 11-2: Module position

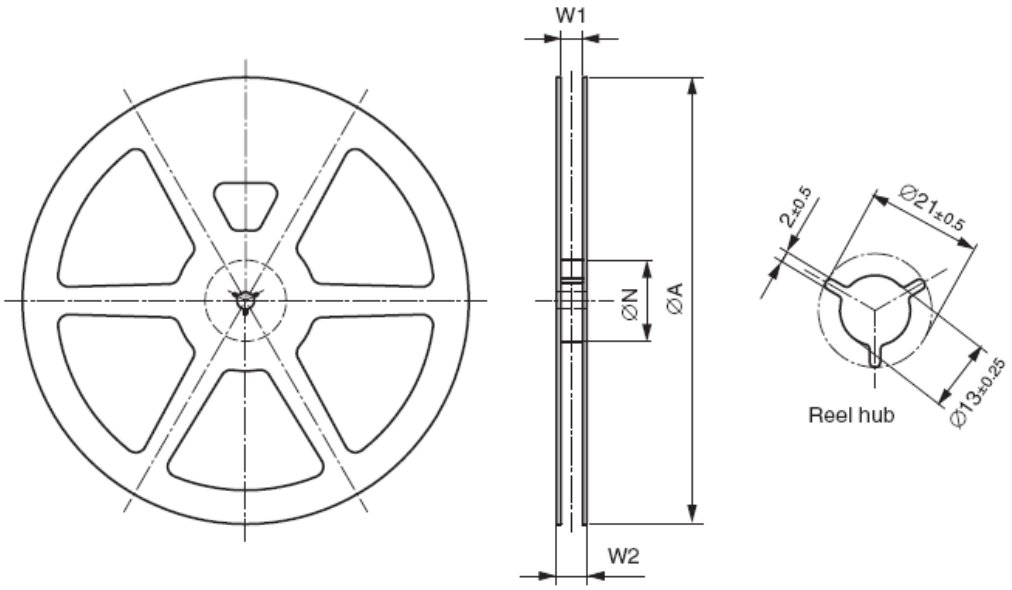


Figure 11-3: Reel

ØA	330.00 ± 0.85
ØN	60.00 ± 0.5
W_1	33.00 ± 0.5
W_2	39.00 ± 0.5

Table 11-2: Reel dimensions [mm]

Reel material: Antistatic Plastic

Each reel contains 250 or 500 modules.

11.2. Moisture Sensitivity

The devices are moisture sensitive at MSL 3 according to standard IPC/JEDEC J-STD-033B.

The recommended drying process for samples and bulk components is to be done at 125°C for 48 hours.

11.3. Assembly

The ORG14XX series modules support automatic assembly and reflow soldering processes.

Reflow soldering of the ORG14XX series modules on the component side of the motherboard PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD.

Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

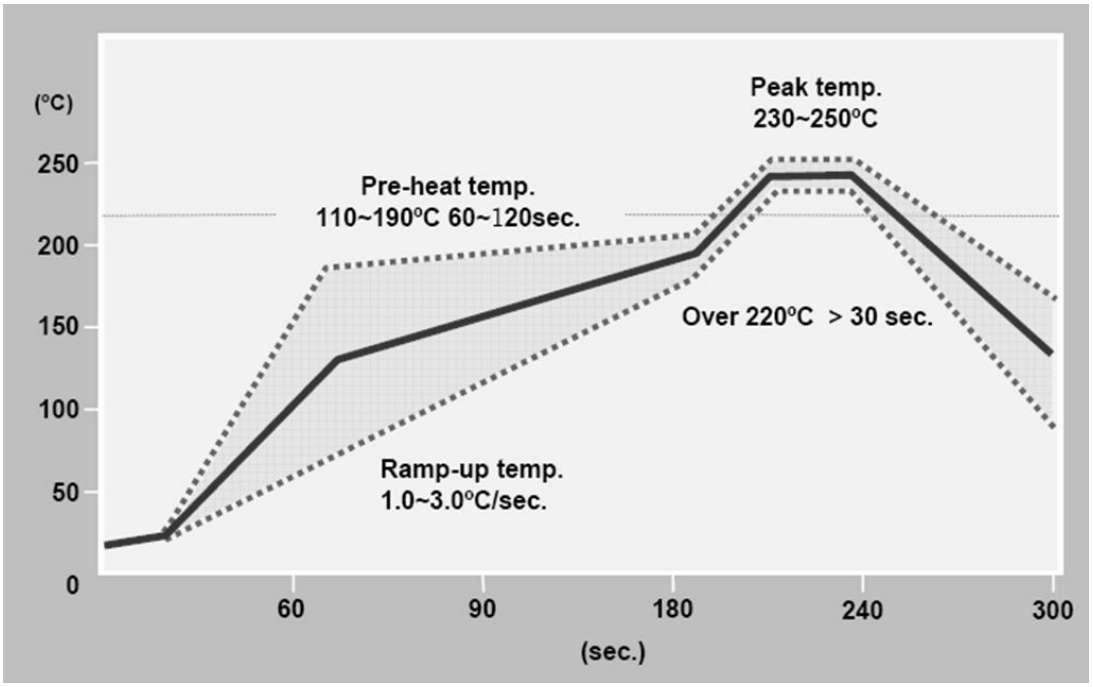


Figure 11-4: Recommended soldering profile

Suggested peak reflow temperature is 250°C for 10 sec. for Pb-Free solder paste.

Absolute Maximum reflow temperature is 260°C for 10 sec.

11.4. Rework

If localized heating is required to rework or repair the ORG14XX series module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

11.5. ESD Sensitivity

The ORG14XX series module is ESD sensitive device and should be handled with care.

11.6. Compliances

The following standards are applied on the ORG14XX series modules production:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

The ORG14XX series modules are being manufactured ISO 9001:2000 accredited facilities.

The ORG14XX series modules are designed and being manufactured and handled to comply with and according with Pb-Free/RoHS Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

The ORG14XX series modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- US FCC 47CFR Part 15:09, Subpart B, Class B

11.7. Safety Information

Improper handling and use can cause permanent damage to the device.

There is also the possible risk of personal injury from mechanical trauma or shocking hazard.

11.8. Disposal Information

The product should not be treated as household waste.

For more detailed information about recycling electronic components, please contact your local waste management authority.

12.Mechanical Specifications

- The ORG14XX series module has advanced ultra-miniature packaging and a LGA SMD footprint.
- The ORG14XX series module PCB footprint size is 17mm x 17mm.
- The ORG1408 module is surface mount device packaged on a miniature printed circuit board with a metallic RF enclosure featuring miniature RF connector.
- There are 22 surface mount connection pads with a base metal of copper and an Electroless Nickel / Immersion Gold (ENIG) finish.
- The ORG14XX series module has been designed and packaged for automated pick and place assembly and reflow soldering processes.

12.1. ORG1408 Module

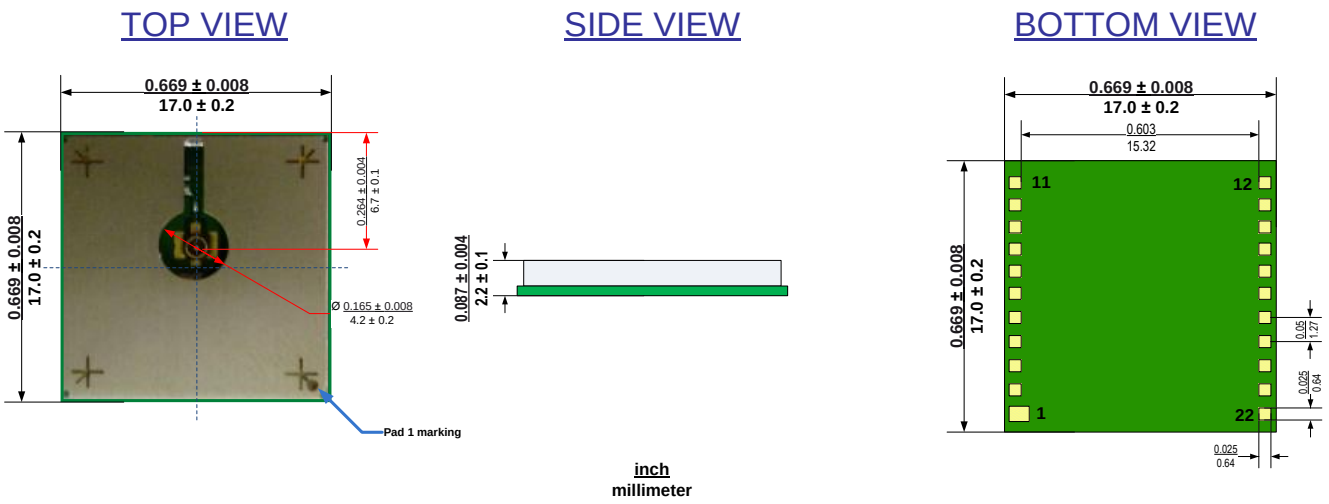


Figure 12-1: ORG1408 mechanical drawing

Dimensions	Length	Width	Height	Weight	
mm	17.0 ± 0.2	17.0 ± 0.2	2.2 ± 0.1	gr	1.4
inch	0.669 ± 0.008	0.669 ± 0.008	0.088 ± 0.004	oz	0.1

Table 12-1: ORG1408 mechanical summary

12.2. Plug

Mating plug for RF antenna connector is Hirose W.FL or Sunridge MCD series.

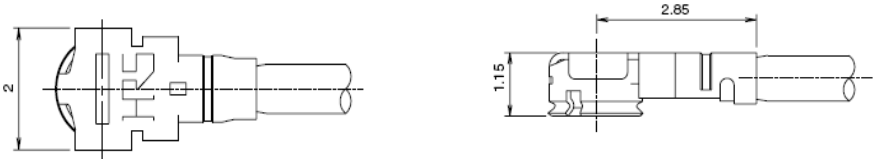
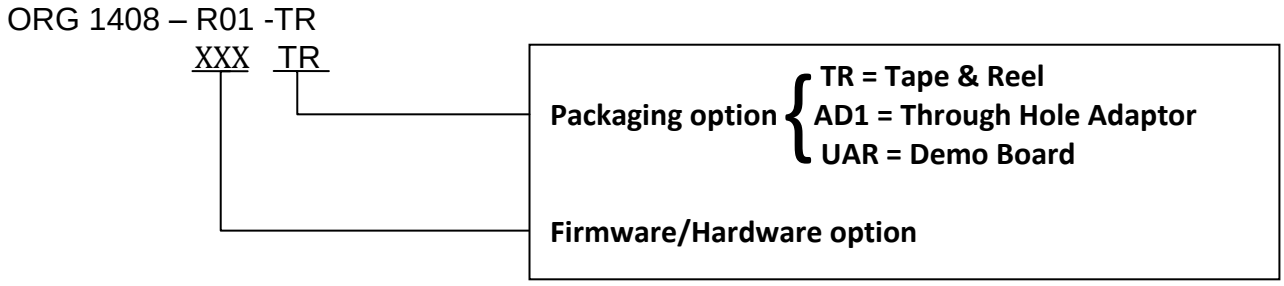


Figure 12-2: ORG1408 receptacle mechanical drawing

13.Ordering Information



		Standard Series	Premium Series
Ordering code		**ORG1408-R01**	**ORG1408-PM01**
Internal Switch Mode support		✓	✓
Firmware Features	Jammer Remover	✓	✓
	CGEE™ and SGEE™	✓	✓
	ATP™, PTF™, APM™	✓	✓
	SiRFAware MPM™		✓
	SBAS (WAAS/EGNOS)		✓
	MEMS sensors support		✓
	ABP™ support		✓

Table 13-1: Firmware options

	Boot Option 01	Boot Option 02	Boot Option 03
Ordering code	**ORG1408-xx01**	**ORG1408-xx02**	**ORG1408-xx03**
Power On State	Full Power	Hibernate	Hibernate
Host Interface	UART	UART	SPI
Interface settings on power	4,800 bps	4,800 bps	Slave
Data format on power	NMEA	NMEA	NMEA

Table 13- 2: Hardware options