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**Wilk Elektronik S.A.**

# GOODRAM Industrial microSD (MLC, PseudoSLC)

# Version 1.0

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# 1. Introduction

## 1.1. General Description

The Micro Secure Digital (microSD) card version 3.0 is fully compliant to the specification released by SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.00 Final] Specifications.

The microSD 3.0 card comes with 8-pin interface, designed to operate at a maximum operating frequency of 50MHz or 100MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. Its capacity could be more than 2GB and up to 32GB in the future with FAT32 which is called Micro SDHC (microSD High Capacity).

Industrial micro Secure Digital 3.0 card is one of the most popular cards today based on its high performance, good reliability and wide compatibility. Not to mention that it's well adapted for hand-held applications in semi-industrial/medical markets already. Moreover, with customized firmware technique, Industrial 8032 microSD 3.0 can be configured with pSLC SD Mode and presents outstanding performance along with better P/E cycles.

## 1.2. Flash Management

- o **Error Correction Code (ECC)**

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, PS8032 applies the BCH ECC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption.

- o **Wear Leveling**

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the

device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

- o **Bad Block Management**

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Bad blocks that are developed during the lifespan of the flash are named "Later Bad Blocks". implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

- o **Smart Function**

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an special function that allows a memory device to automatically monitor its health. provides a program named SmartInfo Tool to observe 's SD and microSD cards. **Note that this tool can only support 's PS8032 controller and industrial SD and microSD cards.** This tool will display the controller version, flash type, firmware version, endurance life ratio, good block ratio, and so forth. In addition, a warning message will appear under the following 3 conditions:

(1) When the life ratio remained is less than **10%**,

(2) When the amount of abnormal power on is more than **3,500** cycles, and

(3) When there are less than **5** usable blocks for replacing bad blocks.

- o **Auto-Read Refresh**

Auto-Read Refresh is especially applied on devices that read data mostly but rarely write data, such as GPS. When blocks are continuously read, then the device cannot activate wear leveling since it can only be applied while writing data. Thus, errors will accumulate and become uncorrectable. Accordingly, to avoid errors exceed the amount ECC can correct and blocks turn bad, 's firmware will automatically refresh the bit errors when the error number in one block approaches the threshold, ex., 24 bits.

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o **Pseudo SLC (pSLC)**

Pseudo SLC can be considered as an extended version of MLC. While MLC contains fast and slow pages, pSLC only applies fast pages for programming. The concept of pSLC is demonstrated in the two tables below. The first and second bits of a memory cell represent a fast and slow page respectively, as shown in the left table. Since only fast pages are programmed when applying pSLC, the bits highlighted in red are used, as shown in the right table. Accordingly, because only fast pages are programmed, pSLC provides better performance and endurance than MLC. Moreover, pSLC performs similarly with SLC, yet pSLC is more cost-effective.

| MLC Flash | | Pseudo SLC Flash | |
|---|---|---|---|
| 1st Bit (Fast page) | 2nd Bit (Slow page) | 1st Bit (Fast page) | 2nd Bit (Slow page) |
| 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 |

Cell Content of MLC (Left) and pSLC (Right)

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# 2. Product Specifications

- **Capacity**

  o MLC: 4GB up to 64GB (Diamond & Gold)

  o Pseudo SLC: 2GB up to 32GB (Diamond & Gold)

- **Operation Temp. Range**

  o Gold Series: -25~85°C

  o Diamond Series: -40~+85°C

- **Storage Temp. Range**

  o -40~+85°C

- **Support SD system specification version 3.0**

- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver3.0 Final] Specifications**

- **Support SD SPI mode**

- **Designed for read-only and read/write cards**

- **Bus Speed Mode (use 4 parallel data lines)**

  o Non-UHS mode

    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec

    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec

      **Note:** SDSC card (capacity less than and including 2GB) only supports non-UHS mode.

  o UHS-I mode

    - SDR12: SDR up to 25MHz, 1.8V signaling

    - SDR25: SDR up to 50MHz, 1.8V signaling

    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec

    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

      **Note:** Timing in 1.8V signaling is different from that of 3.3V signaling.

- **The command list supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions**

- **Copyrights Protection Mechanism**

o   Compliant with the highest security of SDMI standard

- **Support CPRM (Content Protection for Recordable Media) of SD Card**

- **Card removal during read operation will never harm the content**

- **Password Protection of cards (optional)**

- **Write Protect feature using mechanical switch**

- **Built-in write protection features (permanent and temporary)**

- **+4KV/-4KV ESD protection in contact pads**

- **Operation voltage range: 2.7 ~ 3.6V**

- **Performance**

  o   MLC

| Capacity | Mode | Flash Structure | Sequential | |
|---|---|---|---|---|
| | | | Read (MB/s) | Write (MB/s) |
| 4GB | UHS-I | TSB 19nm 4GB x 1 | 26 | 10 |
| 8GB | UHS-I | TSB 19nm 8GB x 1 | 26 | 10 |
| 16GB | UHS-I | TSB 19nm 8GB x 2 | 26 | 10 |
| 32GB | UHS-I | TSB 19nm 8GB x 4 | 26 | 10 |
| 64GB | UHS-I | TSB 19nm 8GB x 8 | 26 | 15 |

  o   Pseudo SLC

| Capacity | Mode | Flash Structure | Sequential | |
|---|---|---|---|---|
| | | | Read (MB/s) | Write (MB/s) |
| 2GB | Non-UHS | TSB 19nm 4GB x 1 | 20 | 20 |
| 4GB | UHS-I | TSB 19nm 8GB x 1 | 26 | 24 |
| 8GB | UHS-I | TSB 19nm 8GB x 2 | 26 | 24 |
| 16GB | UHS-I | TSB 19nm 8GB x 4 | 26 | 24 |
| 32GB | UHS-I | TSB 19nm 8GB x 8 | 26 | 24 |

**NOTES:**

1.   The performance is obtained from TestMetrix Test (@500MB).
2.   Samples are made of Toshiba 19nm MLC Toggle NAND Flash.
3.   Performance may vary from flash configuration and platform.
4.   The table above is for your reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration.

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# 3. Environmental Specifications

o **Environmental Conditions**

- Temperature and Humidity

    o Storage Temperature Range

        - -40°C ~ 85°C

- Operation Temperature Range

    o Gold grade: -25°C ~ 85°C

    o Diamond grade: -40°C ~ 85°C

High Temperature Test Condition (Gold Series)

|  | Temperature | Humidity | Test Time |
|---|---|---|---|
| **Operation** | 85°C | 0% RH | 168 hours |
| **Storage** | 85°C | 0% RH | 500 hours |

**Result:** No any abnormality is detected.

High Temperature Test Condition (Diamond Series)

|  | Temperature | Humidity | Test Time |
|---|---|---|---|
| **Operation** | 85°C | 0% RH | 300 hours |
| **Storage** | 85°C | 0% RH | 500 hours |

**Result:** No any abnormality is detected.

Low Temperature Test Condition (Gold Series)

|  | Temperature | Humidity | Test Time |
|---|---|---|---|
| **Operation** | -25°C | 0% RH | 168 hours |
| **Storage** | -40°C | 0% RH | 300 hours |

**Result:** No any abnormality is detected.

Low Temperature Test Condition (Diamond Series)

|  | Temperature | Humidity | Test Time |
|---|---|---|---|
| **Operation** | -40°C | 0% RH | 168 hours |
| **Storage** | -40°C | 0% RH | 500 hours |

**Result:** No any abnormality is detected.

High Humidity Test Condition (Gold Series)

|  | Temperature | Humidity | Test Time |
|---|---|---|---|
| **Operation** | 40°C | 95% RH | 4 hours |
| **Storage** | 40°C | 95% RH | 500 hours |

**Result:** No any abnormality is detected.

High Humidity Test Condition (Diamond Series)

|  | Temperature | Humidity | Test Time |
|---|---|---|---|
| **Operation** | 55°C | 95% RH | 4 hours |
| **Storage** | 55°C | 95% RH | 500 hours |

**Result:** No any abnormality is detected.

Temperature Cycle Test (Gold Series)

|  | Temperature | Test Time | Cycle |
|---|---|---|---|
| **Operation** | -25°C | 30 min | 20 Cycles |
|  | 85°C | 30 min |  |
| **Storage** | -40°C | 30 min | 20 Cycles |
|  | 85°C | 30 min |  |

**Result:** No any abnormality is detected.

Temperature Cycle Test (Diamond Series)

|  | Temperature | Test Time | Cycle |
|---|---|---|---|
| **Operation** | -40°C | 30 min | 20 Cycles |
|  | 85°C | 30 min |  |
| **Storage** | -40°C | 30 min | 50 Cycles |
|  | 85°C | 30 min |  |

**Result:** No any abnormality is detected.

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o **Shock**

Shock Specification

| | Acceleration Force | Half Sin Pulse Duration |
|---|---|---|
| **Industrial microSD card** | 1500G | 0.5ms |

**Result:** No any abnormality is detected when power on.

o **Vibration**

Vibration Specification

| | Condition | | Vibration Orientation |
|---|---|---|---|
| | **Frequency/Displacement** | **Frequency/Acceleration** | |
| **Industrial microSD card** | 20Hz~80Hz/1.52mm | 80Hz~2000Hz/20G | X, Y, Z axis/30 min for each |

**Result:** No any abnormality is detected when power on.

o **Drop**

Drop Specification

| | Height of Drop | Number of Drop |
|---|---|---|
| **Industrial microSD card** | 150cm free fall | 6 face of each unit |

**Result:** No any abnormality is detected when power on.

o **Bending**

Bending Specification

| | Force | Action |
|---|---|---|
| **Industrial microSD card** | ≥ 10N | Hold 1min/5times |

**Result:** No any abnormality is detected when power on.

o **Torque**

Torque Specification

| | Force | Action |
|---|---|---|
| **Industrial microSD card** | 0.1N-m or +/-2.5 deg | Hold 30 seconds/5times |

**Result:** No any abnormality is detected when power on.

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○ **Electrostatic Discharge (ESD)**

Contact ESD Specification

|  | Condition | Result |
|---|---|---|
| **Industrial microSD card** | Contact: +/- 4KV each item 25 times<br>Air: +/- 8KV 10 times | PASS |

○ **EMI Compliance**

- FCC: CISPR22

- CE: EN55022

- BSMI 13438

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# 4. SD Card Comparison

Comparing SD3.0 Standard and SD3.0 SDHC

| | SD3.0 Standard (Backward compatible to 2.0 host) | SD3.0 SDHC |
|---|---|---|
| **Addressing Mode** | Byte (1 byte unit) | Block (512 byte unit) |
| **HCS/CCS bits of ACMD41** | Support | Support |
| **CMD8 (SEND_IF_COND)** | Support | Support |
| **CMD16 (SET_BLOCKLEN)** | Support | Support (Only CMD42) |
| **Partial Read** | Support | Not Support |
| **Lock/Unlock Function** | Mandatory | Mandatory |
| **Write Protect Groups** | Optional | Not Support |
| **Supply Voltage 2.0v – 2.7v (for initialization)** | Not Support | Not Support |
| **Total Bus Capacitance for each signal line** | 40pF | 40pF |
| **CSD Version (CSD_STRUCTURE Value)** | 1.0 (0x0) | 2.0 (0x1) |
| **Speed Class** | **Optional** | Mandatory (Class 2 / 4 / 6 / 10) |

# 5. Electrical Specifications

## 5.1. Power Consumption

The table below is the power consumption of PS8032 with different flash memory types.

Power Consumption of PS8032 Industrial microSD card

| Flash Mode | Max. Power Up Current (uA) | Max. Standby Current (uA) | Max. Read Current (mA) | Max. Write Current (mA) |
|---|---|---|---|---|
| Single Flash[Note1] (1 x 8bit) | 150 | 150 | 100 | 100 |
| SDR/DDR | 250 | 250 | 200 | 200 |

NOTE:

1. Data transfer mode is single channel.

## 5.2. Electrical Specifications

Absolute Maximum Rating

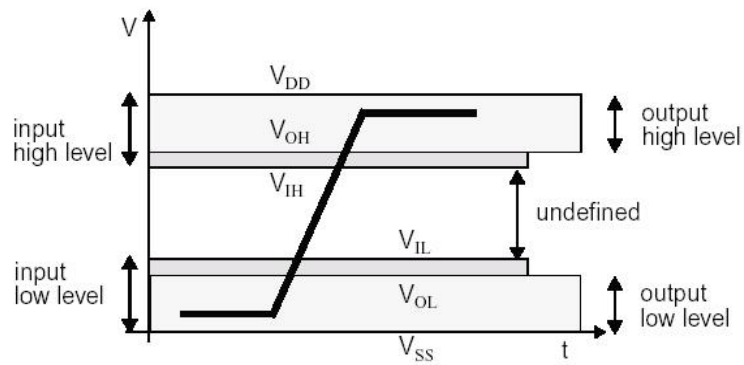| Item | Symbol | Parameter | MIN | MAX | Unit |
|---|---|---|---|---|---|
| 1 | $V_{DD}$-$V_{SS}$ | DC Power Supply | -0.3 | +3.3 | V |
| 2 | $V_{IN}$ | Input Voltage | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| 3 | Ta | Operating Temperature (Gold) | -25 | +85 | ℃ |
| 4 | Ta | Operating Temperature (Diamond) | -40 | +85 | ℃ |
| 5 | Tst | Storage Temperature | -40 | +85 | ℃ |
| 6 | $V_{DD}$ | $V_{DD}$ Voltage | 2.7 | 3.6 | V |

## 5.3. DC Characteristic

Bus Operation Conditions for 3.3V Signaling

Threshold Level for High Voltage Range

| Parameter | Symbol | Min | Max | Unit | Remarks |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 2.7 | 3.6 | V | |
| Output High Voltage | $V_{OH}$ | 0.75*$V_{DD}$ | | V | IOH=-100uA $V_{DD}$Min. |
| Output Low Voltage | $V_{OL}$ | | 0.125*$V_{DD}$ | V | $I_{OL}$ = 100uA $V_{DD\ min}$ |
| Input High Voltage | $V_{IH}$ | 0.625*$V_{DD}$ | $V_{DD}$+0.3 | V | |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$-0.3 | 0.25 *$V_{DD}$ | V | |
| Power up time | | | 250 | ms | from 0v to VDD min. |

o   **Bus Signal Levels**



Bus signal levels

Peak Voltage and Leakage Current

| Parameter | Symbol | Min | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Peak voltage on all lines | | -0.3 | $V_{DD}$+0.3 | V | |
| **All Inputs** | | | | | |
| Input Leakage Current | | -10 | 10 | uA | |
| **All Outputs** | | | | | |
| Output Leakage Current | | -10 | 10 | uA | |

o   **Bus Signal Line Levels**

| Parameter | symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Pull-up resistance | $R_{CMD}$ $R_{DAT}$ | 10 | 100 | kΩ | to prevent bus floating |
| Total bus capacitance for each signal line | $C_L$ | | 40 | pF | 1 card CHOST+CBUS shall not exceed 30 pF |
| Capacitance of the card for each signal pin | CCARD | | 10 | pF | |
| Maximum signal line inductance | | | 16 | nH | $f_{pp}$<20 MHz |
| Pull-up resistance inside card (pin1) | RDAT3 | 10 | 90 | kΩ | May be used for card detection |

o **Power Up Time**

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.
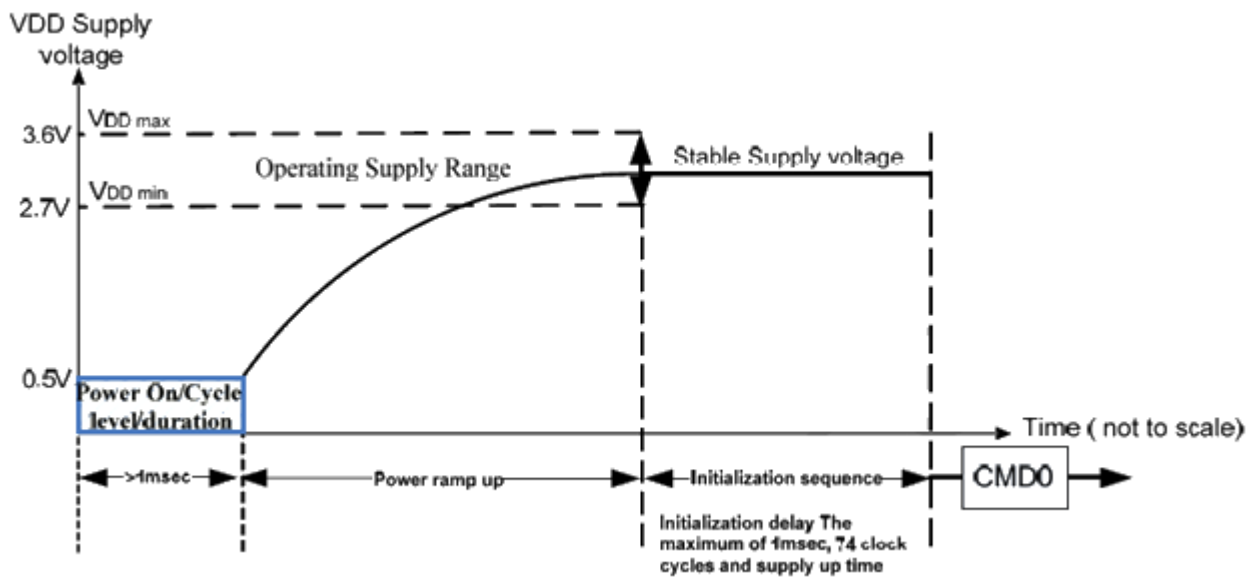


o **Power On or Power Cycle**

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

o **Power Supply Ramp Up**

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

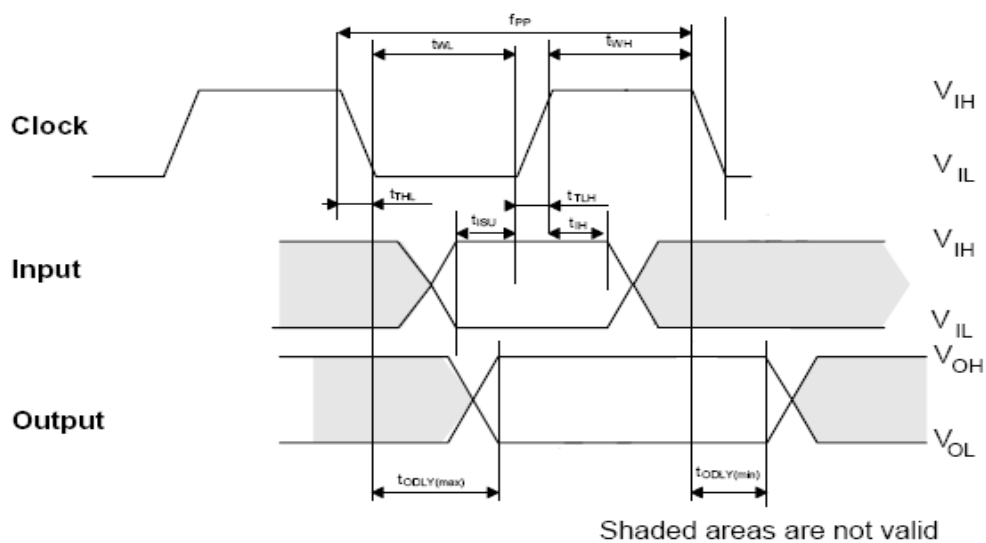(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

o **Power Down and Power Cycle**

- When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

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- If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

## 5.4. AC Characteristic

o **microSD Interface timing (Default)**

Clock, Input, Output timing diagram with labels: $f_{PP}$, $t_{WL}$, $t_{WH}$, $V_{IH}$, $V_{IL}$, $t_{THL}$, $t_{TLH}$, $t_{ISU}$, $t_{IH}$, $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, $t_{ODLY(max)}$, $t_{ODLY(min)}$

Shaded areas are not valid

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| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK (All values are referred to min($V_{IH}$) and max($V_{IL}$)** | | | | | |
| Clock frequency Data Transfer Mode | $f_{PP}$ | 0 | 25 | MHz | $C_{card} \leq 10$ pF (1 card) |
| Clock frequency Identification Mode | $f_{OD}$ | $0_{(1)}$/100 | 400 | kHz | $C_{card} \leq 10$ pF (1 card) |
| Clock low time | $t_{WL}$ | 10 | | ns | $C_{card} \leq 10$ pF (1 card) |
| Clock high time | $t_{WH}$ | 10 | | ns | $C_{card} \leq 10$ pF (1 card) |
| Clock rise time | $t_{TLH}$ | | 10 | ns | $C_{card} \leq 10$ pF (1 card) |
| Clock fall time | $t_{THL}$ | | 10 | ns | $C_{card} \leq 10$ pF (1 card) |
| **Inputs CMD, DAT (referenced to CLK)** | | | | | |
| Input set-up time | $t_{ISU}$ | 5 | | ns | $C_{card} \leq 10$ pF (1 card) |
| Input hold time | $t_{IH}$ | 5 | | ns | $C_{card} \leq 10$ pF (1 card) |
| **Outputs CMD, DAT (referenced to CLK)** | | | | | |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | 0 | 14 | ns | $C_L \leq 40$ pF (1 card) |
| Output Delay time during Identification Mode | tODLY | 0 | 50 | ns | $C_L \leq 40$ pF (1 card) |

(1)    0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

Card Input Timing (High Speed Card)
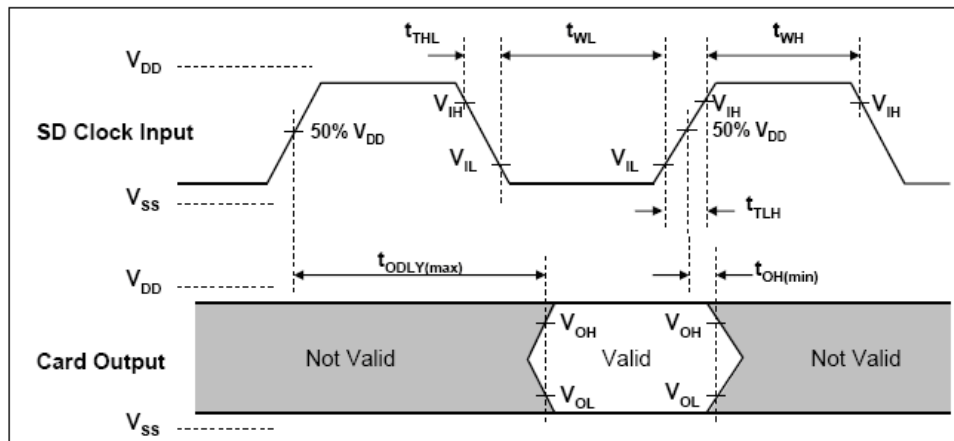


Card Output Timing (High Speed Mode)

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| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK (All values are referred to min($V_{IH}$) and max($V_{IL}$)** | | | | | |
| Clock frequency Data Transfer Mode | $f_{PP}$ | 0 | 50 | MHz | $C_{card} \leq 10$ pF (1 card) |
| Clock low time | $t_{WL}$ | 7 | | ns | $C_{card} \leq 10$ pF (1 card) |
| Clock high time | $t_{WH}$ | 7 | | ns | $C_{card} \leq 10$ pF (1 card) |
| Clock rise time | $t_{TLH}$ | | 3 | ns | $C_{card} \leq 10$ pF (1 card) |
| Clock fall time | $t_{THL}$ | | 3 | ns | $C_{card} \leq 10$ pF (1 card) |
| **Inputs CMD, DAT (referenced to CLK)** | | | | | |
| Input set-up time | $t_{ISU}$ | 6 | | ns | $C_{card} \leq 10$ pF (1 card) |
| Input hold time | $t_{IH}$ | 2 | | ns | $C_{card} \leq 10$ pF (1 card) |
| **Outputs CMD, DAT (referenced to CLK)** | | | | | |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | | 14 | ns | $C_L \leq 40$ pF (1 card) |
| Output Hold time | $T_{OH}$ | 2.5 | | ns | $C_L \leq 15$ pF (1 card) |
| Total System capacitance of each line[1] | $C_L$ | | 40 | pF | CL ≤ 15 pF (1 card) |

(1)     In order to satisfy severe timing, the host shall drive only one card.

- o **microSD Interface timing (SDR12, SDR25 and SDR50 Modes)**

Input:
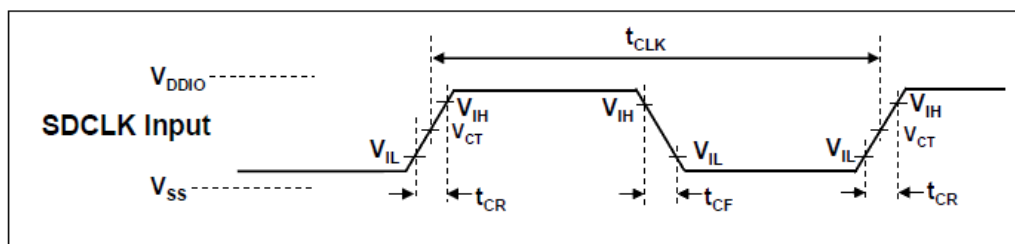


**Clock Signal Timing**

| Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|
| tCLK | 4.80 | - | ns | 208MHz (Max.), Between rising edge, VCT= 0.975V |
| tCR, tCF | - | 0.2* tCLK | ns | tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF |
| Clock Duty | 30 | 70 | % | |

Clock Signal Timing

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SDR50 Input Timing:
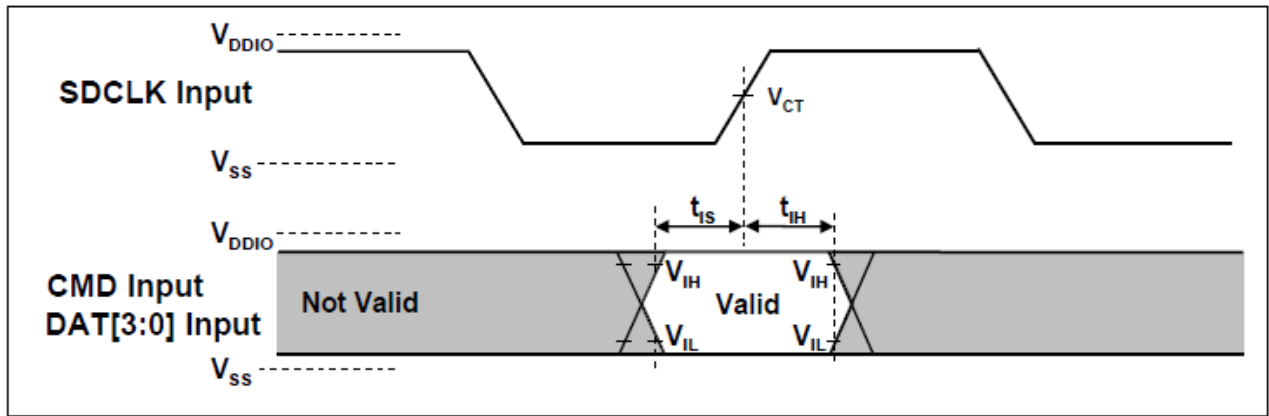


Card Input Timing

| Symbol | Min | Max | Unit | SDR50 Mode |
|--------|-----|-----|------|------------|
| tIs | 3.00 | - | ns | $C_{CARD}$ =10pF, VCT= 0.975V |
| tIH | 0.80 | - | ns | $C_{CARD}$ =5pF, VCT= 0.975V |

Output:
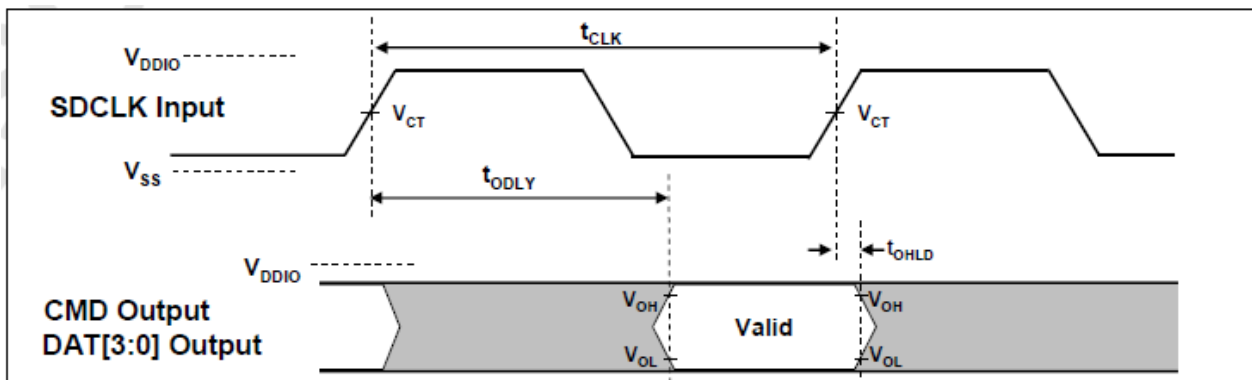


Output Timing of Fixed Data Window

| Symbol | Min | Max | Unit | Remark |
|--------|-----|-----|------|--------|
| tODLY | - | 7.5 | ns | tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50 |
| tODLY | - | 14 | ns | tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12, |
| TOH | 1.5 | - | ns | Hold time at the tODLY (min.), CL=15pF |

Output Timing of Fixed Data Window

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o   microSD Interface timing (DDR50 Modes)
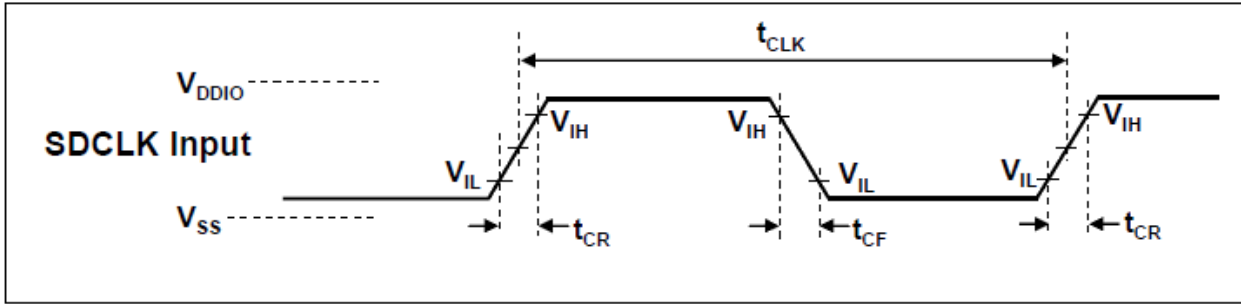


**Clock Signal Timing**

| Symbol | Min | Max | Unit | Remark |
|--------|-----|-----|------|--------|
| tCLK | 20 | - | ns | 50MHz (Max.), Between rising edge |
| tCR, tCF | - | 0.2* tCLK | ns | tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF |
| Clock Duty | 45 | 55 | % | |

**Clock Signal Timing**



In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line)

Available timing window for card output transition

Available timing window for host to sample data from card
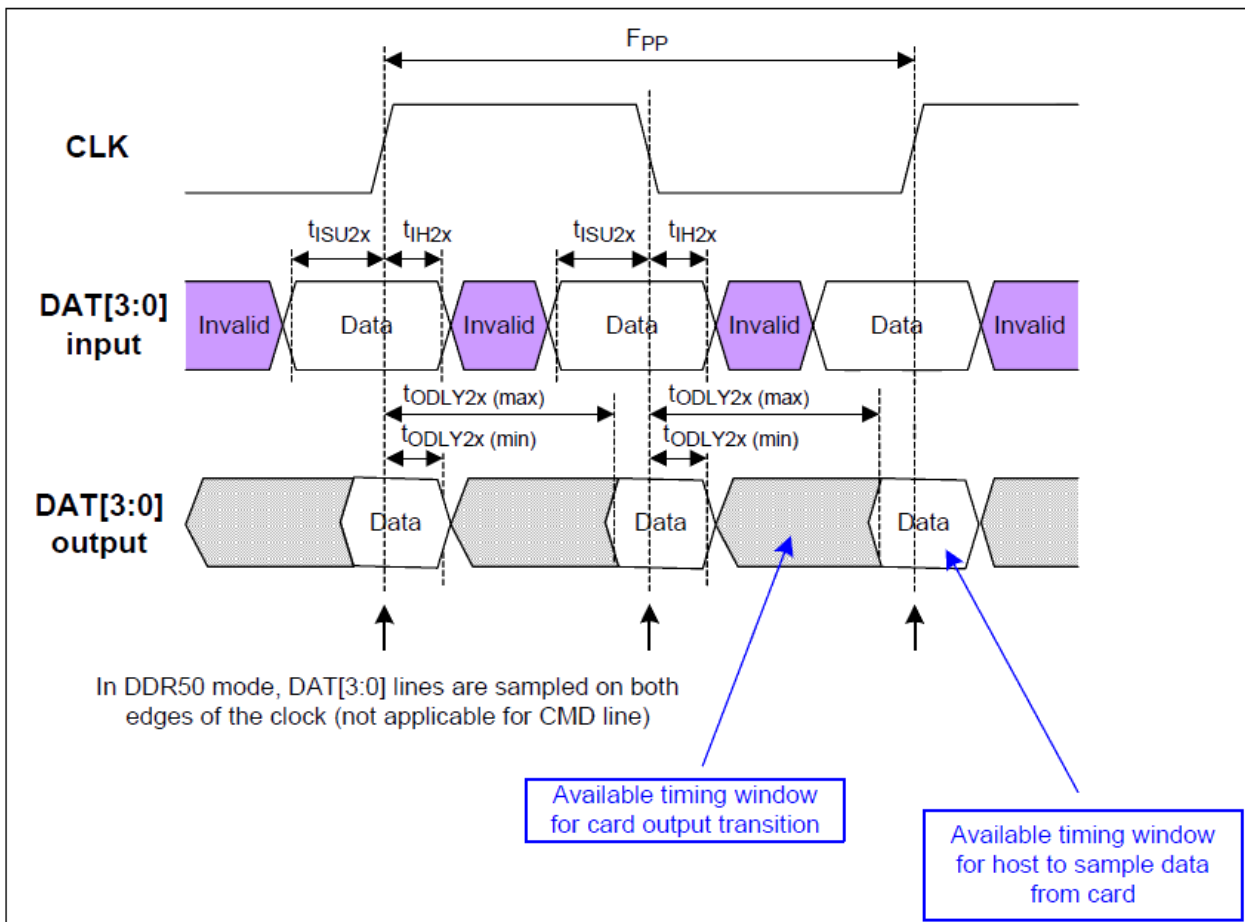
**Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode**

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| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| **Input CMD** (referenced to CLK rising edge) | | | | | |
| Input set-up time | $t_{ISU}$ | 6 | - | ns | $C_{card} \leq 10$ pF (1 card) |
| Input hold time | $t_{IH}$ | 0.8 | - | ns | $C_{card} \leq 10$ pF (1 card) |
| **Output CMD** (referenced to CLK rising edge) | | | | | |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | | 13.7 | ns | $C_L \leq 30$ pF (1 card) |
| Output Hold time | $T_{OH}$ | 1.5 | - | ns | $C_L \geq 15$ pF (1 card) |
| **Inputs DAT** (referenced to CLK rising and falling edges) | | | | | |
| Input set-up time | $t_{ISU2x}$ | 3 | - | ns | $C_{card} \leq 10$ pF (1 card) |
| Input hold time | $t_{IH2x}$ | 0.8 | - | ns | $C_{card} \leq 10$ pF (1 card) |
| **Outputs DAT** (referenced to CLK rising and falling edges) | | | | | |
| Output Delay time during Data Transfer Mode | $t_{ODLY2x}$ | - | 7.0 | ns | $C_L \leq 25$ pF (1 card) |
| Output Hold time | $T_{OH2x}$ | 1.5 | - | ns | $C_L \geq 15$ pF (1 card) |

**Bus Timings – Parameters Values (DDR50 mode)**

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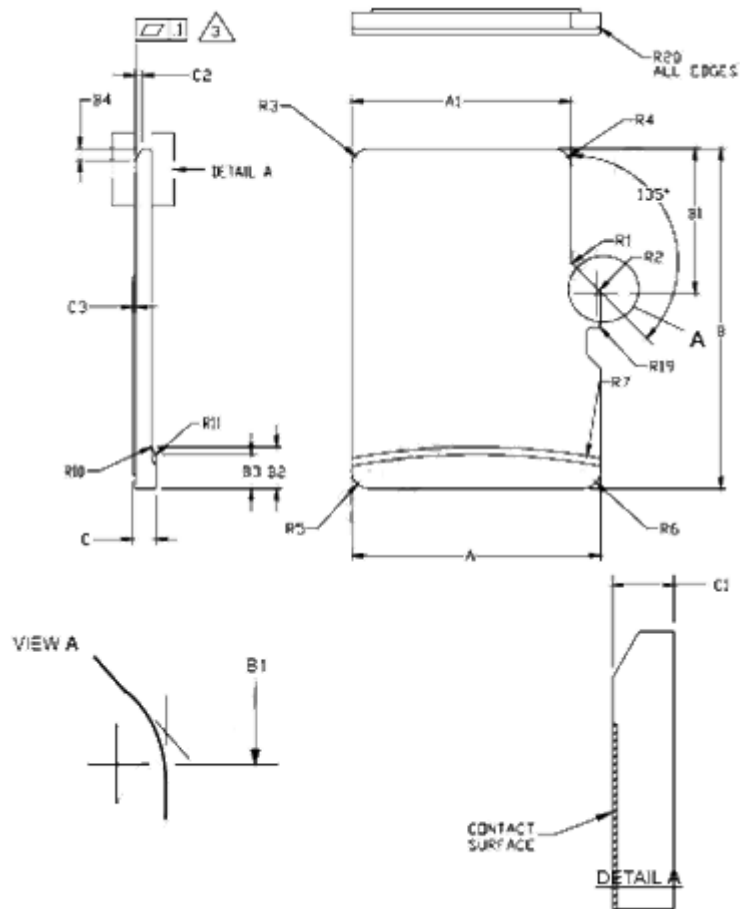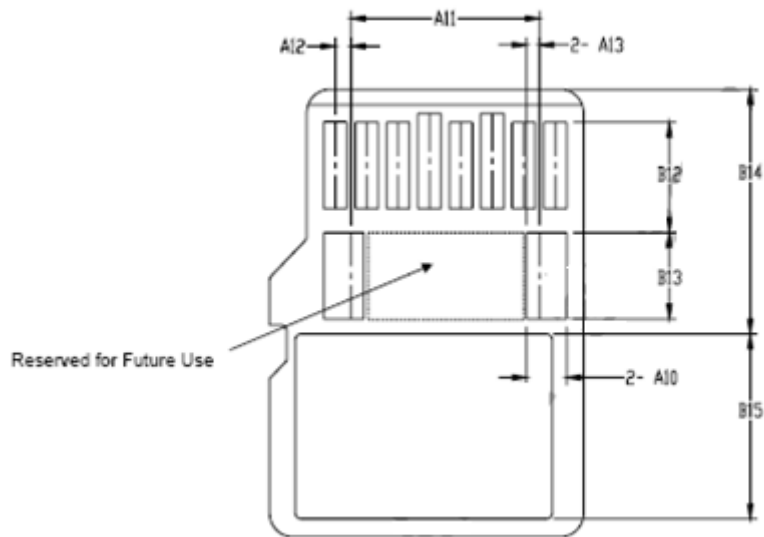
# 6. Interface

## 6.1. Pad Assignment and Descriptions
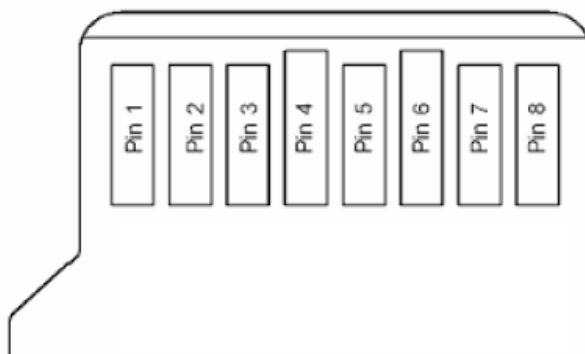


| pin | SD Mode | | | SPI Mode | | |
|---|---|---|---|---|---|---|
| | Name | Type[1] | Description | Name | Type | Description |
| 1 | DAT2 | I/O/PP | Data Line[bit2] | RSV | | |
| 2 | CD/DAT3 [2] | I/O/PP [3] | Card Detect/ Data Line[bit3] | CS | I [3] | Chip Select (neg true) |
| 3 | CMD | PP | Command/Response | DI | I | Data In |
| 4 | $V_{DD}$ | S | Supply voltage | $V_{DD}$ | S | Supply voltage |
| 5 | CLK | I | Clock | SCLK | I | Clock |
| 6 | $V_{SS}$ | S | Supply voltage ground | $V_{SS}$ | S | Supply voltage ground |
| 7 | DAT0 | I/O/PP | Data Line[bit0] | DO | O/PP | Data Out |
| 8 | DAT1 | I/O/PP | Data Line[bit1] | RSV | | |

(1) S: power supply, I: input; O: output using push-pull drivers; PP:I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3)are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should

drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

| Name | Width | Description |
|---|---|---|
| CID | 128bit | Card identification number; card individual number for identification. **Mandatory** |
| RCA[1] | 16bit | Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory** |
| DSR | 16bit | Driver Stage Register; to configure the card's output drivers. **Optional** |
| CSD | 128bit | Card Specific Data; information about the card operation conditions. **Mandatory** |
| SCR | 64bit | SD Configuration Register; information about the SD Memory Card's Special Features capabilities  **Mandatory** |
| OCR | 32bit | Operation conditions register. **Mandatory.** |
| SSR | 512bit | SD Status; information about the card proprietary features **Mandatory** |
| OCR | 32bit | Card Status; information about the card status **Mandatory** |

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# 7. Physical Dimension

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| | COMMON DIMENSIONS | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | 10.90 | 11.00 | 11.10 | |
| A1 | 9.60 | 9.70 | 9.80 | |
| A2 | - | 3.85 | - | BASIC |
| A3 | 7.60 | 7.70 | 7.80 | |
| A4 | - | 1.10 | - | BASIC |
| A5 | 0.75 | 0.80 | 0.85 | |
| A6 | - | - | 8.50 | |
| A7 | 0.90 | - | - | |
| A8 | 0.60 | 0.70 | 0.80 | |
| A9 | 0.80 | - | - | |
| A10 | 1.35 | 1.40 | 1.45 | |
| A11 | 6.50 | 6.60 | 6.70 | |
| A12 | 0.50 | 0.55 | 0.60 | |
| A13 | 0.40 | 0.45 | 0.50 | |
| B | 14.90 | 15.00 | 15.10 | |
| B1 | 6.30 | 6.40 | 6.50 | |
| B2 | 1.64 | 1.84 | 2.04 | |
| B3 | 1.30 | 1.50 | 1.70 | |
| B4 | 0.42 | 0.52 | 0.62 | |
| B5 | 2.80 | 2.90 | 3.00 | |
| B6 | 5.50 | - | - | |
| B7 | 0.20 | 0.30 | 0.40 | |
| B8 | 1.00 | 1.10 | 1.20 | |
| B9 | - | - | 9.00 | |
| B10 | 7.80 | 7.90 | 8.00 | |
| B11 | 1.10 | 1.20 | 1.30 | |
| B12 | 3.60 | 3.70 | 3.80 | |
| B13 | 2.80 | 2.90 | 3.00 | |
| B14 | 8.20 | - | - | |
| B15 | - | - | 6.20 | |
| C | 0.90 | 1.00 | 1.10 | |
| C1 | 0.60 | 0.70 | 0.80 | |
| C2 | 0.20 | 0.30 | 0.40 | |
| C3 | 0.00 | - | 0.15 | |
| D1 | 1.00 | - | - | |
| D2 | 1.00 | - | - | |
| D3 | 1.00 | - | - | |
| R1 | 0.20 | 0.40 | 0.60 | |
| R2 | 0.20 | 0.40 | 0.60 | |
| R3 | 0.70 | 0.80 | 0.90 | |
| R4 | 0.70 | 0.80 | 0.90 | |
| R5 | 0.70 | 0.80 | 0.90 | |
| R6 | 0.70 | 0.80 | 0.90 | |
| R7 | 29.50 | 30.00 | 30.50 | |
| R10 | - | 0.20 | - | |
| R11 | - | 0.20 | - | |
| R17 | 0.10 | 0.20 | 0.30 | |
| R18 | 0.20 | 0.40 | 0.60 | |
| R19 | 0.05 | - | 0.20 | |
| R20 | 0.02 | - | 0.15 | |

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS ARE IN MILLIMETERS.

3. COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

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**Warning**

• Do not bend, crush, drop, or place heavy objects on top of the Product. Do not use tweezers, pliers, or similar items that could damage the Product. Take particular care when inserting or removing the Product. Stop using the Product when the Product does not work properly. Failure to follow these instructions could result in fire, damage to the Product and/or other property, and/or personal injury including burns and electric shock.

• Keep out of reach of small children. Accidental swallowing may cause suffocation or injury. Contact a doctor immediately if you suspect a child has swallowed the Product. .

• Do not directly touch the interface pins, put them in contact with metal, strike them with hard objects, or cause them to short. Do not expose to static electricity.

• Do not disassemble or modify the Product. This may cause electric shock, damage to the Product, or fire.


Notes on usage

• The Product contains nonvolatile semiconductor memory. Do not use the Product in accordance with a method of usage other than that written in the manual. This may cause the destruction or loss of data.

• To protect against accidental data loss, you should back up your data frequently on more than one type of storage media. **** Corporation assumes no liability for destruction or loss of data recorded on the Card for any reason.

• When used over a long period of time or repeatedly, the reading, writing and deleting capabilities of the Product will eventually fail, and the performance speed of the Product may decrease below the original speed specific to the Product's applicable class.

• If the Product is to be transferred or destroyed, note that the data it contained may still be recoverable unless it is permanently deleted by third-party deletion software or similar means beforehand.


**Product applications and design.**


Product is intended for use in general electronics applications (e.g., computers, personal equipment, office equipment, measuring equipment, industrial robots and home electronics appliances) or for specific applications as expressly stated in this document. Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact ("Unintended Use"). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for Unintended Use unless specifically permitted in this document.


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