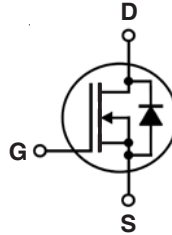


High Voltage Depletion Mode MOSFET

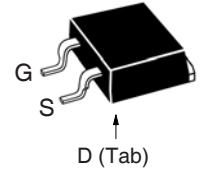
IXTA1R6N100D2HV

$V_{DSX} = 1000V$
 $I_{D(on)} \geq 1.6A$
 $R_{DS(on)} \leq 10\Omega$

N-Channel



TO-263HV



G = Gate D = Drain
 S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSX}	$T_J = 25^\circ C$ to $150^\circ C$	1000	V
V_{GSX}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
P_D	$T_C = 25^\circ C$	100	W
T_J		- 55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		- 55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Force	10.65 / 2.2..14.6	N/lb
Weight		2.5	g

Features

- High Voltage package
- High Blocking Voltage
- Normally ON Mode
- International Standard Package
- Molding Epoxies Meet UL94 V-0 Flammability Classification

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Audio Amplifiers
- Start-Up Circuits
- Protection Circuits
- Ramp Generators
- Current Regulators
- Active Loads

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSX}	$V_{GS} = -5V, I_D = 250\mu A$	1000		V
$V_{GS(off)}$	$V_{DS} = 25V, I_D = 100\mu A$	- 2.5		V
I_{GSX}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100 nA
$I_{DSX(off)}$	$V_{DS} = V_{DSX}, V_{GS} = -5V$ $T_J = 125^\circ C$			2 μA 25 μA
$R_{DS(on)}$	$V_{GS} = 0V, I_D = 0.8A$, Note 1			10 Ω
$I_{D(on)}$	$V_{GS} = 0V, V_{DS} = 50V$, Note 1	1.6		A

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 30\text{V}$, $I_D = 0.8\text{A}$, Note 1	0.65	1.10	S
C_{iss}	$V_{GS} = -10\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		645	pF
C_{oss}			43	pF
C_{rss}			11	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = \pm 5\text{V}$, $V_{DS} = 500\text{V}$, $I_D = 0.8\text{A}$ $R_G = 5\Omega$ (External)		27	ns
t_r			65	ns
$t_{d(off)}$			34	ns
t_f			41	ns
$Q_{g(on)}$	$V_{GS} = 5\text{V}$, $V_{DS} = 500\text{V}$, $I_D = 0.8\text{A}$		27.0	nC
Q_{gs}			1.6	nC
Q_{gd}			13.5	nC
R_{thJC}				1.25 $^\circ\text{C}/\text{W}$

Safe-Operating-Area Specification

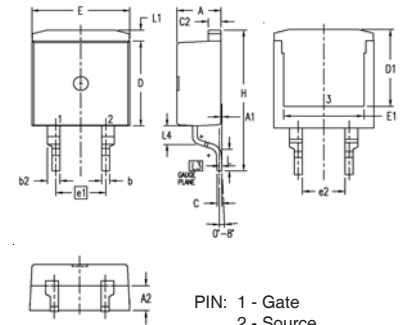
Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
SOA	$V_{DS} = 800\text{V}$, $I_D = 75\text{mA}$, $T_C = 75^\circ\text{C}$, $T_p = 5\text{s}$	60		W

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{SD}	$I_F = 1.6\text{A}$, $V_{GS} = -10\text{V}$, Note 1		0.8	1.3 V
t_{rr}	$I_F = 1.6\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$, $V_{GS} = -10\text{V}$		970	ns
I_{RM}			9.96	A
Q_{RM}			4.80	μC

Note 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

TO-263 HV Outline



PIN: 1 - Gate
2 - Source
3 - Drain

SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	.170	.185	4.30	4.70
A1	.000	.008	0.00	0.20
A2	.091	.098	2.30	2.50
b	.028	.035	0.70	0.90
b2	.046	.054	1.18	1.38
C	.018	.024	0.45	0.60
C2	.049	.055	1.25	1.40
D	.354	.370	9.00	9.40
D1	.311	.327	7.90	8.30
E	.386	.402	9.80	10.20
E1	.307	.323	7.80	8.20
e1	.200 BSC		5.08 BSC	
(e2)	.163	.174	4.13	4.43
H	.591	.614	15.00	15.60
L	.079	.102	2.00	2.60
L1	.039	.055	1.00	1.40
L3	.010 BSC		0.254 BSC	
(L4)	.071	.087	1.80	2.20

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2
by one or more of the following U.S. patents: 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

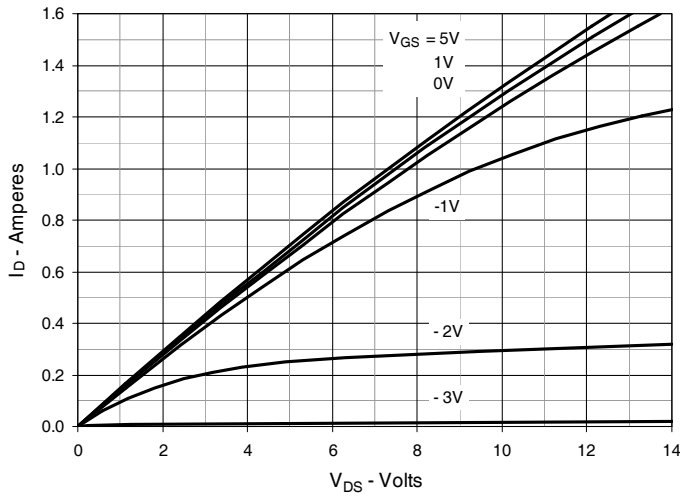
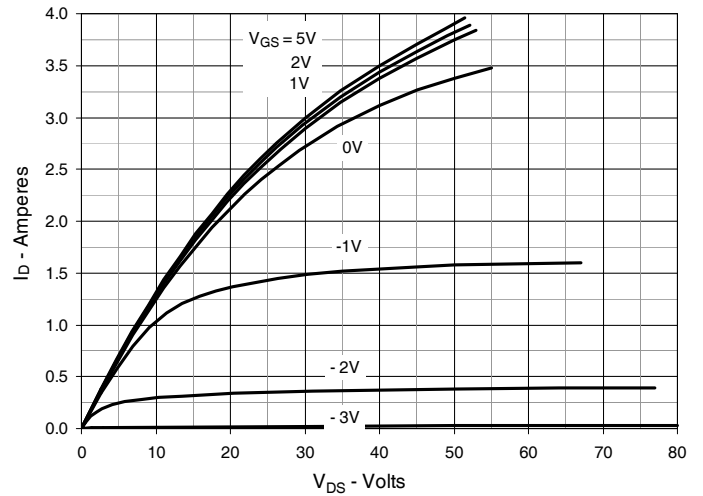
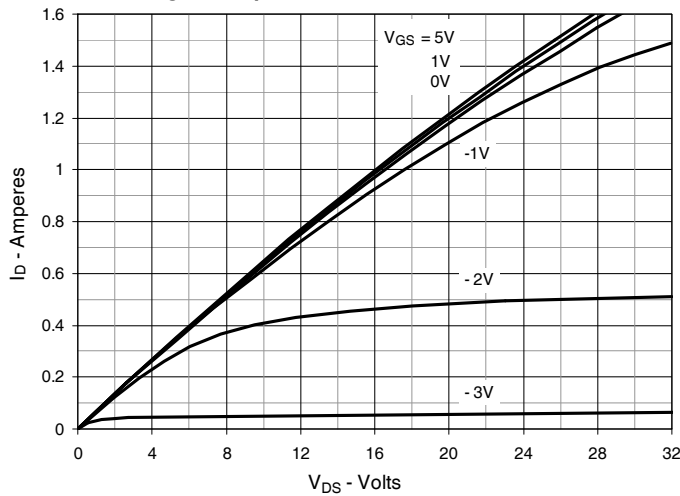
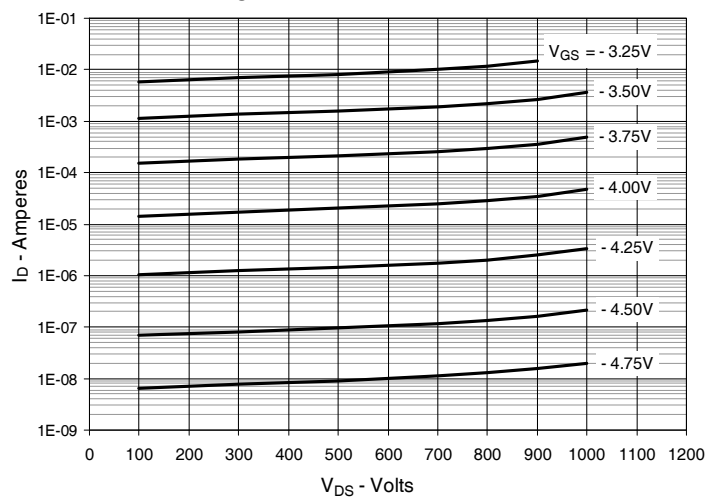
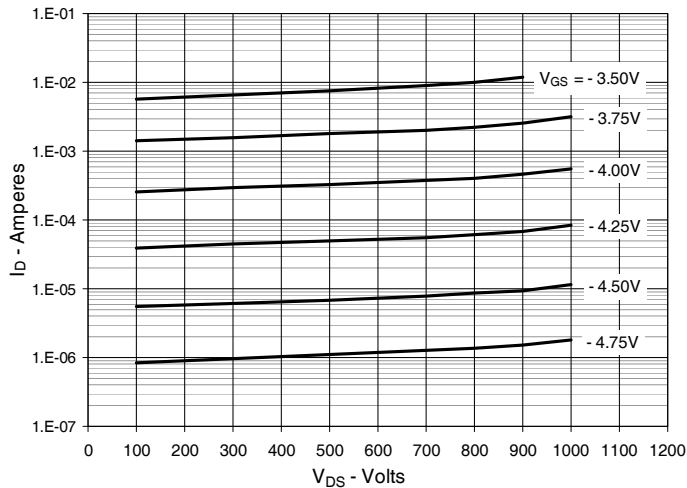
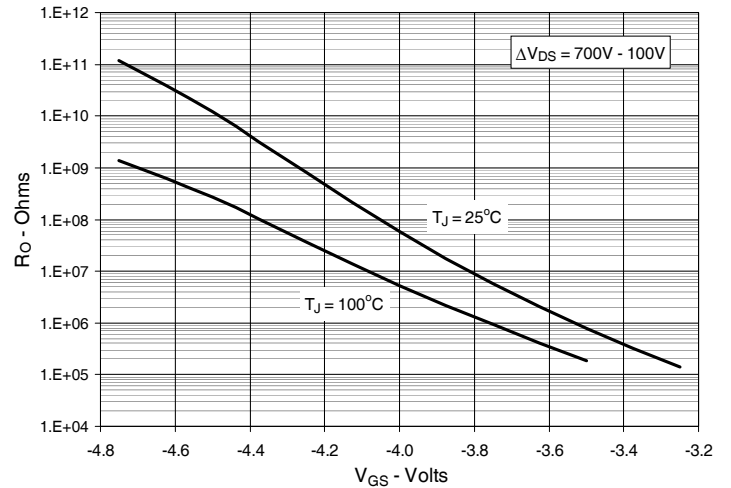
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. Drain Current @ $T_J = 25^\circ\text{C}$

Fig. 5. Drain Current @ $T_J = 100^\circ\text{C}$

Fig. 6. Dynamic Resistance vs. Gate Voltage


Fig. 7. Normalized $R_{DS(on)}$ vs. Junction Temperature

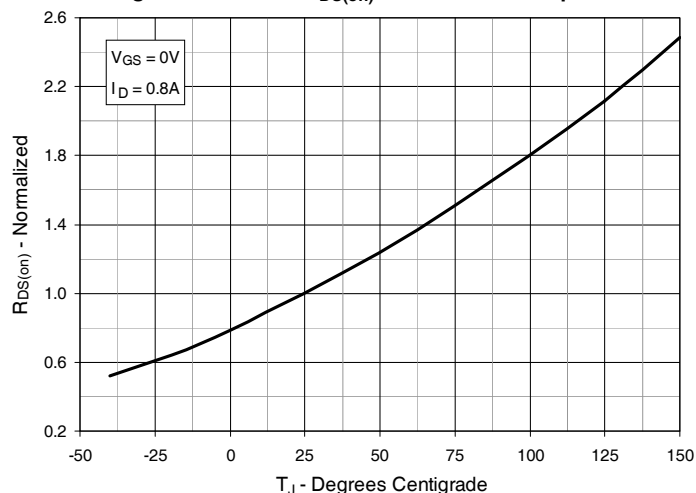


Fig. 8. $R_{DS(on)}$ Normalized to $I_D = 0.8A$ Value vs. Drain Current

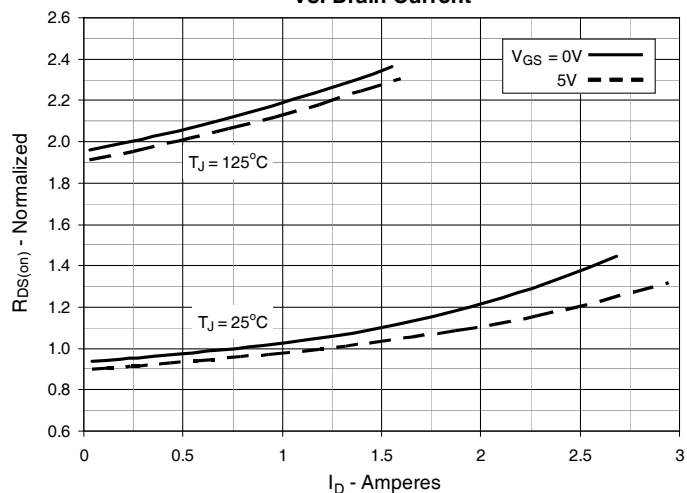


Fig. 9. Input Admittance

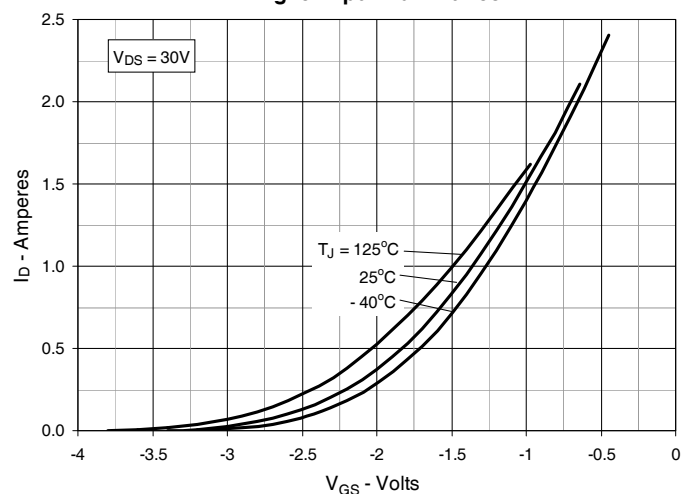


Fig. 10. Transconductance

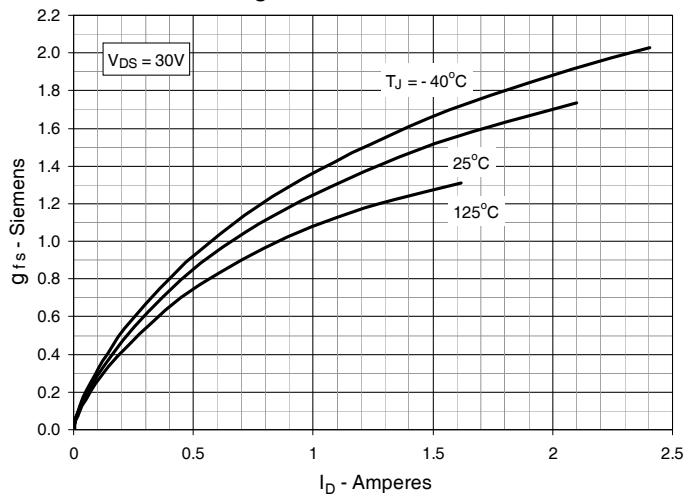


Fig. 11. Breakdown and Threshold Voltages vs. Junction Temperature

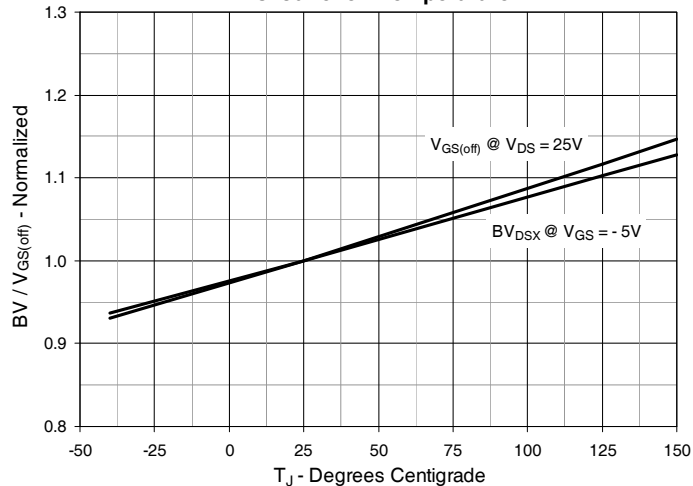


Fig. 12. Forward Voltage Drop of Intrinsic Diode

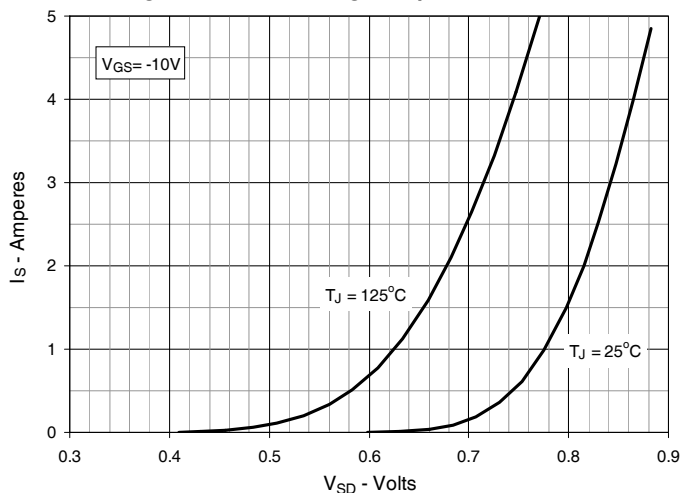


Fig. 13. Capacitance

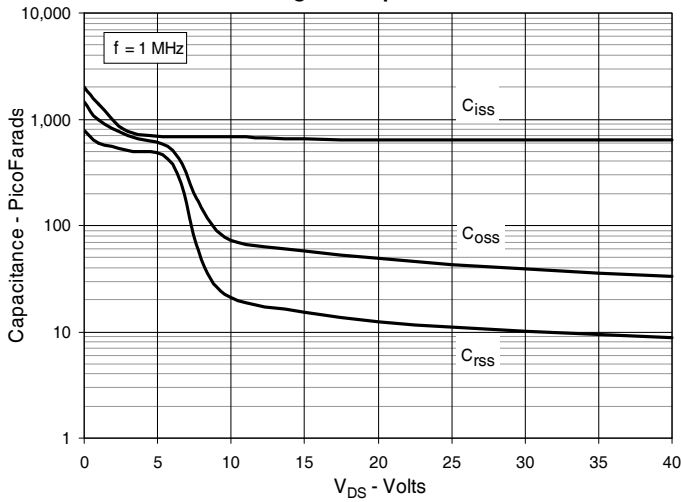


Fig. 14. Gate Charge

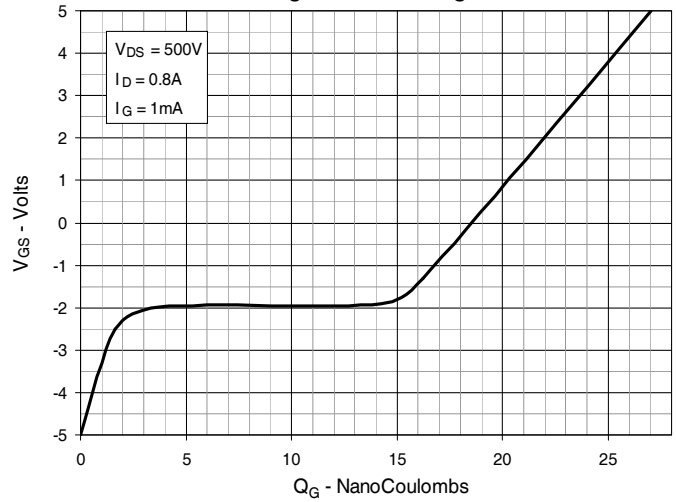


Fig. 15. Forward-Bias Safe Operating Area @ $T_C = 25^\circ\text{C}$

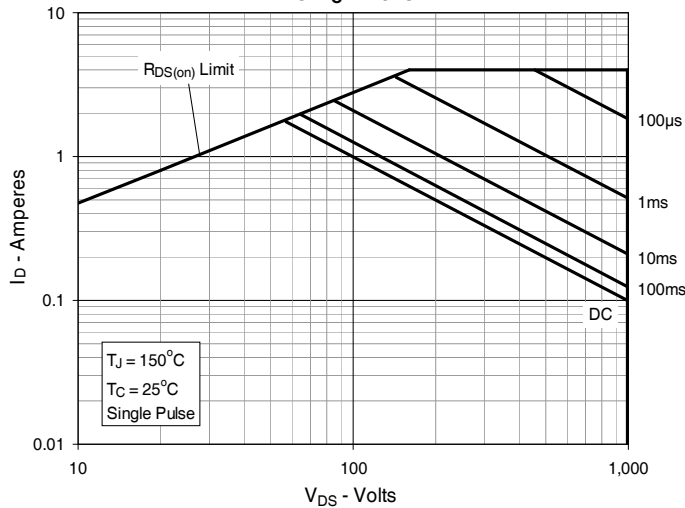


Fig. 16. Forward-Bias Safe Operating Area @ $T_C = 75^\circ\text{C}$

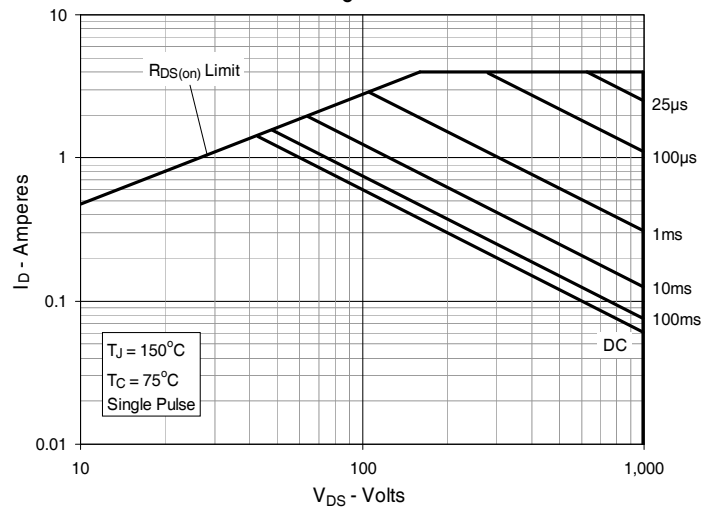
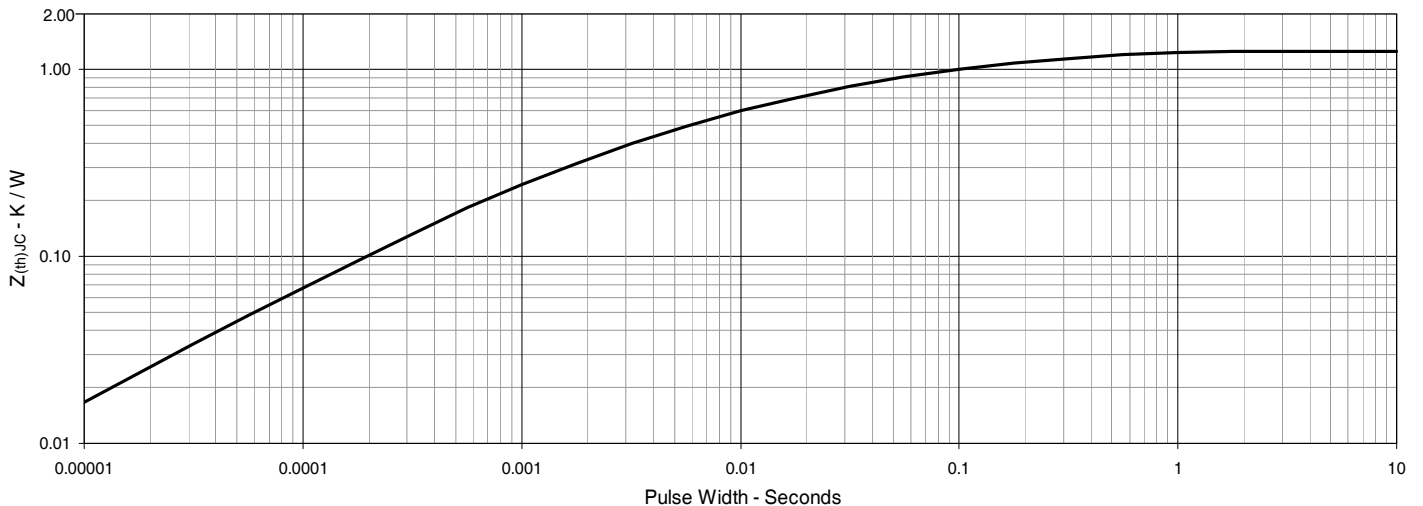


Fig. 17. Maximum Transient Thermal Impedance





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