

**TrenchT2™**  
**GigaMOS™ HiperFET™**  
**Power MOSFET**

**IXFZ520N075T2**

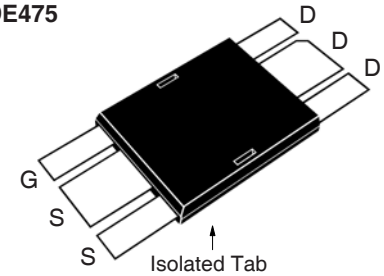
$V_{DSS} = 75V$   
 $I_{D25} = 420A$   
 $R_{DS(on)} \leq 1.6m\Omega$

(Electrically Isolated Tab)



N-Channel Enhancement Mode  
 Avalanche Rated  
 Fast Intrinsic Diode

DE475



G = Gate      D = Drain  
 S = Source

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ C$ to $175^\circ C$	75	V
$V_{DGR}$	$T_J = 25^\circ C$ to $175^\circ C$ , $R_{GS} = 1M\Omega$	75	V
$V_{GSS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ C$	420	A
$I_{DM}$	$T_C = 25^\circ C$ , Pulse Width Limited by $T_{JM}$	1560	A
$I_A$	$T_C = 25^\circ C$	200	A
$E_{AS}$	$T_C = 25^\circ C$	3	J
$P_D$	$T_C = 25^\circ C$	600	W
$T_J$		-55 ... +175	$^\circ C$
$T_{JM}$		175	$^\circ C$
$T_{stg}$		-55 ... +175	$^\circ C$
$V_{ISOL}$	50/60 Hz, RMS	$t = 1$ minute	2500 V~
	$I_{ISOL} \leq 1mA$	$t = 1$ second	3000 V~
$T_L$	1.6mm (0.062 in.) from Case for 10s	300	$^\circ C$
$T_{SOLD}$	Plastic Body for 10s	260	$^\circ C$
$V_{ISOL}$	50/60 Hz, 1 Minute	2500	V~
$F_C$	Mounting Force	20..120 / 4.5..27	N/lb.
Weight		3	g

**Features**

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Substrate
  - Excellent Thermal Transfer
  - Increased Temperature and Power Cycling Capability
  - High Isolation Voltage (2500V~)
- 175°C Operating Temperature
- Very High Current Handling Capability
- Fast Intrinsic Diode
- Avalanche Rated
- Very Low  $R_{DS(on)}$

**Advantages**

- Easy to Mount
- Space Savings
- High Power Density

**Applications**

- DC-DC Converters and Off-Line UPS
- Primary-Side Switch
- High Speed Power Switching Applications

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V, I_D = 3mA$	75		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 8mA$	2.0		V
$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$			$\pm 200$ nA
$I_{DSS}$	$V_{DS} = V_{DSS}, V_{GS} = 0V$ $T_J = 150^\circ C$			10 $\mu A$
				1.5 mA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 100A$ , Note 1			1.6 m $\Omega$

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 10\text{V}$ , $I_D = 60\text{A}$ , Note 1	95	160	S
$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		41	nF
$C_{oss}$			4150	pF
$C_{rss}$			530	pF
$R_{GI}$	Gate Input Resistance		1.36	$\Omega$
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 200\text{A}$ $R_G = 1\Omega$ (External)		48	ns
$t_r$			36	ns
$t_{d(off)}$			80	ns
$t_f$			35	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 260\text{A}$		545	nC
$Q_{gs}$			177	nC
$Q_{gd}$			135	nC
$R_{thJC}$				0.25 $^\circ\text{C/W}$
$R_{thCS}$		0.15		$^\circ\text{C/W}$

**Source-Drain Diode**

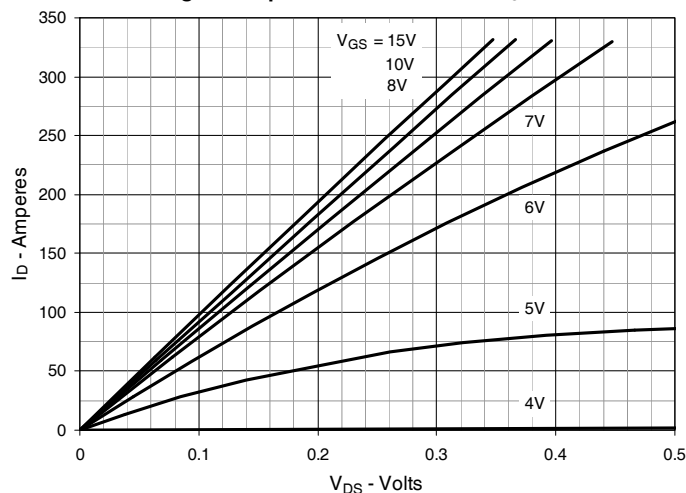
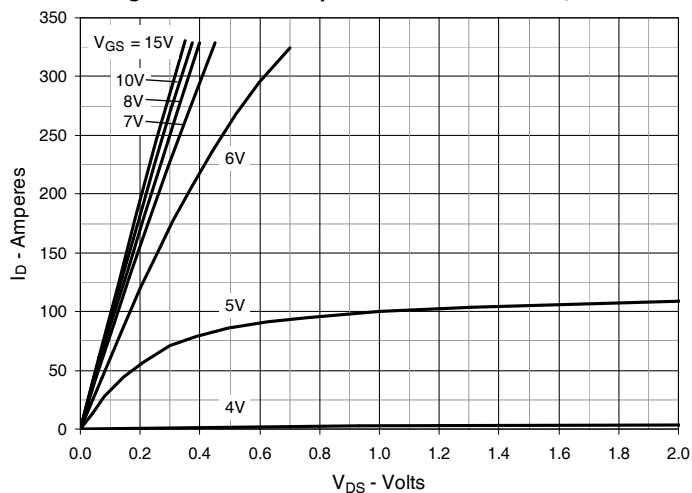
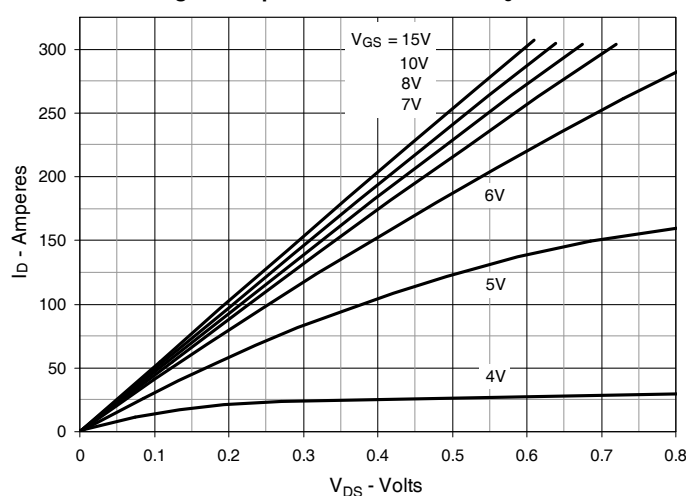
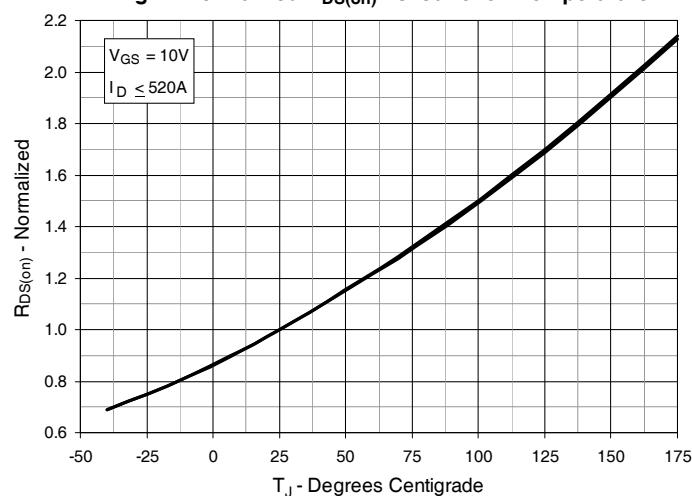
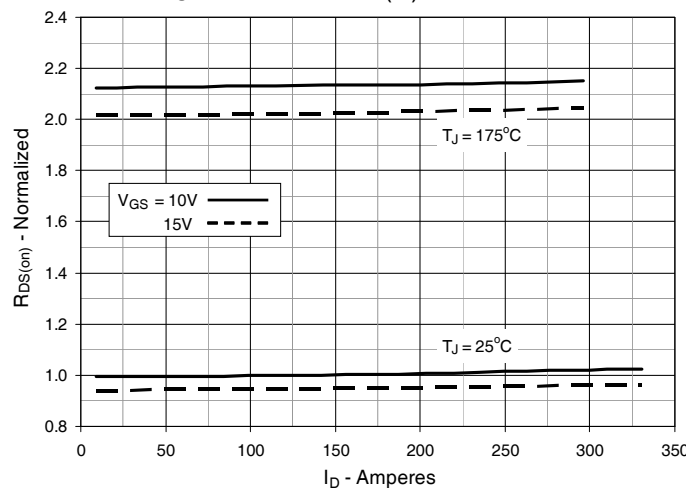
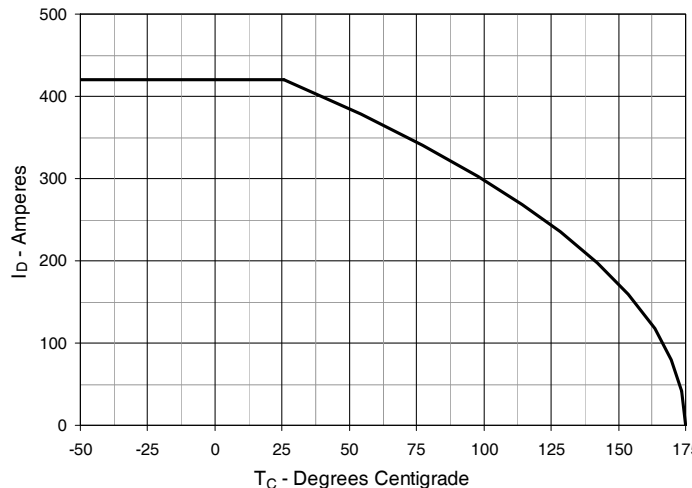
Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$I_S$	$V_{GS} = 0\text{V}$			520 A
$I_{SM}$	Repetitive, Pulse Width Limited by $T_{JM}$			1600 A
$V_{SD}$	$I_F = 100\text{A}$ , $V_{GS} = 0\text{V}$ , Note 1			1.25 V
$t_{rr}$	$I_F = 150\text{A}$ , $V_{GS} = 0\text{V}$ $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 37.5\text{V}$			150 ns
$I_{RM}$			7	A
$Q_{RM}$			357	nC

Note 1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .

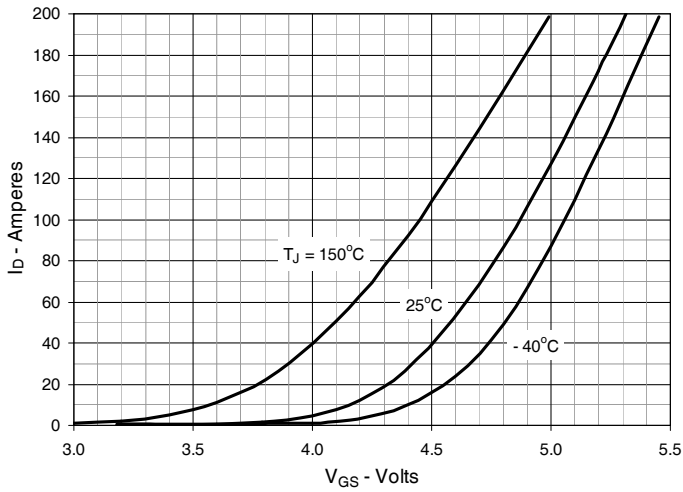
IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

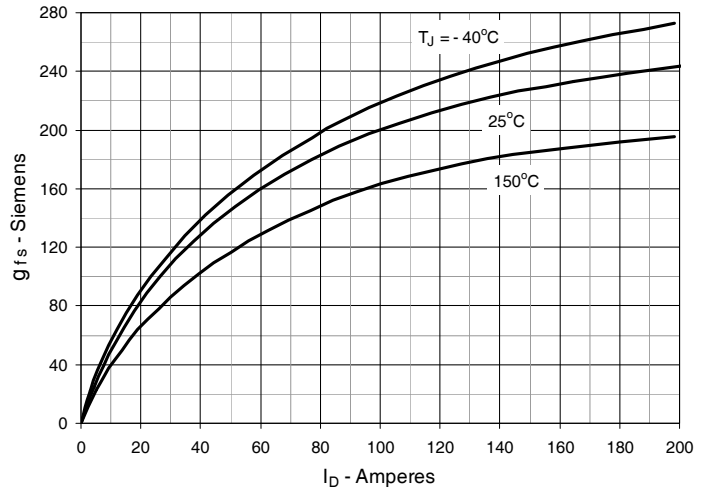
4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 3. Output Characteristics @  $T_J = 150^\circ\text{C}$** 

**Fig. 4. Normalized  $R_{DS(on)}$  vs. Junction Temperature**

**Fig. 5. Normalized  $R_{DS(on)}$  vs. Drain Current**

**Fig. 6. Drain Current vs. Case Temperature**


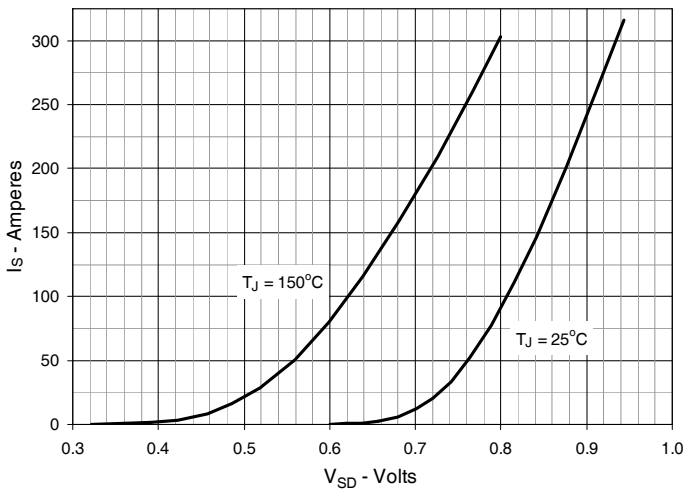
**Fig. 7. Input Admittance**



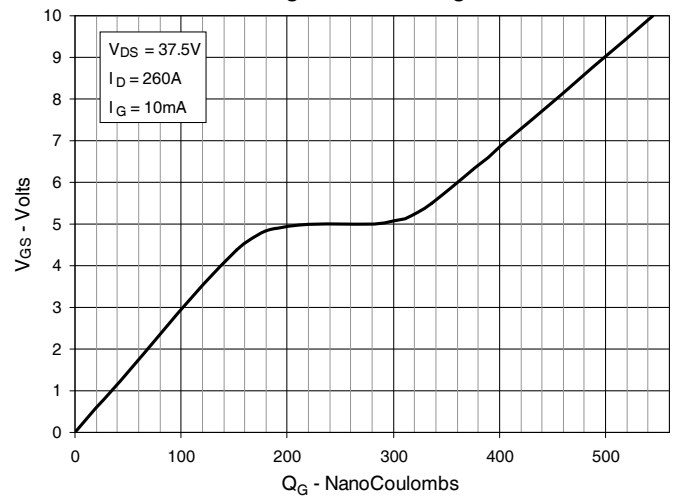
**Fig. 8. Transconductance**



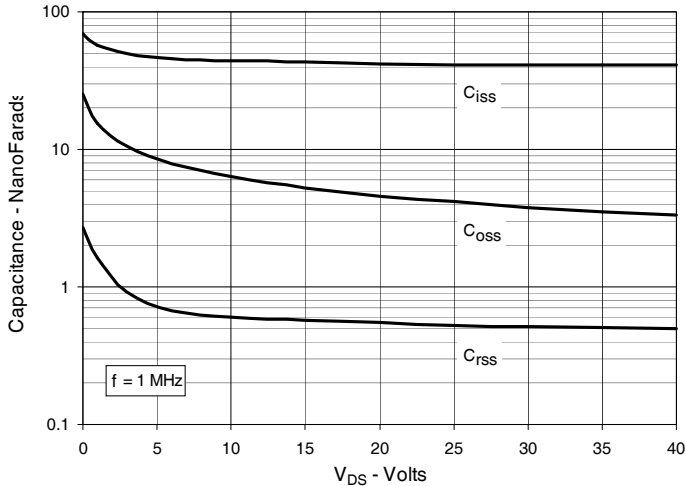
**Fig. 9. Forward Voltage Drop of Intrinsic Diode**



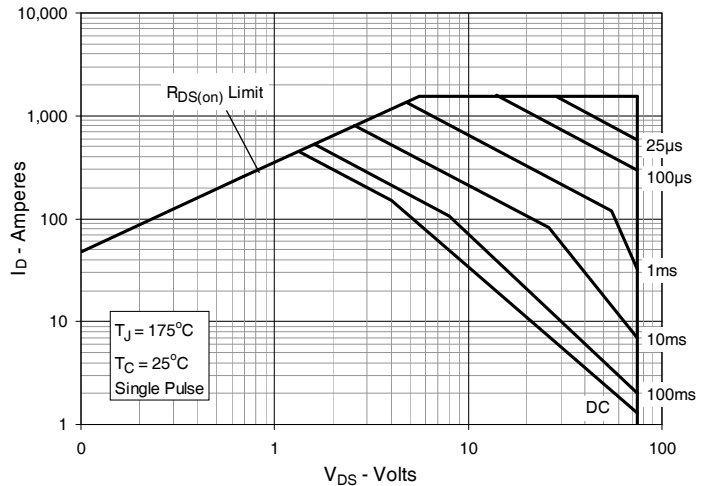
**Fig. 10. Gate Charge**

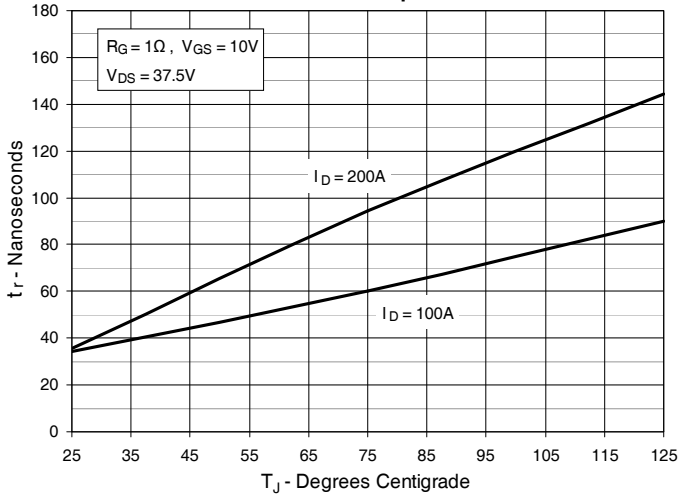
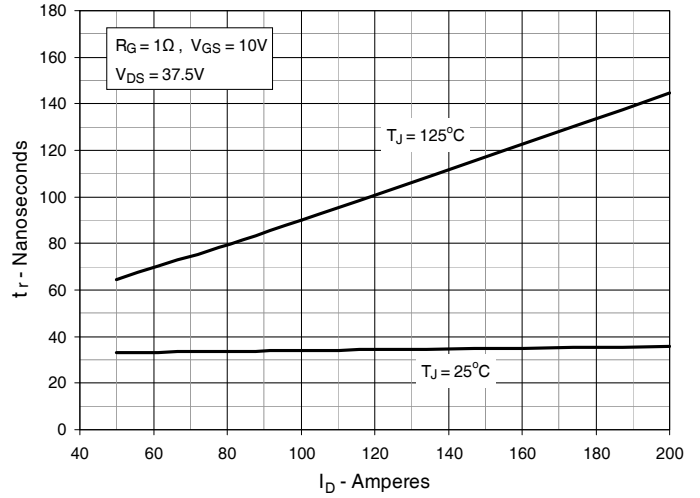
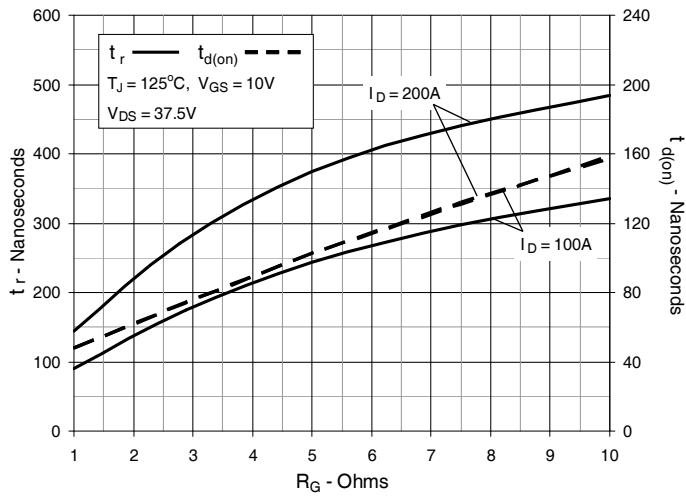
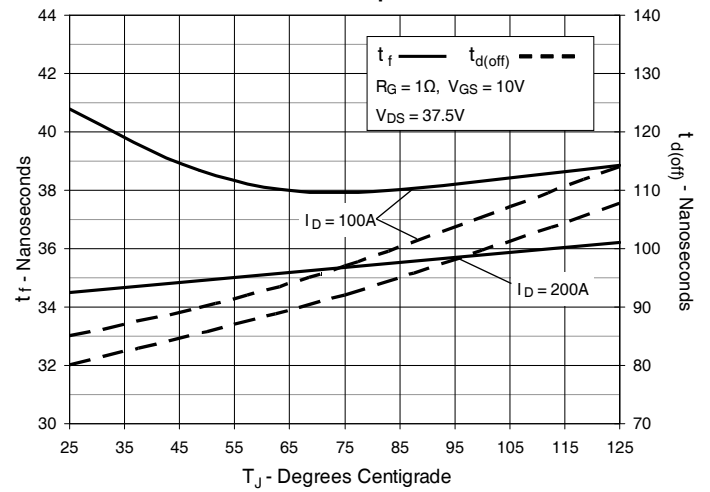
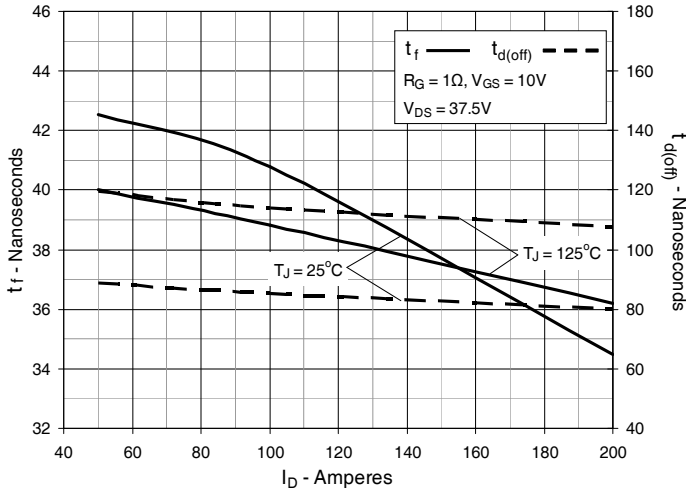
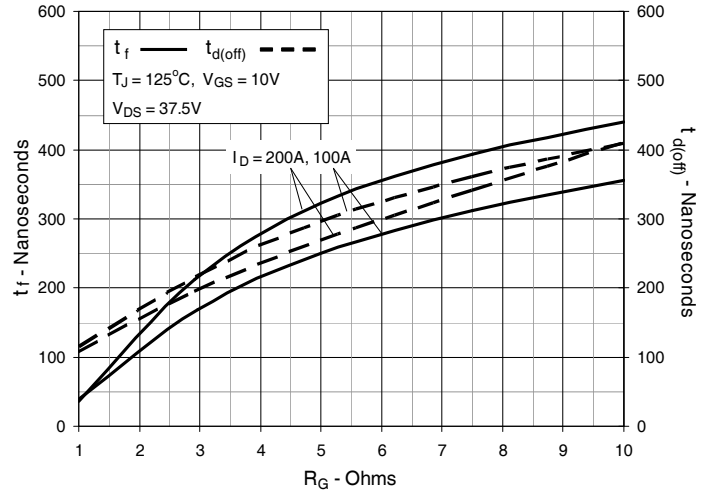


**Fig. 11. Capacitance**



**Fig. 12. Forward-Bias Safe Operating Area**



**Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature**

**Fig. 14. Resistive Turn-on Rise Time vs. Drain Current**

**Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance**

**Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature**

**Fig. 17. Resistive Turn-off Switching Times vs. Drain Current**

**Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance**






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