TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS167E

November 1997 - Revised October 2004

CD54/74HC240, CD54/74HCT240, CD74HC241, CD54/74HCT241, CD54/74HC244, CD54/74HCT244

High-Speed CMOS Logic
Octal Buffer/Line Drivers, Three-State

Features

- **HC/HCT240 Inverting**
- **HC/HCT241 Non-Inverting**
- **HC/HCT244 Non-Inverting**
- **Typical Propagation Delay = 8ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C for HC240**
- **Three-State Outputs**
- **Buffered Inputs**
- **High-Current Bus Driver Outputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC240 and 'HCT240 are inverting three-state buffers having two active-low output enables. The CD74HC241, 'HCT241, 'HC244 and 'HCT244 are non-inverting three-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC240F3A	-55 to 125	20 Ld CERDIP
CD54HC244F3A	-55 to 125	20 Ld CERDIP
CD54HCT240F3A	-55 to 125	20 Ld CERDIP
CD54HCT241F3A	-55 to 125	20 Ld CERDIP
CD54HCT244F3A	-55 to 125	20 Ld CERDIP
CD74HC240E	-55 to 125	20 Ld PDIP
CD74HC240M	-55 to 125	20 Ld SOIC
CD74HC240M96	-55 to 125	20 Ld SOIC
CD74HC241E	-55 to 125	20 Ld PDIP
CD74HC241M	-55 to 125	20 Ld SOIC
CD74HC241M96	-55 to 125	20 Ld SOIC
CD74HC244E	-55 to 125	20 Ld PDIP
CD74HC244M	-55 to 125	20 Ld SOIC
CD74HC244M96	-55 to 125	20 Ld SOIC
CD74HCT240E	-55 to 125	20 Ld PDIP
CD74HCT240M	-55 to 125	20 Ld SOIC
CD74HCT240M96	-55 to 125	20 Ld SOIC
CD74HCT240PW	-55 to 125	20 Ld TSSOP
CD74HCT240PWR	-55 to 125	20 Ld TSSOP
CD74HCT240PWT	-55 to 125	20 Ld TSSOP
CD74HCT241E	-55 to 125	20 Ld PDIP
CD74HCT241M	-55 to 125	20 Ld SOIC
CD74HCT241M96	-55 to 125	20 Ld SOIC
CD74HCT244E	-55 to 125	20 Ld PDIP
CD74HCT244M	-55 to 125	20 Ld SOIC
CD74HCT244M96	-55 to 125	20 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.
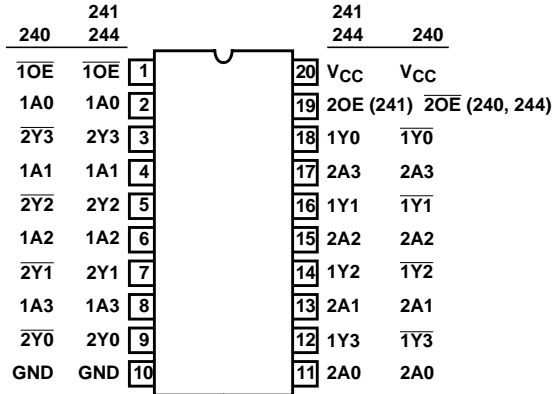
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Pinout

**CD54HC240, CD54HCT240, CD54HCT241,
CD54HC244, CD54HCT244
(CERDIP)
CD74HC240, CD74HC241, CD74HCT241,
CD74HC244, CD74HCT244
(PDIP, SOIC)
CD74HCT240,
(PDIP, SOIC, TSSOP)**

TOP VIEW

240	241 244				241 244	240
$\overline{1OE}$	$\overline{1OE}$	1		20	V_{CC}	V_{CC}
1A0	1A0	2		19	2OE (241)	$\overline{2OE}$ (240, 244)
$\overline{2Y3}$	2Y3	3		18	1Y0	$\overline{1Y0}$
1A1	1A1	4		17	2A3	2A3
$\overline{2Y2}$	2Y2	5		16	1Y1	$\overline{1Y1}$
1A2	1A2	6		15	2A2	2A2
$\overline{2Y1}$	2Y1	7		14	1Y2	$\overline{1Y2}$
1A3	1A3	8		13	2A1	2A1
$\overline{2Y0}$	2Y0	9		12	1Y3	$\overline{1Y3}$
GND	GND	10		11	2A0	2A0

Functional Diagram

						241 AND 244	240
1A0	2			18	1Y0		$\overline{1Y0}$
1A1	4			16	1Y1		$\overline{1Y1}$
1A2	6			14	1Y2		$\overline{1Y2}$
1A3	8			12	1Y3		$\overline{1Y3}$
2A0	11			9	2Y0		$\overline{2Y0}$
2A1	13			7	2Y1		$\overline{2Y1}$
2A2	15			5	2Y2		$\overline{2Y2}$
2A3	17			3	2Y3		$\overline{2Y3}$

240 AND 244 / 241

$\overline{1OE}$ $\overline{1OE}$ 1

$\overline{2OE}$ 2OE 19

V_{CC} = 20
GND = 10
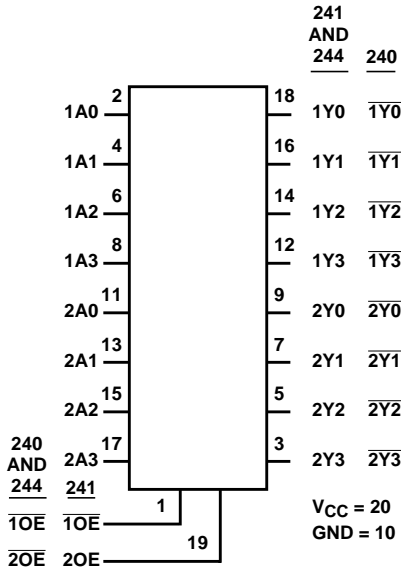
Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
  For -0.5V < V_O < V_{CC} + 0.5V . . . . ±35mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±70mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA}
  E (PDIP) Package . . . . 69°C/W
  M (SOIC) Package . . . . 58°C/W
  PW (TSSOP) Package . . . . 83°C/W
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
  (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A) . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
  HC Types . . . . .2V to 6V
  HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance wIth JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications   (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	-	6	-	-	±0.5	-	±0.5	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	-	5.5	-	-	±0.5	-	±5	-	±10	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
HCT240	
nA0-A3	1.5
$\overline{1OE}$	0.7
$\overline{2OE}$	0.7
HCT241	
nA0-A3	0.7
$\overline{1OE}$	0.7
2OE	1.5
HCT244	
nA0-A3	0.7
$\overline{1OE}$	0.7
$\overline{2OE}$	0.7

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications $C_L = 50pF$, Input t_r, $t_f = 6ns$

PARAMETER	SYMBOL	TEST CONDI-TIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C TYP	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C TYP	-55°C TO 125°C MAX	UNITS
HC TYPES													
Propagation Delay Data to Outputs HC240	t_{PLH}, t_{PHL}	$C_L = 50pF$	2	-	-	100	-	-	125	-	-	150	ns
			4.5	-	-	20	-	-	25	-	-	30	ns
		$C_L = 15pF$	5	-	8	-	-	-	-	-	-	-	ns
		$C_L = 50pF$	6	-	-	17	-	-	21	-	-	26	ns
Data to Outputs HC241	t_{PLH}, t_{PHL}	$C_L = 50pF$	2	-	-	110	-	-	140	-	-	165	ns
			4.5	-	-	22	-	-	28	-	-	33	ns
		$C_L = 15pF$	5	-	9	-	-	-	-	-	-	-	ns
		$C_L = 50pF$	6	-	-	19	-	-	24	-	-	28	ns
Data to Outputs HC244	t_{PLH}, t_{PHL}	$C_L = 50pF$	2	-	-	110	-	-	140	-	-	165	ns
			4.5	-	-	22	-	-	28	-	-	33	ns
		$C_L = 15pF$	5	-	9	-	-	-	-	-	-	-	ns
		$C_L = 50pF$	6	-	-	19	-	-	24	-	-	28	ns
Output Enable and Disable Time	t_{THL}, t_{TLH}	$C_L = 50pF$	2	-	-	150	-	-	190	-	-	225	ns
			4.5	-	-	30	-	-	38	-	-	45	ns
			5	-	12	-	-	-	-	-	-	-	ns
			6	-	-	26	-	-	33	-	-	38	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50pF$	2	-	-	60	-	-	75	-	-	90	ns
			4.5	-	-	12	-	-	15	-	-	18	ns
			6	-	-	10	-	-	13	-	-	15	ns
Input Capacitance	C_I	$C_L = 50pF$	-	10	-	10	-	-	10	-	-	10	pF
Three-State Output Capacitance	C_O	$C_L = 50pF$	-	-	-	20	-	-	20	-	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	$C_L = 15pF$											
HC240			5	-	38	-	-	-	-	-	-	-	pF
HC241			5	-	34	-	-	-	-	-	-	-	pF
HC244			5	-	46	-	-	-	-	-	-	-	pF
HCT TYPES													
Propagation Delay Data to Outputs HCT240	t_{PHL}, t_{PLH}	$C_L = 50pF$	4.5	-	-	22	-	-	28	-	-	33	ns
		$C_L = 15pF$	5	-	9	-	-	-	-	-	-	-	ns
Data to Outputs HCT241	t_{PHL}, t_{PLH}	$C_L = 50pF$	4.5	-	-	25	-	-	31	-	-	38	ns
		$C_L = 15pF$	5	-	10	-	-	-	-	-	-	-	ns
Data to Outputs HCT244	t_{PHL}, t_{PLH}	$C_L = 50pF$	4.5	-	-	25	-	-	31	-	-	38	ns
		$C_L = 15pF$	5	-	10	-	-	-	-	-	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDI- TIONS	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Enable and Disable Times	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	30	-	-	38	-	-	45	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	4.5	-	-	12	-	-	15	-	-	18	ns
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	-	10	-	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}												
HCT240		-	5	-	40	-	-	-	-	-	-	-	pF
HCT241		-	5	-	38	-	-	-	-	-	-	-	pF
HCT244		-	5	-	40	-	-	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per channel.

4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
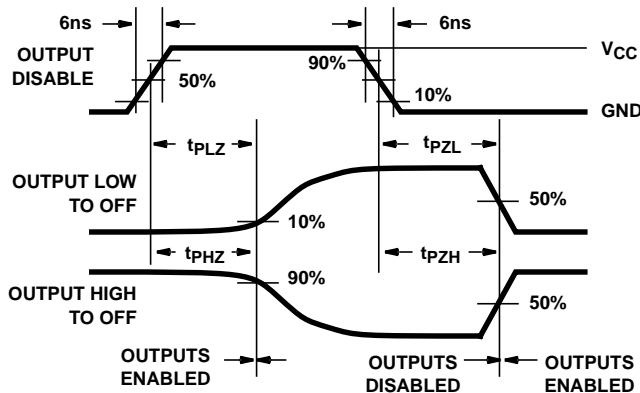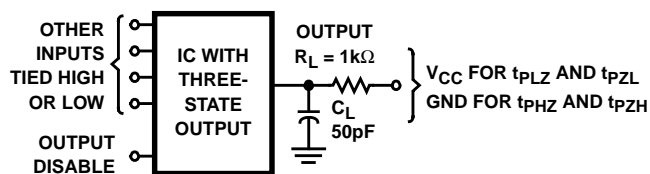

FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM

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Test Circuits and Waveforms (Continued)

NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC240F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8407401RA CD54HC240F3A	Samples
CD54HC244F	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC244F	Samples
CD54HC244F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8409601RA CD54HC244F3A	Samples
CD54HCT240F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8550501RA CD54HCT240F3A	Samples
CD54HCT241F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HCT241F3A	Samples
CD54HCT244F	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HCT244F	Samples
CD54HCT244F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8513001RA CD54HCT244F3A	Samples
CD74HC240E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC240E	Samples
CD74HC240M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC240M	Samples
CD74HC240M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC240M	Samples
CD74HC240MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC240M	Samples
CD74HC241E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC241E	Samples
CD74HC241EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC241E	Samples
CD74HC241M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC241M	Samples
CD74HC241M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC241M	Samples
CD74HC241M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC241M	Samples
CD74HC241MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC241M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC244E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC244E	Samples
CD74HC244EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC244E	Samples
CD74HC244M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples
CD74HC244M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples
CD74HC244M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples
CD74HC244M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples
CD74HC244MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC244M	Samples
CD74HCT240E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT240E	Samples
CD74HCT240EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT240E	Samples
CD74HCT240M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT240M	Samples
CD74HCT240M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT240M	Samples
CD74HCT240MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT240M	Samples
CD74HCT240PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK240	Samples
CD74HCT240PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK240	Samples
CD74HCT240PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK240	Samples
CD74HCT241E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT241E	Samples
CD74HCT241EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT241E	Samples
CD74HCT241M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT241M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT241M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT241M	Samples
CD74HCT241M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT241M	Samples
CD74HCT241MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT241M	Samples
CD74HCT244E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT244E	Samples
CD74HCT244EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT244E	Samples
CD74HCT244M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT244M	Samples
CD74HCT244M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT244M	Samples
CD74HCT244M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT244M	Samples
CD74HCT244ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT244M	Samples

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC240, CD54HC244, CD54HCT240, CD54HCT241, CD54HCT244, CD74HC240, CD74HC244, CD74HCT240, CD74HCT241, CD74HCT244 :

- Catalog: CD74HC240, CD74HC244, CD74HCT240, CD74HCT241, CD74HCT244

- Military: CD54HC240, CD54HC244, CD54HCT240, CD54HCT241, CD54HCT244

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC240M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HC241M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HC244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HCT240M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HCT240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CD74HCT240PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CD74HCT241M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74HCT244M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC240M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC241M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC244M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT240M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT240PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
CD74HCT240PWT	TSSOP	PW	20	250	367.0	367.0	38.0
CD74HCT241M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT244M96	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T**)   CERAMIC DUAL IN-LINE PACKAGE
14 LEADS SHOWN

DIM PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

16 9

0.260 (6,60)
0.240 (6,10)

1 8

0.070 (1,78)
0.045 (1,14) ⚠D

0.045 (1,14)
0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      ⚠C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      ⚠D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

$\dfrac{0.512\ (13,00)}{0.496\ (12,60)}$

20

11

$\dfrac{0.419\ (10,63)}{0.393\ (9,97)}$

$\dfrac{0.299\ (7,60)}{0.291\ (7,40)}$

1

10

Pin 1
Index Area

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\dfrac{0.012\ (0,30)}{0.004\ (0,10)}$

$\dfrac{0.013\ (0,33)}{0.008\ (0,20)}$

⌓ | 0.004 (0,10)

Gauge Plane

0.010 (0,25)

0°−8°

Seating Plane

$\dfrac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−4/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AC.

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6   18x1,27

20x0,55   18x1,27

20x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202−4/F   08/13

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Refer to IPC7351 for alternate board design.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 ⓜ

20   11

Ⓓ 4,50
    4,30

6,60
6,20

1   10

6,60
6,40

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

△ | 0,10

4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
         Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153

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PW (R–PDSO–G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284–5/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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