8-bit AVR Microcontroller

# ATmega324PB

**DATASHEET PRELIMINARY SUMMARY**

## Introduction

The Atmel® ATmega324PB is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega324PB achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

## Feature

High Performance, Low Power Atmel®AVR® 8-Bit Microcontroller Family

- Advanced RISC Architecture
  - 131 Powerful Instructions
  - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 32KBytes of In-System Self-Programmable Flash program memory
  - 1KBytes EEPROM
  - 2KBytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- Atmel QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix acquisition
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard

  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Peripheral Touch Controller (PTC)
    - Capacitive touch buttons, sliders and wheels
    - 32 Self-cap channels and 256 mutual cap channels
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - Three 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Ten PWM Channels
  - 8-channel 10-bit ADC
    - Differential mode with selectable gain at 1×, 10× or 200×
  - Three Programmable Serial USART
  - Two Master/Slave SPI Serial Interface
  - Two Byte-oriented 2-wire Serial Interface (Philips $I^2C$ compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
  - Clock failure detection mechanism and switch to 1MHz internal RC clock in case of failure
- I/O and Packages
  - 39 programmable I/O lines
  - 44-pin TQFP and 44-pin QFN/MLF
- Operating Voltage:
  - 1.8 - 5.5V
- Temperature Range:
  - -40°C to 105°C
- Speed Grade:
  - 0 - 4MHz @ 1.8 - 5.5V
  - 0 - 10MHz @ 2.7 - 5.5.V
  - 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active Mode: 0.4mA
  - Power-down Mode: 0.2µA
  - Power-save Mode: 1.3µA (Including 32kHz RTC)

# Table of Contents

# 1. Description

The Atmel® ATmega324PB is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega324PB achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

The Atmel AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in a single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega324PB provides the following features: 32K bytes of In-System Programmable Flash with Read-While-Write capabilities, 1Kbytes EEPROM, 2Kbytes SRAM, 39 general purpose I/O lines, 32 general purpose working registers, *five* flexible Timer/Counters with compare modes, internal and external interrupts, three serial programmable USART, two byte-oriented 2-wire Serial Interface (I2C), two SPI serial port, a 8-channel 10-bit ADC , a programmable Watchdog Timer with internal Oscillator, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming, Clock failure detection mechanism and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Interface, SPI port, and interrupt system to continue functioning. PTC with enabling up to 32 self-cap and 256 mutual-cap sensors. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. Also ability to run PTC in power-save mode/wake-up on touch and Dynamic on/off of PTC analog and digital portion. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer, PTC, and ADC to minimize switching noise during ADC conversions. In Standby mode, the crystal/ resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Composer allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega324PB is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega324PB is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

## 2. Configuration Summary

| Features | ATmega324PB |
|---|---|
| Pin count | 44 |
| Flash (KB) | 32 |
| SRAM (KB) | 2 |
| EEPROM (KB) | 1 |
| General Purpose I/O lines | 39 |
| SPI | 2 |
| TWI ($I^2C$) | 2 |
| USART | 3 |
| ADC | 10-bit 15ksps |
| ADC channels | 8 |
| AC | 1 |
| 8-bit Timer/Counters | 2 |
| 16-bit Timer/Counters | 3 |
| PWM channels | 10 |
| PTC | Available |
| Peripheral Touch Controller (PTC) channels (X- x Y-Lines) for mutual capacitance | 256 (16 x 16 ) |
| Peripheral Touch Controller (PTC) channels for self capacitance (Y-Lines only) | 32 |
| Clock Failure Detector (CFD) | Available |
| Output Compare Modulator (OCM1C2) | Available |

# 3. Ordering Information

| Speed [MHz] | Power Supply [V] | Ordering Code[2] | Package[1] | Operational Range |
|---|---|---|---|---|
| 20 | 1.8 - 5.5 | ATmega324PB-AU<br>ATmega324PB-AUR[3]<br>ATmega324PB-MU<br>ATmega324PB-MUR[3] | 44A<br>44A<br>44M1<br>44M1 | Industrial<br>(-40°C to 85°C) |
| | | ATmega324PB-AN<br>ATmega324PB-ANR[3]<br>ATmega324PB-MN<br>ATmega324PB-MNR[3] | 44A<br>44A<br>44M1<br>44M1 | Industrial<br>(-40°C to 105°C) |

Note: 1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.

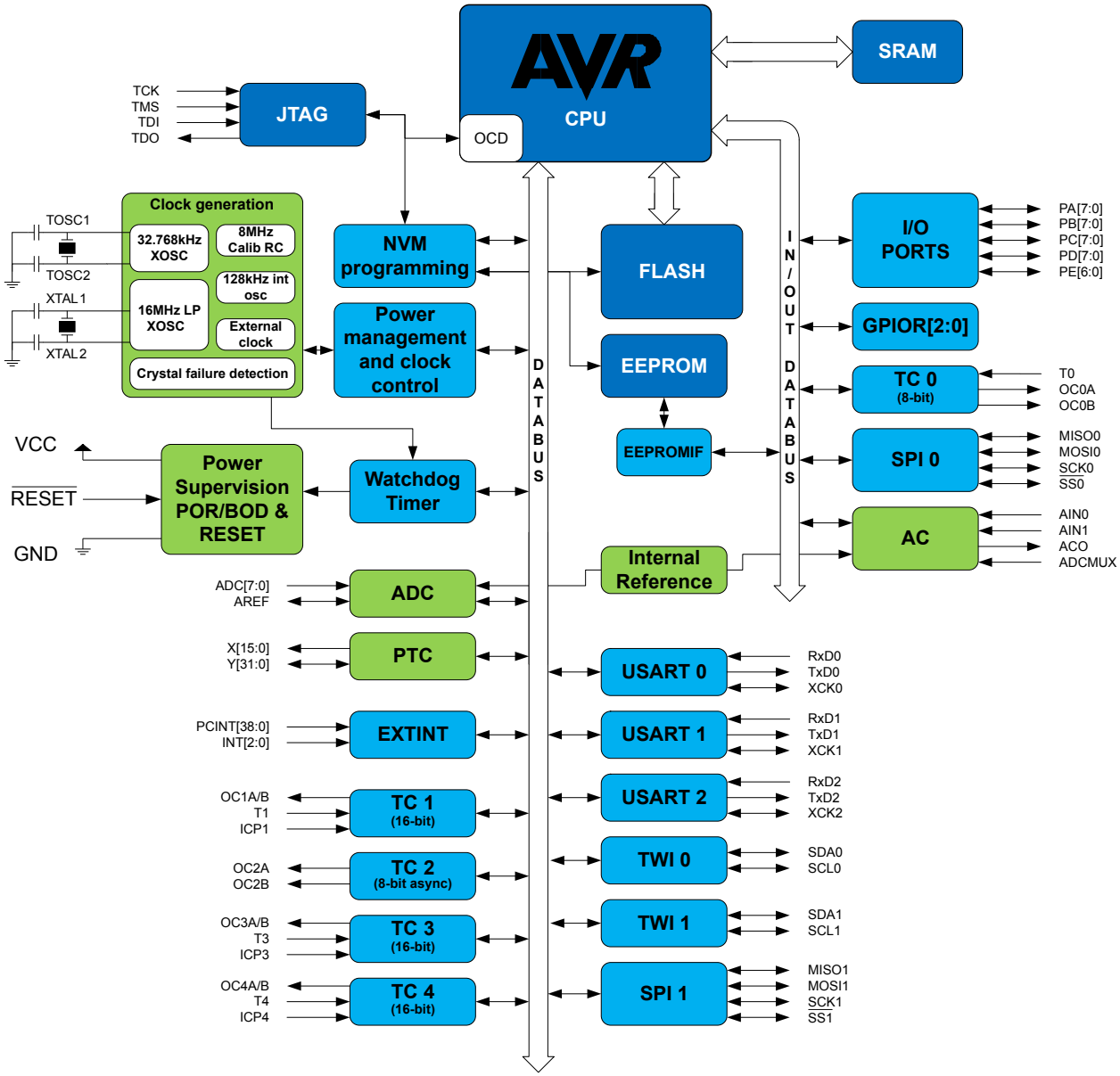
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. Tape & Reel.

| Package Type | |
|---|---|
| 44A | 44-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP) |
| 44M1 | 44-pad, 7 x 7 x 1.9mm body, Lead Pitch 0.50mm, Very-thin Fine pitch, Quad Flat No Lead Package/Quad Flat No-Lead/Micro Lead Frame Package (VQFN/QFN/MLF) |

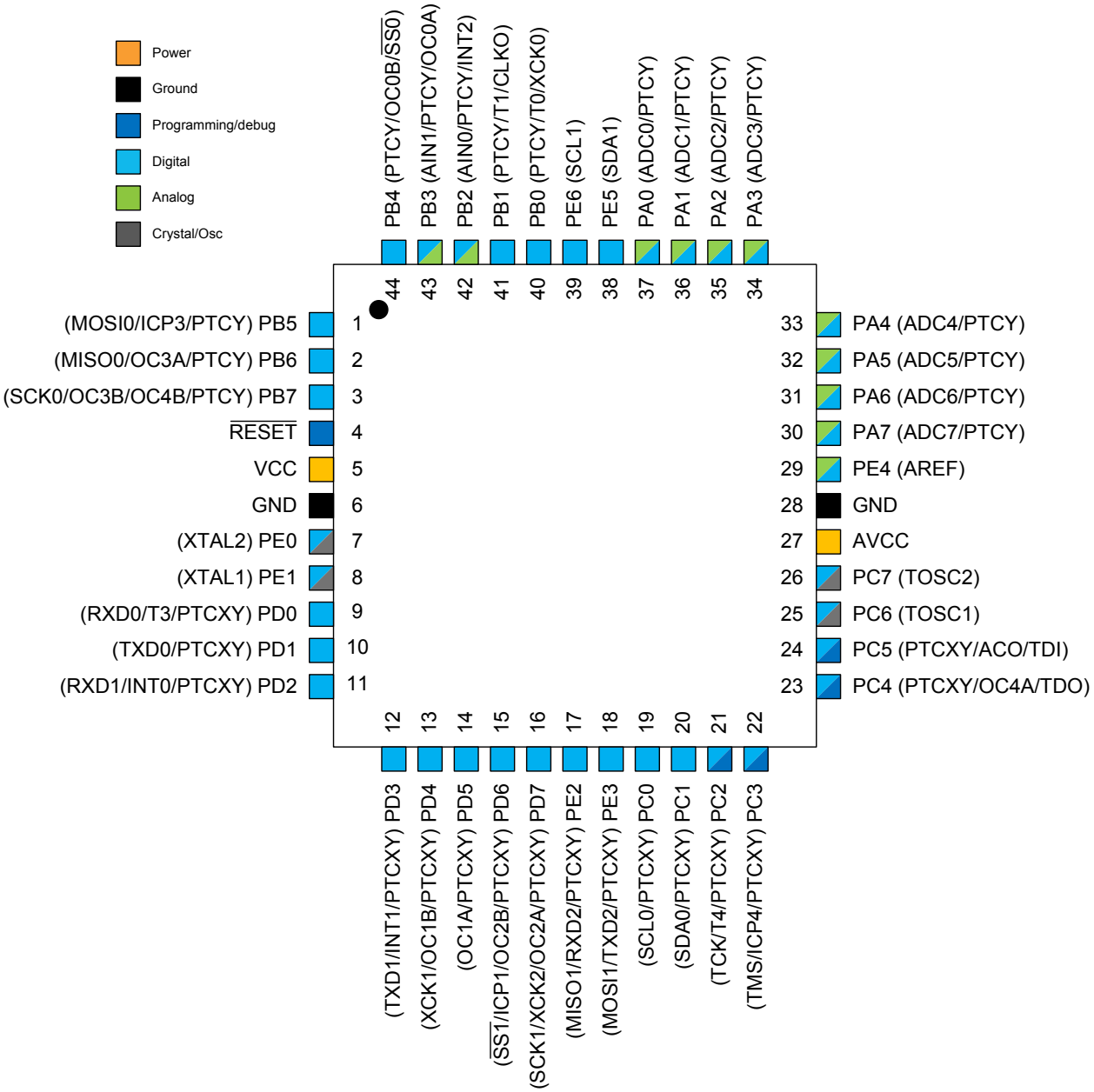
# 4. Block Diagram

**Figure 4-1 Block Diagram**



# 5. Pin Configurations

**Figure 5-1 Pinout ATmega324PB**




## 5.1. Pin Descriptions

### 5.1.1. VCC

Digital supply voltage.

### 5.1.2. GND

Ground.

### 5.1.3. Port A (PA[7:0])

This port serves as analog inputs to the Analog-to-digital Converter.

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

### 5.1.4. Port B (PB[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of various special features.

### 5.1.5. Port C (PC[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of the JTAG interface, along with special features.

### 5.1.6. Port D (PD[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of various special features.

### 5.1.7. Port E (PE6:0) XTAL1/XTAL2/AREF

This is a 7-bit bi-directional GPIO port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running. PE0 and PE1 are multiplexed with XTAL1 and XTAL2 input. PE4 is multiplexed with AREF for the A/D Converter.

### 5.1.8. $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

### 5.1.9. AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to $V_{CC}$, even if the ADC is not used. If the ADC is used, it should be connected to $V_{CC}$ through a low-pass filter.

# 6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

**Table 6-1 PORT Function Multiplexing**

| No. | PAD | EXTINT | PCINT | ADC/AC | PTC X | PTC Y | OSC | T/C # 0 | T/C # 1 | USART | I2C | SPI | JTAG |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | PB[5] | | PCINT13 | | | Y29 | | ICP3 | | | | MOSI0 | |
| 2 | PB[6] | | PCINT14 | | | Y30 | | OC3A | | | | MISO0 | |
| 3 | PB[7] | | PCINT15 | | | Y31 | | OC3B | OC4B | | | SCK0 | |
| 4 | $\overline{\text{RESET}}$ | | | | | | | | | | | | |
| 5 | VCC | | | | | | | | | | | | |
| 6 | GND | | | | | | | | | | | | |
| 7 | PE[0] | | PCINT32 | | | | XTAL2 | | | | | | |
| 8 | PE[1] | | PCINT33 | | | | XTAL1 | | | | | | |
| 9 | PD[0] | | PCINT24 | | X0 | Y8 | | T3 | | RxD0 | | | |
| 10 | PD[1] | | PCINT25 | | X1 | Y9 | | | | TxD0 | | | |
| 11 | PD[2] | INT0 | PCINT26 | | X2 | Y10 | | | | RxD1 | | | |
| 12 | PD[3] | INT1 | PCINT27 | | X3 | Y11 | | | | TXD1 | | | |
| 13 | PD[4] | | PCINT28 | | X4 | Y12 | | | OC1B | XCK1 | | | |
| 14 | PD[5] | | PCINT29 | | X5 | Y13 | | | OC1A | | | | |
| 15 | PD[6] | | PCINT30 | | X6 | Y14 | | OC2B | ICP1 | | | $\overline{\text{SS1}}$ | |
| 16 | PD[7] | | PCINT31 | | X7 | Y15 | | OC2A | | XCK2 | | SCK1 | |
| 17 | PE[2] | | | | X8 | Y16 | | | | RxD2 | | MISO1 | |
| 18 | PE[3] | | | | X9 | Y17 | | | | TxD2 | | MOSI1 | |
| 19 | PC[0] | | PCINT16 | | X10 | Y18 | | | | | SCL0 | | |
| 20 | PC[1] | | PCINT17 | | X11 | Y19 | | | | | SDA0 | | |
| 21 | PC[2] | | PCINT18 | | X12 | Y20 | | | T4 | | | | TCK |
| 22 | PC[3] | | PCINT19 | | X13 | Y21 | | | ICP4 | | | | TMS |
| 23 | PC[4] | | PCINT20 | | X14 | Y22 | | | OC4A | | | | TDO |
| 24 | PC[5] | | PCINT21 | ACO | X15 | Y23 | | | | | | | TDI |
| 25 | PC[6] | | PCINT22 | | | | TOSC1 | | | | | | |
| 26 | PC[7] | | PCINT23 | | | | TOSC2 | | | | | | |
| 27 | AVCC | | | | | | | | | | | | |
| 28 | GND | | | | | | | | | | | | |
| 29 | PE[4] | | | AREF | | | | | | | | | |
| 30 | PA[7] | | PCINT7 | ADC7 | | Y7 | | | | | | | |
| 31 | PA[6] | | PCINT6 | ADC6 | | Y6 | | | | | | | |
| 32 | PA[5] | | PCINT5 | ADC5 | | Y5 | | | | | | | |
| 33 | PA[4] | | PCINT4 | ADC4 | | Y4 | | | | | | | |
| 34 | PA[3] | | PCINT3 | ADC3 | | Y3 | | | | | | | |

| No. | PAD | EXTINT | PCINT | ADC/AC | PTC X | PTC Y | OSC | T/C # 0 | T/C # 1 | USART | I2C | SPI | JTAG |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 35 | PA[2] | | PCINT2 | ADC2 | | Y2 | | | | | | | |
| 36 | PA[1] | | PCINT1 | ADC1 | | Y1 | | | | | | | |
| 37 | PA[0] | | PCINT0 | ADC0 | | Y0 | | | | | | | |
| 38 | PE[5] | | | | | | | | | | SDA1 | | |
| 39 | PE[6] | | | | | | | | | | SCL1 | | |
| 40 | PB[0] | | PCINT8 | | | Y24 | | T0 | | XCK0 | | | |
| 41 | PB[1] | | PCINT9 | | | Y25 | CLKO | | T1 | | | | |
| 42 | PB[2] | INT2 | PCINT10 | AIN0 | | Y26 | | | | | | | |
| 43 | PB[3] | | PCINT11 | AIN1 | | Y27 | | OC0A | | | | | |
| 44 | PB[4] | | PCINT12 | | | Y28 | | OC0B | | | | $\overline{SS0}$ | |

# 7. General Information

## 7.1. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com/avr.

## 7.2. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

## 7.3. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

## 7.4. Capacitive Touch Sensing

### 7.4.1. QTouch Library

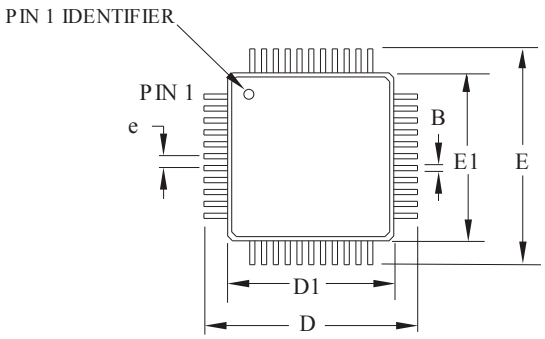
The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the Atmel QTouch and Atmel QMatrix® acquisition methods.

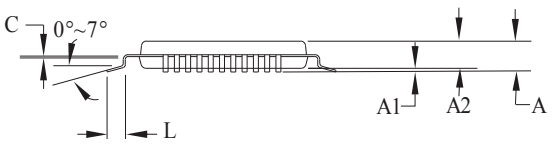
Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: http://www.atmel.com/technologies/touch/. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

# 8. Packaging Information

## 8.1. 44A




**COMMON DIMENSIONS**
(Unit of Measure = mm)

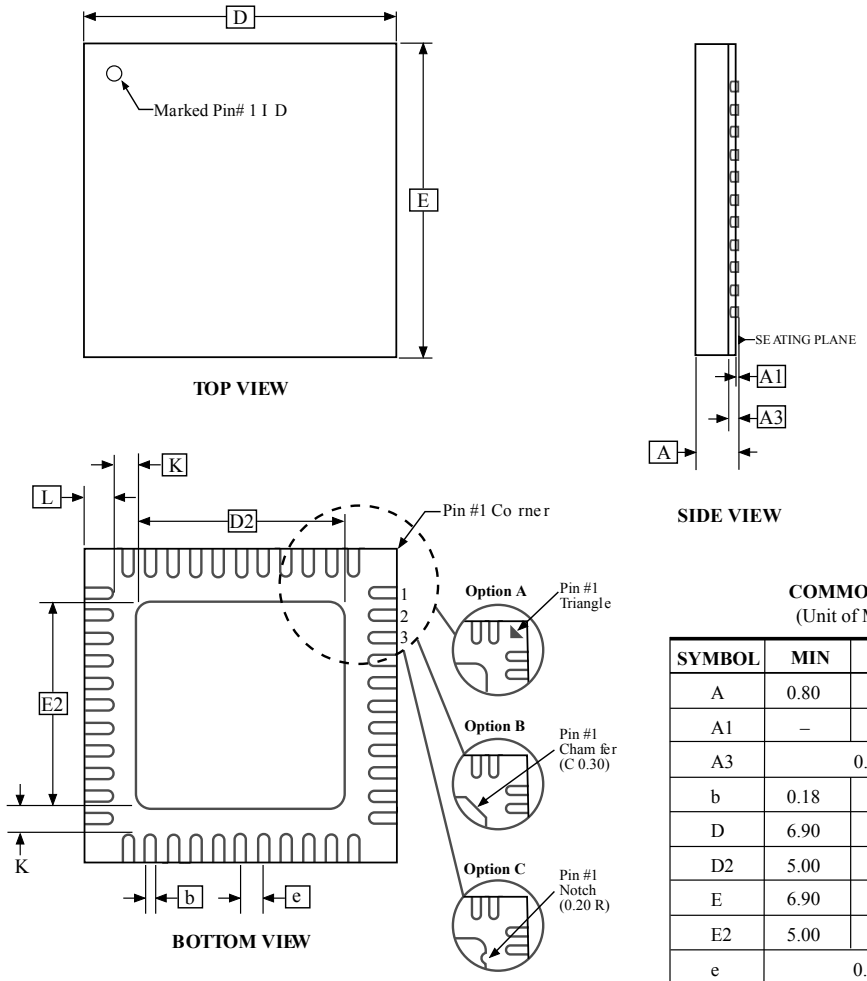
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | 0.37 | 0.45 | |
| C | 0.09 | (0.17) | 0.20 | |
| L | 0.45 | 0.60 | 0.75 | |
| e | 0.80 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

06/02/2014

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| Atmel Package Drawing Contact: packagedrawings@atmel.com | **44A,** 44-lead, 10 x 10mm body size, 1.0mm body thickness, 0.8 mm lead pitch, thin profile plastic quad flat package (TQFP) | 44A | C |

## 8.2. 44M1




Note : JEDEC Standard MO-220, Fig . 1 (S AW Singulation) VKKD-3 .

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | – | 0.02 | 0.05 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | 6.90 | 7.00 | 7.10 | |
| D2 | 5.00 | 5.20 | 5.40 | |
| E | 6.90 | 7.00 | 7.10 | |
| E2 | 5.00 | 5.20 | 5.40 | |
| e | | 0.50 BSC | | |
| L | 0.59 | 0.64 | 0.69 | |
| K | 0.20 | 0.26 | 0.41 | |

9/26/08

| Package Drawing Contact: avr@atmel.com | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| | **44M1,**44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN) | ZWS | 44M1 | H |

# 9. Instruction Set Summary

| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| ADD | Rd, Rr | Add two Registers without Carry | Rd ← Rd + Rr | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add two Registers with Carry | Rd ← Rd + Rr + C | Z,C,N,V,H | 1 |
| SUB | Rd, Rr | Subtract two Registers | Rd ← Rd - Rr | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | Rd ← Rd - K | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract two Registers with Carry | Rd ← Rd - Rr - C | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract Constant from Reg with Carry. | Rd ← Rd - K - C | Z,C,N,V,H | 1 |
| AND | Rd, Rr | Logical AND Registers | Rd ← Rd · Rr | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | Rd ← Rd · K | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | Rd ← Rd v Rr | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | Rd ← Rd v K | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | Rd ← Rd ⊕ Rr | Z,N,V | 1 |
| COM | Rd | One’s Complement | Rd ← 0xFF - Rd | Z,C,N,V | 1 |
| NEG | Rd | Two’s Complement | Rd ← 0x00 - Rd | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd · (0xFF - K) | Z,N,V | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V | 1 |
| DEC | Rd | Decrement | Rd ← Rd - 1 | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd · Rd | Z,N,V | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V | 1 |
| SER | Rd | Set Register | Rd ← 0xFF | None | 1 |

| BRANCH INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | | None | 2 |
| RCALL | k | Relative Subroutine Call | PC ← PC + k + 1 | None | 3 |
| ICALL | | Indirect Call to (Z) | | None | 3 |
| RET | | Subroutine Return | PC ← STACK | None | 4 |
| RETI | | Interrupt Return | PC ← STACK | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | Rd - Rr | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | Rd - Rr - C | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | Rd - K | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |

| BRANCH INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| SBIC | A, b | Skip if Bit in I/O Register Cleared | if (I/O(A,b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIS | A, b | Skip if Bit in I/O Register is Set | if (I/O(A,b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC←PC+k + 1 | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC←PC+k + 1 | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if ( I = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if ( I = 0) then PC ← PC + k + 1 | None | 1/2 |

| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0)←C,Rd(n+1)← Rd(n),C¬Rd(7) | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0...6 | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | Rd(3...0)←Rd(7...4),Rd(7...4)¬Rd(3...0) | None | 1 |
| BSET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| SEC | | Set Carry | C ← 1 | C | 1 |
| CLC | | Clear Carry | C ← 0 | C | 1 |

| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| SEN | | Set Negative Flag | N ← 1 | N | 1 |
| CLN | | Clear Negative Flag | N ← 0 | N | 1 |
| SEZ | | Set Zero Flag | Z ← 1 | Z | 1 |
| CLZ | | Clear Zero Flag | Z ← 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I ← 1 | I | 1 |
| CLI | | Global Interrupt Disable | I ← 0 | I | 1 |
| SES | | Set Signed Test Flag | S ← 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S ← 0 | S | 1 |
| SEV | | Set Two's Complement Overflow. | V ← 1 | V | 1 |
| CLV | | Clear Two's Complement Overflow | V ← 0 | V | 1 |
| SET | | Set T in SREG | T ← 1 | T | 1 |
| CLT | | Clear T in SREG | T ← 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |

| DATA TRANSFER INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| MOV | Rd, Rr | Move Between Registers | Rd ← Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd ← K | None | 1 |
| LD | Rd, X | Load Indirect | Rd ← (X) | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Increment | Rd ← (X), X ← X + 1 | None | 2 |
| LD | Rd, - X | Load Indirect and Pre-Decrement | X ← X - 1, Rd ← (X) | None | 2 |
| LD | Rd, Y | Load Indirect | Rd ← (Y) | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Increment | Rd ← (Y), Y ← Y + 1 | None | 2 |
| LD | Rd, - Y | Load Indirect and Pre-Decrement | Y ← Y - 1, Rd ← (Y) | None | 2 |
| LD | Rd, Z | Load Indirect | Rd ← (Z) | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Increment | Rd ← (Z), Z ← Z+1 | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Decrement | Z ← Z - 1, Rd ← (Z) | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | Rd ← (k) | None | 2 |
| ST | X, Rr | Store Indirect | (X) ← Rr | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Increment | (X) ← Rr, X ← X + 1 | None | 2 |
| ST | - X, Rr | Store Indirect and Pre-Decrement | X ← X - 1, (X) ← Rr | None | 2 |
| ST | Y, Rr | Store Indirect | (Y) ← Rr | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Increment | (Y) ← Rr, Y ← Y + 1 | None | 2 |
| ST | - Y, Rr | Store Indirect and Pre-Decrement | Y ← Y - 1, (Y) ← Rr | None | 2 |
| ST | Z, Rr | Store Indirect | (Z) ← Rr | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Increment | (Z) ← Rr, Z ← Z + 1 | None | 2 |

| DATA TRANSFER INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| ST | -Z, Rr | Store Indirect and Pre-Decrement | Z ← Z - 1, (Z) ← Rr | None | 2 |
| STS | k, Rr | Store Direct to SRAM | (k) ← Rr | None | 2 |
| IN | Rd, A | In from I/O Location | Rd ← I/O (A) | None | 1 |
| OUT | A, Rr | Out to I/O Location | I/O (A) ← Rr | None | 1 |
| PUSH | Rr | Push Register on Stack | STACK ← Rr | None | 2 |
| POP | Rd | Pop Register from Stack | Rd ← STACK | None | 2 |

| MCU CONTROL INSTRUCTIONS | | | | | |
|---|---|---|---|---|---|
| **Mnemonics** | **Operands** | **Description** | **Operation** | **Flags** | **#Clocks** |
| NOP | | No Operation | No Operation | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

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