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**3-wire Serial EEPROM**  
**16K (2,048 x 8 or 1,024 x 16)**

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**DATASHEET**

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**Features**

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- Low-voltage Operation
  - $V_{CC} = 1.8V$  to 5.5V
  - $V_{CC} = 2.7V$  to 5.5V
- User-selectable Internal Organization
  - 16K: 2,048 x 8 or 1,024 x 16
- 3-wire Serial Interface
- Sequential Read Operation
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- 2MHz Clock Rate (5V)
- Self-timed Write Cycle (10ms Max)
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, and 8-lead PDIP Packages
- Die Sales: Wafer Form, Waffle Pack, and Bumped Wafers

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**Description**

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The Atmel® AT93C86A provides 16,384 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 1,024 words of 16 bits each (when the ORG pin is connected to  $V_{CC}$ ) and 2,048 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C86A is available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, and 8-lead PDIP packages.

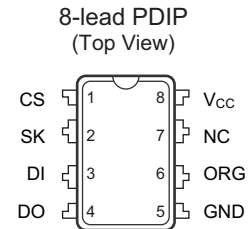
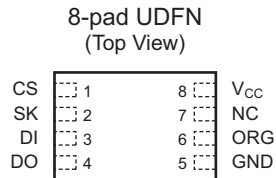
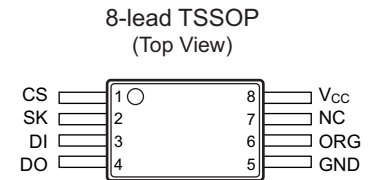
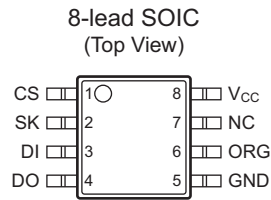
The AT93C86A is enabled through the Chip Select pin (CS) and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded, and the data is clocked out serially on the DO pin. The write cycle is completely self-timed, and no separate erase cycle is required before Write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C86A operates from 1.8V to 5.5V or from 2.7V to 5.5V.

# 1. Pin Configurations and Pinouts

**Table 1-1. Pin Configurations**

| Pin Name        | Function              |
|-----------------|-----------------------|
| CS              | Chip Select           |
| SK              | Serial Data Clock     |
| DI              | Serial Data Input     |
| DO              | Serial Data Output    |
| GND             | Ground                |
| V <sub>CC</sub> | Power Supply          |
| ORG             | Internal Organization |
| NC              | No Connect            |



Note: Drawings are not to scale.

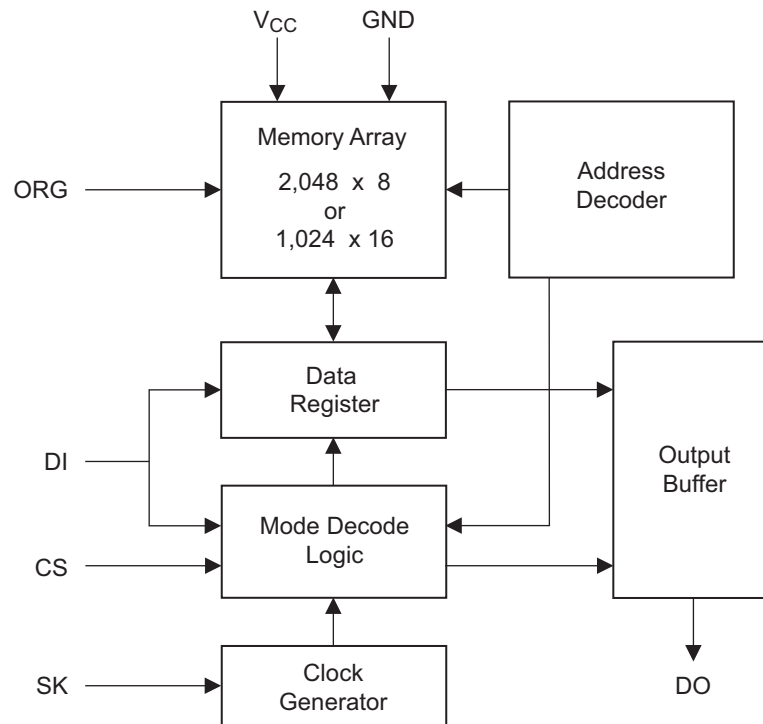
# 2. Absolute Maximum Ratings\*

|  |                  |
|--|------------------|
| Operating Temperature . . . . .                        | -55°C to +125°C  |
| Storage Temperature . . . . .                          | -65°C to +150°C  |
| Voltage on any pin<br>with respect to ground . . . . . | -1.00V to +7.00V |
| Maximum Operating Voltage . . . . .                    | 6.25V            |
| DC Output Current . . . . .                            | 5.0mA            |

\*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 3. Block Diagram

Figure 3-1. Block Diagram



Note: When the ORG pin is connected to  $V_{CC}$ , the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, and the application does not load the input beyond the capability of the internal  $1M\Omega$  pull-up resistor, then the x16 organization is selected.

## 4. Memory Organization

### 4.1 Pin Capacitance

**Table 4-1. Pin Capacitance<sup>(1)</sup>**

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ ,  $V_{CC} = 5.0\text{V}$  (unless otherwise noted).

| Symbol    | Test Conditions                | Max | Units | Conditions            |
|-----------|--------------------------------|-----|-------|-----------------------|
| $C_{OUT}$ | Output Capacitance (DO)        | 5   | pF    | $V_{OUT} = 0\text{V}$ |
| $C_{IN}$  | Input Capacitance (CS, SK, DI) | 5   | pF    | $V_{IN} = 0\text{V}$  |

Note: 1. This parameter is characterized, and is not 100% tested.

### 4.2 DC Characteristics

**Table 4-2. DC Characteristics**

Applicable over recommended operating range from  $T_{AI} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.8\text{V}$  to  $5.5\text{V}$  (unless otherwise noted).

| Symbol          | Parameter           | Test Condition                             | Min                        | Typ                 | Max                 | Unit          |
|-----------------|---------------------|--|----------------------------|---------------------|---------------------|---------------|
| $V_{CC1}$       | Supply Voltage      |  | 1.8                        |                     | 5.5                 | V             |
| $V_{CC2}$       | Supply Voltage      |  | 2.7                        |                     | 5.5                 | V             |
| $V_{CC3}$       | Supply Voltage      |  | 4.5                        |                     | 5.5                 | V             |
| $I_{CC}$        | Supply Current      | $V_{CC} = 5.0\text{V}$                     | Read at 1.0MHz             | 0.5                 | 2.0                 | mA            |
|                 |                     |  | Write at 1.0MHz            | 0.5                 | 2.0                 | mA            |
| $I_{SB1}$       | Standby Current     | $V_{CC} = 1.8\text{V}$                     | CS = 0V                    | 0.4                 | 1.0                 | $\mu\text{A}$ |
| $I_{SB2}$       | Standby Current     | $V_{CC} = 2.7\text{V}$                     | CS = 0V                    | 6.0                 | 10.0                | $\mu\text{A}$ |
| $I_{SB3}$       | Standby Current     | $V_{CC} = 5.0\text{V}$                     | CS = 0V                    | 10.0                | 15.0                | $\mu\text{A}$ |
| $I_{IL}$        | Input Leakage       | $V_{IN} = 0\text{V}$ to $V_{CC}$           |                            | 0.1                 | 3.0                 | $\mu\text{A}$ |
| $I_{OL}$        | Output Leakage      | $V_{IN} = 0\text{V}$ to $V_{CC}$           |                            | 0.1                 | 3.0                 | $\mu\text{A}$ |
| $V_{IL1}^{(1)}$ | Input Low Voltage   | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ |                            | -0.6                | 0.8                 | V             |
| $V_{IH1}^{(1)}$ | Input High Voltage  | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ |                            | 2.0                 | $V_{CC} + 1$        | V             |
| $V_{IL2}^{(1)}$ | Input Low Voltage   | $1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$ |                            | -0.6                | $V_{CC} \times 0.3$ | V             |
| $V_{IH2}^{(1)}$ | Input High Voltage  | $1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$ |                            | $V_{CC} \times 0.7$ | $V_{CC} + 1$        | V             |
| $V_{OL1}$       | Output Low Voltage  | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | $I_{OL} = 2.1\text{mA}$    |                     | 0.4                 | V             |
| $V_{OH1}$       | Output High Voltage | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | $I_{OH} = -0.4\text{mA}$   |                     | 2.4                 | V             |
| $V_{OL2}$       | Output Low Voltage  | $1.8\text{V} \leq V_{CC} \leq 2.5\text{V}$ | $I_{OL} = 0.15\text{mA}$   |                     | 0.2                 | V             |
| $V_{OH2}$       | Output High Voltage | $1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$ | $I_{OH} = -100\mu\text{A}$ |                     | $V_{CC} - 0.2$      | V             |

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only, and are not tested.

## 4.3 AC Characteristics

**Table 4-3. AC Characteristics**

Applicable over recommended operating range from  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $CL = 1$  TTL gate and  $100\text{pF}$  (unless otherwise noted).

| Symbol                   | Parameter                  | Test Condition                             | Min  | Typ       | Max  | Units        |
|--------------------------|----------------------------|--|------|-----------|------|--------------|
| $f_{SK}$                 | SK Clock Frequency         | $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 0    |           | 2    | MHz          |
|                          |                            | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 0    |           | 1    | MHz          |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 0    |           | 250  | kHz          |
| $t_{SKH}$                | SK High Time               | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 250  |           |      | ns           |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 1000 |           |      | ns           |
| $t_{SKL}$                | SK Low Time                | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 250  |           |      | ns           |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 1000 |           |      | ns           |
| $t_{CS}$                 | Minimum CS Low Time        | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 250  |           |      | ns           |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 1000 |           |      | ns           |
| $t_{CSS}$                | CS Setup Time              | Relative to SK                             |      |           |      |              |
|                          |                            | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 50   |           |      | ns           |
| $t_{DIS}$                | DI Setup Time              | Relative to SK                             |      |           |      |              |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 200  |           |      | ns           |
| $t_{DIH}$                | DI Hold Time               | Relative to SK                             |      |           |      |              |
|                          |                            | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 100  |           |      | ns           |
| $t_{CSH}$                | CS Hold Time               | Relative to SK                             |      |           |      |              |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 400  |           |      | ns           |
| $t_{PD1}$                | Output Delay to 1          | AC Test                                    |      |           |      |              |
|                          |                            | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ |      |           | 250  | ns           |
| $t_{PDO}$                | Output Delay to 0          | AC Test                                    |      |           |      |              |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ |      |           | 1000 | ns           |
| $t_{SV}$                 | CS to Status Valid         | AC Test                                    |      |           |      |              |
|                          |                            | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ |      |           | 250  | ns           |
| $t_{DF}$                 | CS to DO in High-impedance | AC Test                                    |      |           |      |              |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ |      |           | 1000 | ns           |
| $t_{WP}$                 | Write Cycle Time           | AC Test                                    |      |           |      |              |
|                          |                            | $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ |      |           | 150  | ns           |
| $t_{DF}$                 | CS to DO in High-impedance | CS = $V_{IL}$                              |      |           |      |              |
|                          |                            | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ |      |           | 400  | ns           |
| $t_{WP}$                 | Write Cycle Time           | $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$ | 0.1  | 3         | 10   | ms           |
| Endurance <sup>(1)</sup> | 5.0V, 25°C                 |  |      | 1,000,000 |      | Write Cycles |

Note: 1. This parameter is characterized, and is not 100% tested.

## 5. Functional Description

The AT93C86A is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the Host processor. A valid instruction starts with a rising edge of CS and consists of a Start bit (Logic 1), followed by the appropriate opcode, and the desired memory address location.

**Table 5-1. AT93C86A Instruction Set**

| Instruction | SB | Opcode | Address                          |                                 | Data                            |                                  | Comments  |
|-------------|----|--------|----------------------------------|---------------------------------|---------------------------------|----------------------------------|---|
|             |    |        | x8 <sup>(1)</sup>                | x16 <sup>(1)</sup>              | x8                              | x16                              |   |
| READ        | 1  | 10     | A <sub>10</sub> – A <sub>0</sub> | A <sub>9</sub> – A <sub>0</sub> |                                 |                                  | Reads data stored in memory at specified address.   |
| EWEN        | 1  | 00     | 11XXXXXXXX                       | 11XXXXXX                        |                                 |                                  | Write Enable must precede all programming modes.  |
| ERASE       | 1  | 11     | A <sub>10</sub> – A <sub>0</sub> | A <sub>9</sub> – A <sub>0</sub> |                                 |                                  | Erases memory location A <sub>N</sub> – A <sub>0</sub> .  |
| WRITE       | 1  | 01     | A <sub>10</sub> – A <sub>0</sub> | A <sub>9</sub> – A <sub>0</sub> | D <sub>7</sub> – D <sub>0</sub> | D <sub>15</sub> – D <sub>0</sub> | Writes memory location A <sub>N</sub> – A <sub>0</sub> .  |
| ERAL        | 1  | 00     | 10XXXXXXXX                       | 10XXXXXX                        |                                 |                                  | Erases all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V.                              |
| WRAL        | 1  | 00     | 01XXXXXXXX                       | 01XXXXXX                        | D <sub>7</sub> – D <sub>0</sub> | D <sub>15</sub> – D <sub>0</sub> | Writes all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V and Disable Register cleared. |
| EWDS        | 1  | 00     | 00XXXXXXXX                       | 00XXXXXX                        |                                 |                                  | Disables all programming instructions.  |

Note: 1. The 'X' in the address field represent don't care values, and must be clocked.

**READ:** The READ instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the Serial Output pin, DO. Output data changes are synchronized with the rising edges of the Serial Clock pin, SK. It should be noted that a dummy bit (Logic 0) precedes the 8-bit or 16-bit data output string. The AT93C86A supports sequential Read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (Logic 0) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

**Erase/Write Enable (EWEN):** To ensure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out.

Note: Once in the EWEN state, programming remains enabled until an EWDS instruction is executed, or V<sub>CC</sub> power is removed from the part.

**ERASE:** The ERASE instruction programs all bits in the specified memory location to the Logic 1 state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of  $t_{CS}$ . A Logic 1 at the DO pin indicates that the selected memory location has been erased, and the part is ready for another instruction.

**WRITE:** The WRITE instruction contains the 8-bits or 16-bits of data to be written into the specified memory location. The self-timed programming cycle,  $t_{WP}$ , starts after the last bit of data is received at Serial Data Input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of  $t_{CS}$ . A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction, and the part is ready for further instructions. A Ready/Busy status cannot be obtained if CS is brought high after the end of the self-timed programming cycle,  $t_{WP}$ .

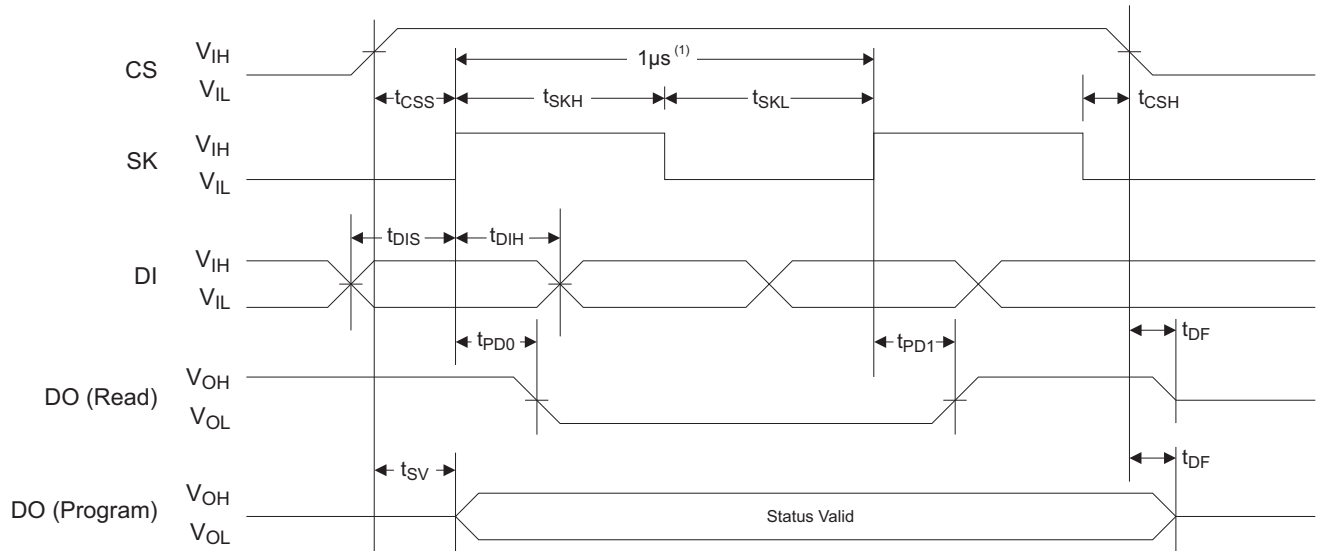
**Erase All (ERAL):** The Erase All (ERAL) instruction programs every bit in the Memory Array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of  $t_{CS}$ . The ERAL instruction is valid only at  $V_{CC} = 5.0V \pm 10\%$ .

**Write All (WRAL):** The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of  $t_{CS}$ . The WRAL instruction is valid only at  $V_{CC} = 5.0V \pm 10\%$ .

**Erase/Write Disable (EWDS):** To protect against accidental data disturbance, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

## 6. Timing Diagrams

Figure 6-1. Synchronous Data Timing

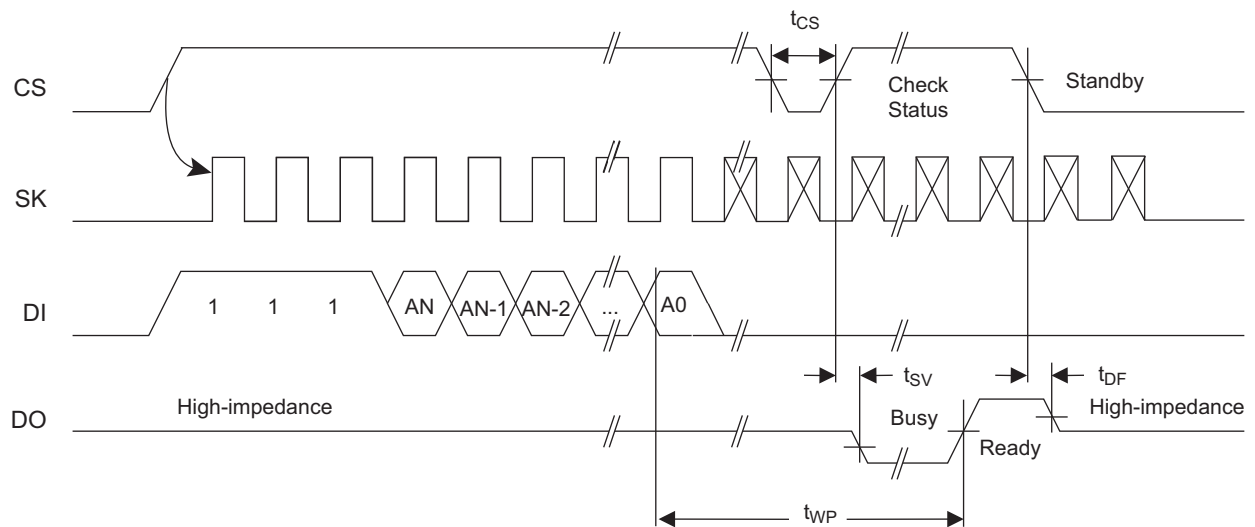


Note: 1. This is the minimum SK period.

Table 6-1. Organization Key for Timing Diagrams

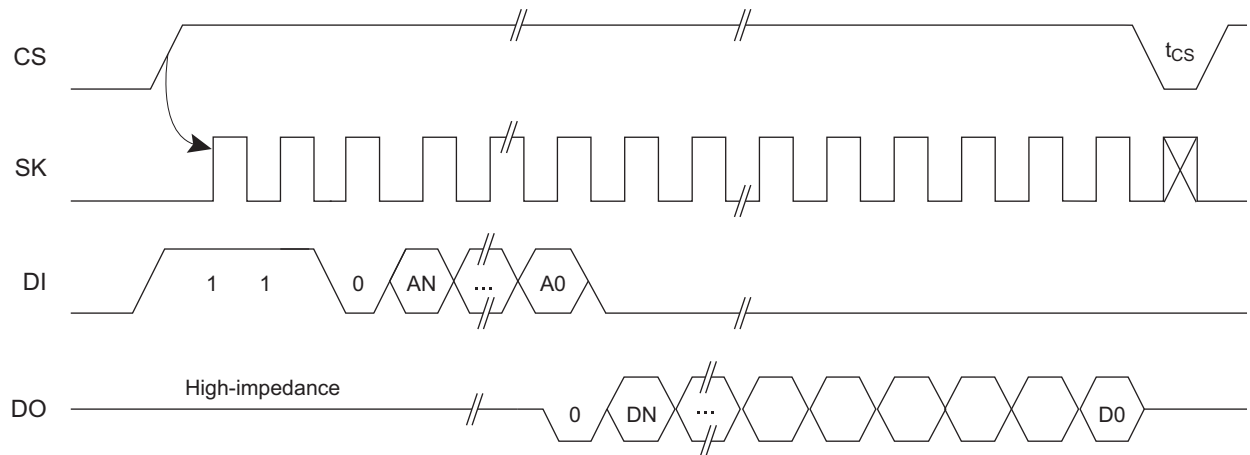
| I/O   | AT93C86A (16K) |          |
|-------|----------------|----------|
|       | x8             | x16      |
| $A_N$ | $A_{10}$       | $A_9$    |
| $D_N$ | $D_7$          | $D_{15}$ |

Figure 6-2. ERASE Timing

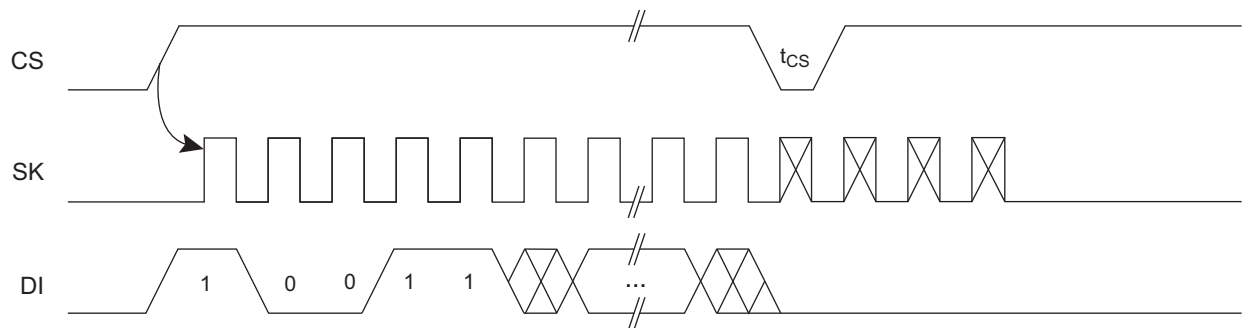




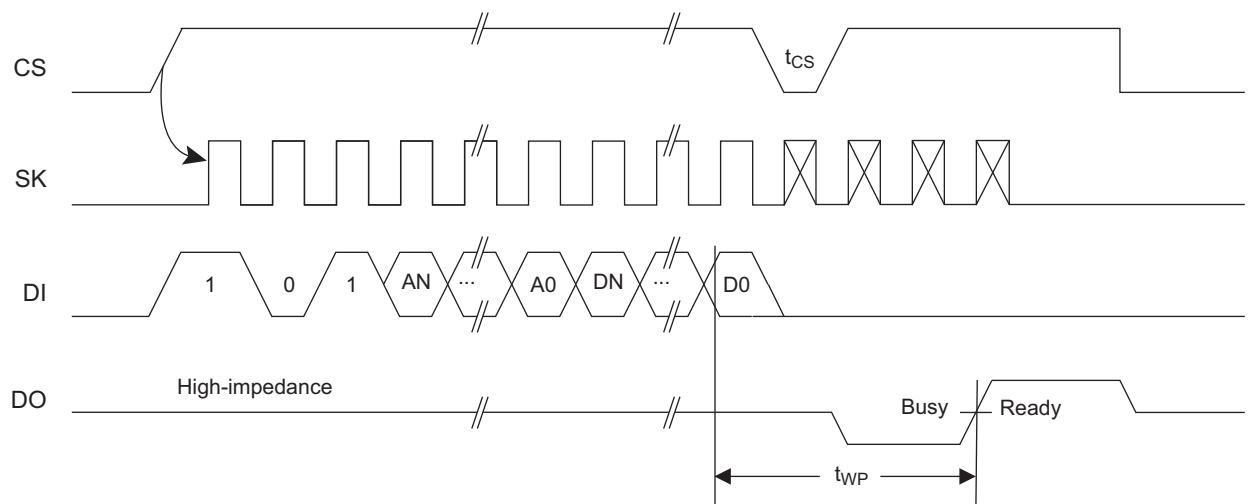
**Figure 6-3. READ Timing**



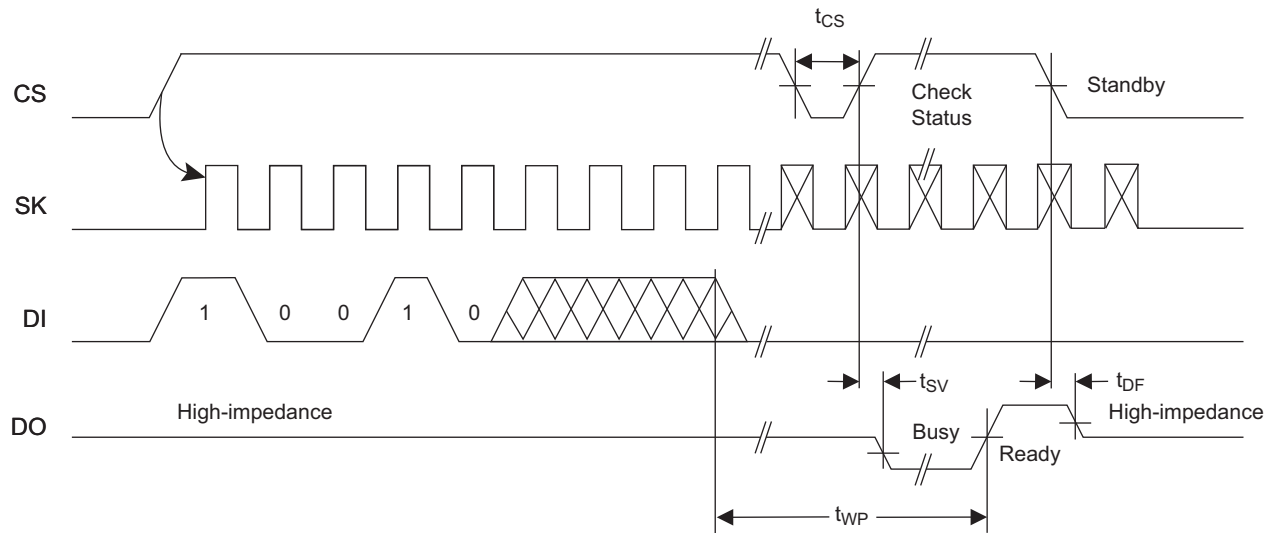
**Figure 6-4. EWEN Timing**



**Figure 6-5. WRITE Timing**

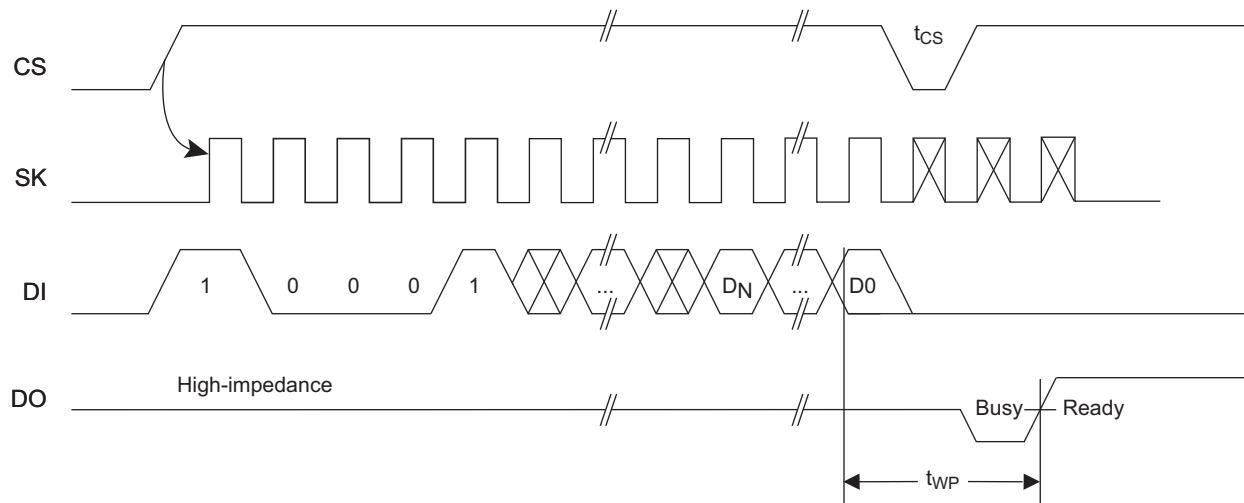


**Figure 6-6. ERAL Timing<sup>(1)</sup>**



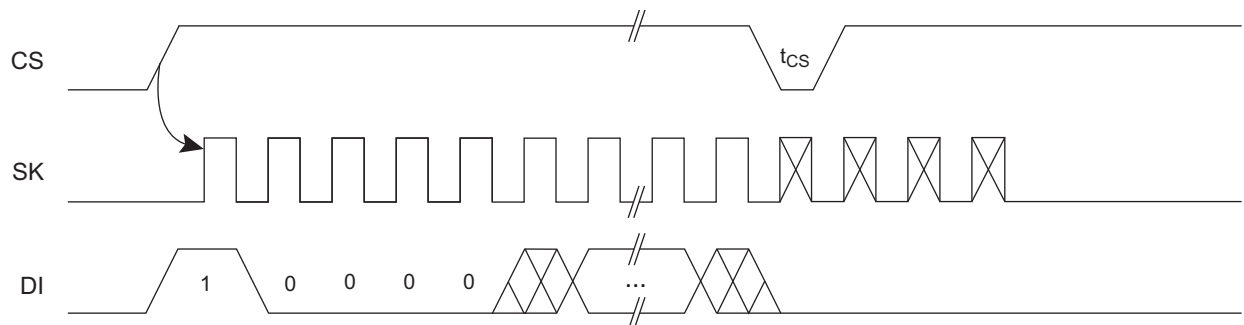
Note: 1.  $V_{CC} = 4.5V$  to  $5.5V$ .

**Figure 6-7. WRAL Timing<sup>(1)</sup>**

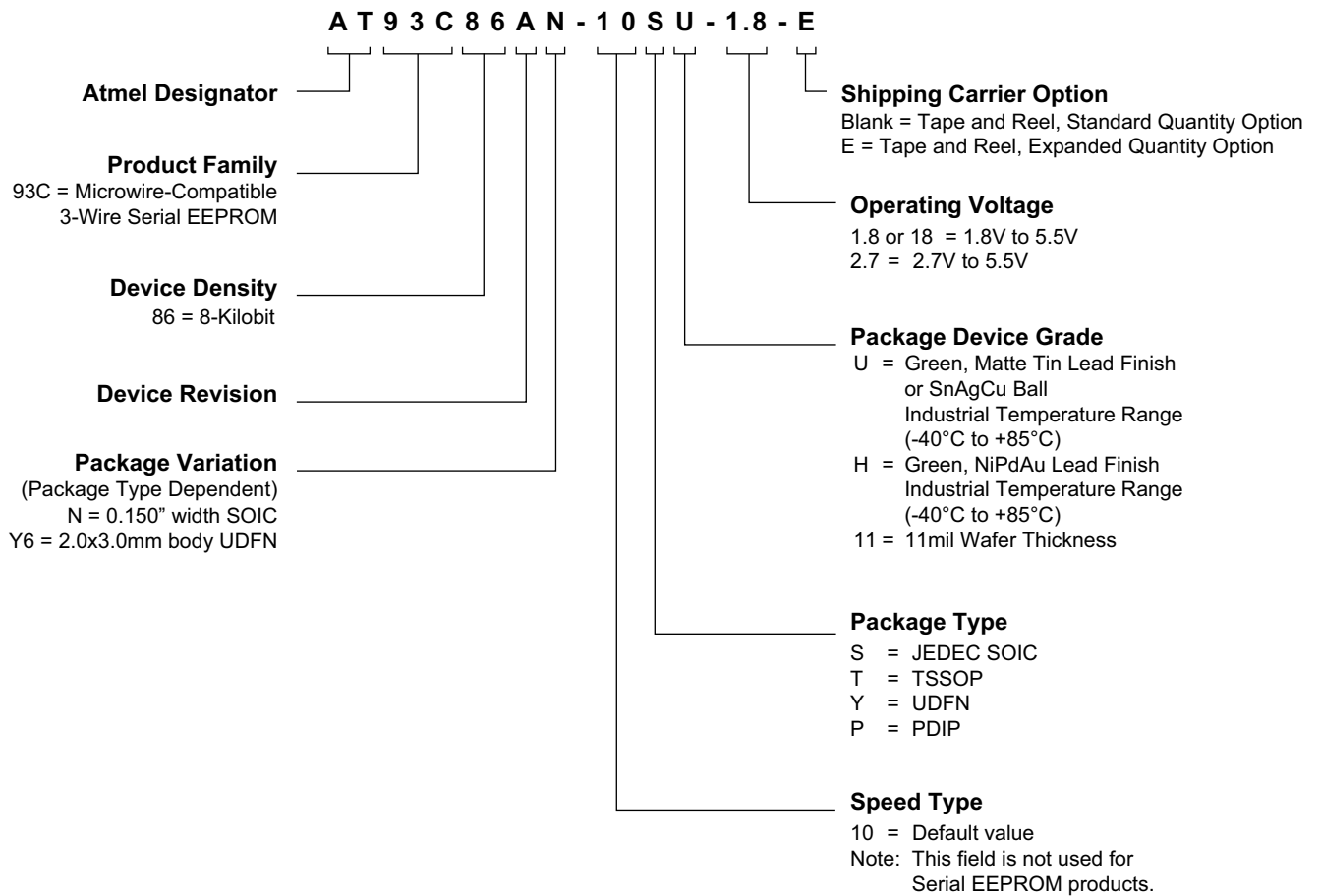


Note: 1. Valid only at  $V_{CC} = 4.5V$  to  $5.5V$ .

**Figure 6-8. EWDS Timing**



## 7. Ordering Code Detail



## 8. Part Markings

### AT93C86A: Package Marking Information

|   |  |
|---|--|
| 8-lead SOIC   | 8-lead TSSOP   |
| <p>Note: Lot Number and location of assembly on the bottom side of the package.</p> | <p>Note: Lot Number, location of assembly and YWW date code on the bottom side of the package.</p> |
| 8-pad UDFN  | 8-lead PDIP  |
| <p>2.0 x 3.0 mm Body</p>  | <p>Note: Lot Number and location of assembly on the bottom side of the package.</p>                |

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

| Catalog Number Truncation  |             |                                  |  |
|--|-------------|----------------------------------|--|
| AT93C86A   |             | Truncation Code ###: 86A         |  |
| Date Codes   |             |                                  | Voltagess  |
| Y = Year   | M = Month   | WW = Work Week of Assembly       | % = Minimum Voltage                                    |
| 4: 2014    8: 2018   | A: January  | 02: Week 2                       | 3 or 27: 2.7V min                                      |
| 5: 2015    9: 2019   | B: February | 04: Week 4                       | 1 or 18: 1.8V min                                      |
| 6: 2016    0: 2020   | ...         | ...                              |  |
| 7: 2017    1: 2021   | L: December | 52: Week 52                      |  |
| Country of Assembly  |             | Lot Number                       | Grade/Lead Finish Material                             |
| @ = Country of Assembly  |             | AAA...A = Atmel Wafer Lot Number | H: Industrial/NiPdAu<br>U: Industrial/Matte Tin/SnAgCu |
| Trace Code   |             |                                  | Atmel Truncation                                       |
| XX = Trace Code (Atmel Lot Numbers Correspond to Code)<br>Example: AA, AB.... YZ, ZZ |             |                                  | AT: Atmel<br>ATM: Atmel<br>ATML: Atmel                 |

6/11/14

|  |   |                                |                  |
|--|---|--------------------------------|------------------|
| <p>Package Mark Contact:<br/>DL-CSO-Assy_eng@atmel.com</p> | <b>TITLE</b><br><b>93C86ASM, AT93C86A Package Marking Information</b> | <b>DRAWING NO.</b><br>93C86ASM | <b>REV.</b><br>A |
|--|---|--------------------------------|------------------|

## 9. Ordering Information

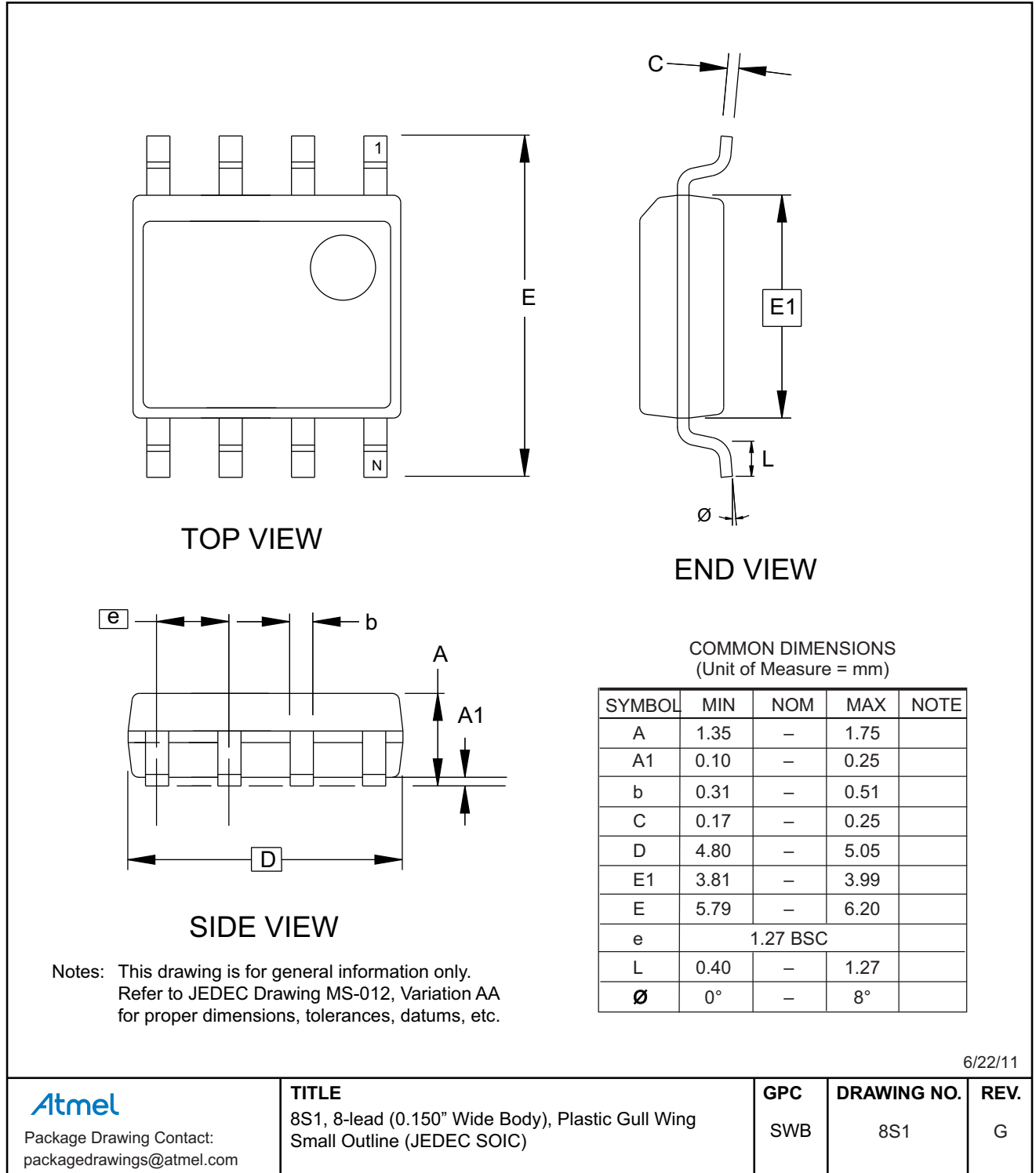
| Atmel Ordering Code <sup>(1)</sup> | Lead Finish                            | Package    | Voltage                     | Delivery Information |                 | Operation Range                              |
|------------------------------------|--|------------|-----------------------------|----------------------|-----------------|--|
|                                    |  |            |                             | Form                 | Quantity        |  |
| AT93C86A-10SU-1.8                  | NiPdAu<br>Lead-free<br>Halogen-free    | 8S1        | 1.8V to 5.5V                | Tape and Reel        | 4,000 per Reel  | Industrial<br>Temperature<br>(-40°C to 85°C) |
| AT93C86A-10SU-2.7                  |  |            | 2.7V to 5.5V <sup>(1)</sup> | Tape and Reel        | 4,000 per Reel  |  |
| AT93C86A-10TU-1.8                  |  | 8X         | 1.8V to 5.5V                | Tape and Reel        | 5,000 per Reel  |  |
| AT93C86A-10TU-2.7                  |  |            | 2.7V to 5.5V <sup>(1)</sup> | Tape and Reel        | 5,000 per Reel  |  |
| AT93C86A-10PU-1.8                  | Matte Tin<br>Lead-free<br>Halogen-free | 8P3        | 1.8V to 5.5V                | Tape and Reel        | 4,000 per Reel  |  |
| AT93C86A-10PU-2.7                  |  |            | 2.7V to 5.5V <sup>(1)</sup> | Tape and Reel        | 4,000 per Reel  |  |
| AT93C86AY6-10YH-1.8                | NiPdAu<br>Lead-free<br>Halogen-free    | 8MA2       | 1.8V to 5.5V                | Tape and Reel        | 5,000 per Reel  |  |
| AT93C86AY6-10YH-18-E               |  |            |                             | Tape and Reel        | 15,000 per Reel |  |
| AT93C86A-W1.8-11 <sup>(2)</sup>    | N/A                                    | Wafer Sale | 1.8V to 5.5V                | Note 2               |                 |  |

- Notes: 1. For 2.7V devices used in a 4.5V to 5.5V range, please refer to performance values in [Section 4.2, “DC Characteristics”](#) and [4.3, “AC Characteristics”](#) on page 5.
2. For Waffle pack and Wafer form; order as SL788 for inkless Wafer form. Bumped die available upon request. Please contact Atmel sales.

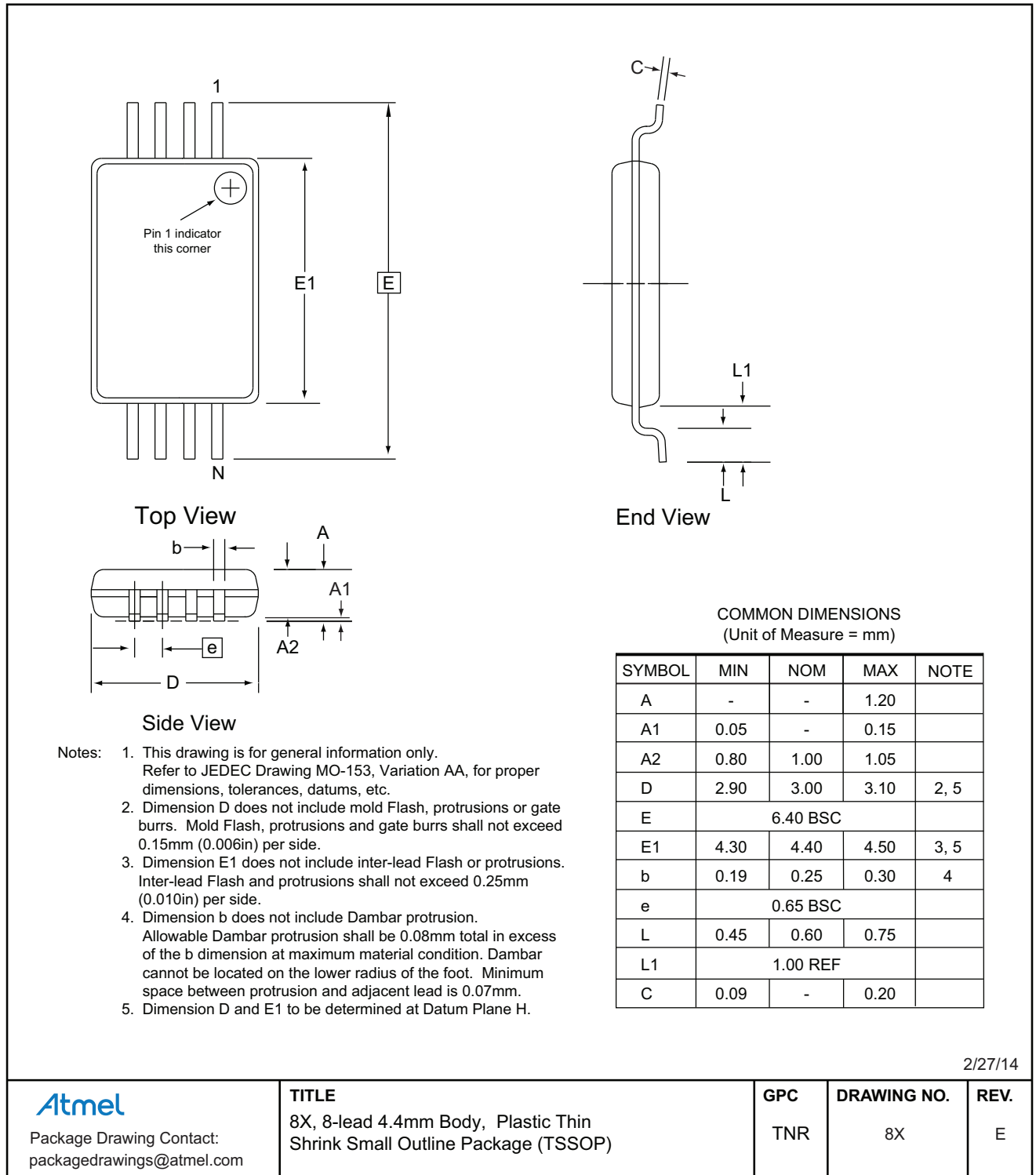
| Package Type |   |
|--------------|---|
| 8S1          | 8-lead, 0.150” wide, Plastic Gull Wing, Small Outline (JEDEC SOIC)        |
| 8X           | 8-lead, 0.170” wide, Thin Shrink Small Outline (TSSOP)                    |
| 8P3          | 8-lead, 0.300” wide body, Plastic Dual In-line Package (PDIP)             |
| 8MA2         | 8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Ultra Thin Dual No Lead (UDFN) |

## 10. Packaging Information

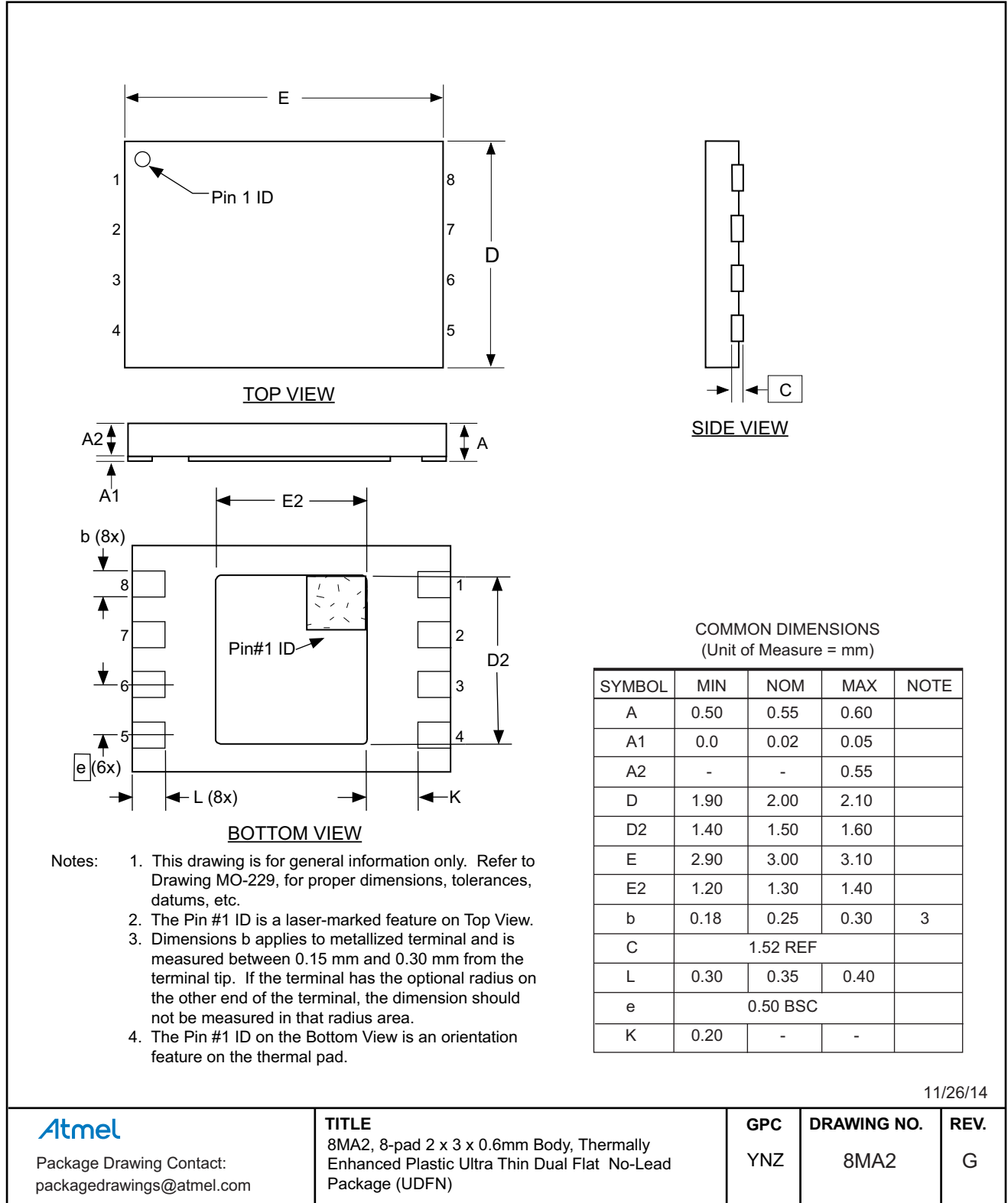
### 10.1 8S1 — 8-lead JEDEC SOIC



## 10.2 8X — 8-lead TSSOP



### 10.3 8MA2 — 8-pad UDFN



11/26/14

**Atmel**

Package Drawing Contact:  
packagedrawings@atmel.com

**TITLE**

8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)

**GPC**

YNZ

**DRAWING NO.**

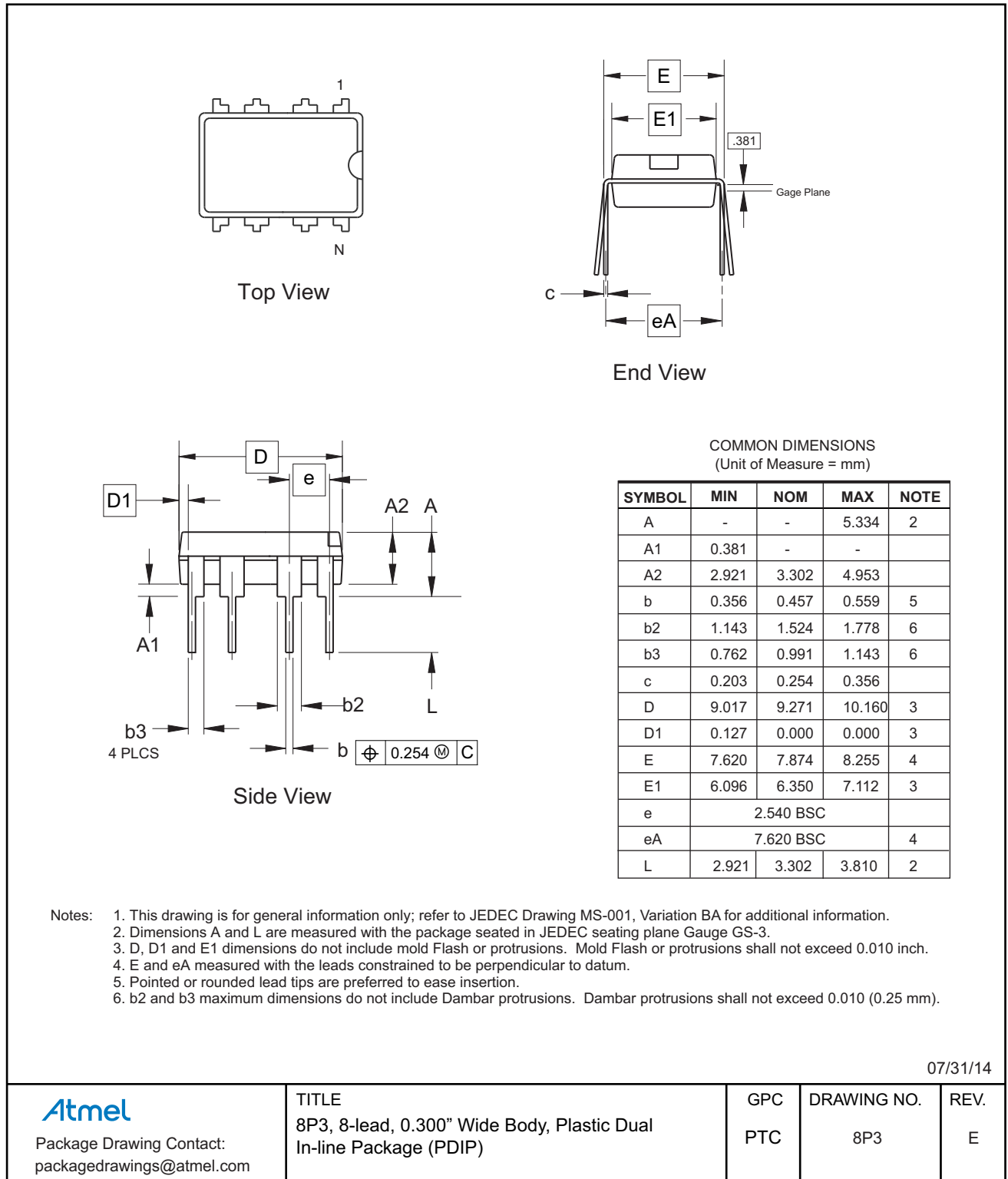
8MA2

**REV.**

G



## 10.4 8P3 — 8-lead PDIP



07/31/14

**Atmel**

Package Drawing Contact:  
packagedrawings@atmel.com

TITLE  
8P3, 8-lead, 0.300" Wide Body, Plastic Dual  
In-line Package (PDIP)

GPC  
PTC

DRAWING NO.  
8P3

REV.  
E

## 11. Revision History

| Revision No. | Date    | Comments  |
|--------------|---------|---|
| 3408J        | 01/2015 | Add the UDFN extended quantity option and update the ordering information section. Update the 8MA2 and 8P3 package drawings.  |
| 3408I        | 08/2014 | Update pinouts, 8MA2 package drawing, grammatical changes, document template, logos, and disclaimer page. No changes to functional specification.   |
| 3408H        | 01/2007 | Add "Bottom View" to pg 1 Ultra Thin MiniMap package drawing pg 4 revise Note 1 added "ensured by characterization".  |
| 3408G        | 07/2006 | Revision history implemented.<br>Delete 'Preliminary' status from datasheet; Add 'Ultra Thin' description to MLP 2x3 package; Delete '1.8V not available' on Figure 1 Note; Add 1.8V range on Table 4 under Write Cycle Time. |



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