

## ADG811/ADG812/ADG813

### FEATURES

- 0.5  $\Omega$  typical on resistance
- 0.8  $\Omega$  maximum on resistance at 125°C
- 1.65 V to 3.6 V operation
- Automotive temperature range: -40°C to +125°C
- High current carrying capability: 300 mA continuous
- Rail-to-rail switching operation
- Fast switching times: <25 ns
- Typical power consumption <0.1  $\mu$ W

### APPLICATIONS

- Cellular phones
- MP3 players
- Power routing
- Battery-powered systems
- PCMCIA cards
- Modems
- Audio and video signal routing
- Communications systems

### GENERAL DESCRIPTION

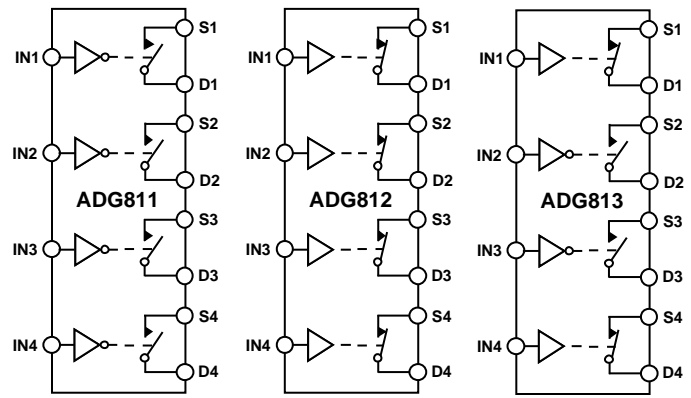
The ADG811/ADG812/ADG813 are low voltage CMOS devices containing four independently selectable switches. These switches offer ultralow on resistance of less than 0.8  $\Omega$  over the full temperature range. The digital inputs can handle 1.8 V logic with a 2.7 V to 3.6 V supply.

These devices contain four independent single-pole/single-throw (SPST) switches. The ADG811 and ADG812 differ only in that the digital control logic is inverted. The ADG811 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG812. The ADG813 contains two switches whose digital control logic is similar to the ADG811, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG813 exhibits break-before-make switching action.

The ADG811/ADG812/ADG813 are fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation. The ADG811 is available in a 16-lead TSSOP package and a 16-lead LFCSP package, and the ADG812/ADG813 are available in a 16-lead TSSOP package.

### FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC 1 INPUT

Figure 1.

04396A-001

### PRODUCT HIGHLIGHTS

1. <0.8  $\Omega$  over full temperature range of -40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Operational with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low THD + N (0.02% typical).
6. Small 3 mm  $\times$  3 mm LFCSP package and 16-lead TSSOP package.

#### Rev. B

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## REVISION HISTORY

### 11/09—Rev. A to Rev. B

Added 16-Lead LFCSP .....	Universal
Changes to Table 4.....	6
Changes to Pin Configurations and Function Description Section.....	7
Moved Terminology Section.....	13
Updated Outline Dimensions .....	14
Changes to Ordering Guide .....	15

### 5/04—Rev. 0 to Rev. A

Updated Format.....	Universal
Updated Package Choices .....	Universal

### 11/03—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted. Temperature range for the Y version is  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ .

**Table 1.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	0.5			$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_S = 10\text{ mA}$ ; see Figure 19
On Resistance Match Between Channels, $\Delta R_{ON}$	0.65 0.04	0.75	0.8	$\Omega$ max $\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0.5\text{ V}$ , $I_S = 10\text{ mA}$
On Resistance Flatness, $R_{FLAT(ON)}$	0.1	0.075 0.15	0.08 0.16	$\Omega$ max $\Omega$ typ $\Omega$ max	$V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_S = 10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.2$			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$ , $V_D = 3.3\text{ V}/0.6\text{ V}$ ; see Figure 20
Drain Off Leakage, $I_D$ (Off)	$\pm 1$ $\pm 0.2$	$\pm 8$	$\pm 80$	nA max nA typ	$V_S = 0.6\text{ V}/3.3\text{ V}$ , $V_D = 3.3\text{ V}/0.6\text{ V}$ ; see Figure 20
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 1$ $\pm 0.2$ $\pm 1$	$\pm 8$	$\pm 80$	nA max nA typ nA max	$V_S = V_D = 0.6\text{ V or }3.3\text{ V}$ ; see Figure 21
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	6		$\pm 0.1$	pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	21 25	26	28	ns typ ns max	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}/0\text{ V}$ ; see Figure 22
$t_{OFF}$	4 5	6	7	ns typ ns max	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$ ; see Figure 22
Break-Before-Make Time Delay, $t_{BBM}$ (ADG813 Only)	17			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
Charge Injection	30		5	ns min pC typ	$V_{S1} = V_{S2} = 1.5\text{ V}$ ; see Figure 23 $V_S = 1.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 24
Off Isolation	-67			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
Total Harmonic Distortion (THD + N)	0.02			%	$R_L = 32\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 2\text{ V p-p}$
Insertion Loss	-0.05			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$
-3 dB Bandwidth	90			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
$C_S$ (Off)	30			pF typ	
$C_D$ (Off)	35			pF typ	
$C_D$ , $C_S$ (On)	60			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.003	1.0	4	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V

<sup>1</sup> Guaranteed by design, but not subject to production test.

# ADG811/ADG812/ADG813

$V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ,  $GND = 0 \text{ V}$ , unless otherwise noted. Temperature range for the Y version is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

**Table 2.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	0.65			$\Omega$ typ	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 10 \text{ mA}$ ; see Figure 19
On Resistance Match Between Channels, $\Delta R_{ON}$	0.72 0.04	0.8	0.88	$\Omega$ max $\Omega$ typ	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0.55 \text{ V}$ , $I_S = 10 \text{ mA}$
On Resistance Flatness, $R_{FLAT(ON)}$	0.16	0.08 0.23	0.085 0.24	$\Omega$ max $\Omega$ typ $\Omega$ max	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 10 \text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.2$			nA typ	$V_{DD} = 2.7 \text{ V}$ $V_S = 0.6 \text{ V}/2.4 \text{ V}$ , $V_D = 2.4 \text{ V}/0.6 \text{ V}$ ; see Figure 20
Drain Off Leakage, $I_D$ (Off)	$\pm 1$ $\pm 0.2$	$\pm 6$	$\pm 35$	nA max nA typ	$V_S = 0.6 \text{ V}/2.4 \text{ V}$ , $V_D = 2.4 \text{ V}/0.6 \text{ V}$ ; see Figure 20
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 1$ $\pm 0.2$ $\pm 1$	$\pm 6$ $\pm 11$	$\pm 35$ $\pm 70$	nA max nA typ nA max	$V_S = V_D = 0.6 \text{ V}$ or $2.4 \text{ V}$ ; see Figure 21
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			1.7	V min	
Input Low Voltage, $V_{INL}$			0.7	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	6			$\mu\text{A}$ max pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	22 27	29	30	ns typ ns max	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}/0 \text{ V}$ ; see Figure 22
$t_{OFF}$	4 6	7	8	ns typ ns max	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}$ ; see Figure 22
Break-Before-Make Time Delay, $t_{BBM}$ (ADG813 Only)	18			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
Charge Injection	25		5	ns min pC typ	$V_{S1} = V_{S2} = 1.5 \text{ V}$ ; see Figure 23 $V_S = 1.25 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; see Figure 24
Off Isolation	-67			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; see Figure 25
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; see Figure 27
Total Harmonic Distortion (THD + N)	0.022			%	$R_L = 32 \Omega$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , $V_S = 1.5 \text{ V}$ p-p
Insertion Loss	-0.06			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$
-3 dB Bandwidth	90			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; see Figure 26
$C_S$ (Off)	32			pF typ	
$C_D$ (Off)	37			pF typ	
$C_D$ , $C_S$ (On)	60			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.003	1.0	4	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 2.7 \text{ V}$ Digital inputs = 0 V or 2.7 V

<sup>1</sup> Guaranteed by design, but not subject to production test.

$V_{DD} = 1.65\text{ V to }1.95\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted. Temperature range for the Y version is  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ .

**Table 3.**

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	1			$\Omega$ typ	$V_{DD} = 1.8\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_S = 10\text{ mA}$ ; see Figure 19
	1.4	2.2	2.2	$\Omega$ max	
On Resistance Match Between Channels, $\Delta R_{ON}$	2.5	4	4	$\Omega$ max	$V_{DD} = 1.65\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_S = 10\text{ mA}$
	0.1			$\Omega$ typ	$V_{DD} = 1.65\text{ V}$ , $V_S = 0.7\text{ V}$ , $I_S = 10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (Off)	$\pm 0.2$			nA typ	$V_{DD} = 1.95\text{ V}$ $V_S = 0.6\text{ V}/1.65\text{ V}$ , $V_D = 1.65\text{ V}/0.6\text{ V}$ ; see Figure 20
Drain Off Leakage $I_D$ (Off)	$\pm 1$	$\pm 5$	$\pm 30$	nA max	
	$\pm 0.2$			nA typ	$V_S = 0.6\text{ V}/1.65\text{ V}$ , $V_D = 1.65\text{ V}/0.6\text{ V}$ ; see Figure 20
Channel On Leakage $I_D$ , $I_S$ (On)	$\pm 1$	$\pm 5$	$\pm 30$	nA max	
	$\pm 0.2$			nA typ	$V_S = V_D = 0.6\text{ V or }1.65\text{ V}$ ; see Figure 21
	$\pm 1$	$\pm 9$	$\pm 60$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			$0.65V_{DD}$	V min	
Input Low Voltage, $V_{INL}$			$0.35V_{DD}$	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
CIN, Digital Input Capacitance	6			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	27			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	35	36	37	ns max	$V_S = 1.5\text{ V}/0\text{ V}$ ; see Figure 22
$t_{OFF}$	6			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	8	9	10	ns max	$V_S = 1.5\text{ V}$ ; see Figure 22
Break-Before-Make Time Delay, $t_{BBM}$ (ADG813 Only)	20			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1\text{ V}$ ; see Figure 23
Charge Injection	15			pC typ	$V_S = 1\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 24
Off Isolation	-67			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; Figure 25
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 27
Total Harmonic Distortion (THD + N)	0.14			%	$R_L = 32\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 1.2\text{ V p-p}$
Insertion Loss	-0.08			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$
-3 dB Bandwidth	90			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
$C_S$ (Off)	32			pF typ	
$C_D$ (Off)	38			pF typ	
$C_D$ , $C_S$ (On)	60			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.003			$\mu\text{A}$ typ	$V_{DD} = 1.95\text{ V}$ Digital inputs = 0 V or 1.95 V
		1.0	4	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design, but not subject to production test.

# ADG811/ADG812/ADG813

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

**Table 4.**

Parameter	Rating
V <sub>DD</sub> to GND	−0.3 V to +4.6 V
Analog Inputs <sup>1</sup>	−0.3 V to V <sub>DD</sub> + 0.3 V
Digital Inputs <sup>1</sup>	GND − 0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	(Pulsed at 1 ms, 10% duty-cycle maximum)
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range, Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ <sub>JA</sub> Thermal Impedance	150°C/W
θ <sub>JC</sub> Thermal Impedance	27°C/W
LFCSP Package	
θ <sub>JA</sub> Thermal Impedance	70°C/W
IR Reflow, Peak Temperature <20 sec	235°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

**Table 5. ADG811/ADG812 Truth Table**

ADG811 IN	ADG812 IN	Switch Condition
0	1	On
1	0	Off

**Table 6. ADG813 Truth Table**

Logic	Switch 1, Switch 4	Switch 2, Switch 3
0	Off	On
1	On	Off

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

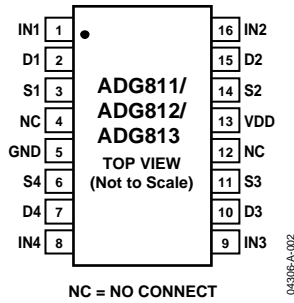
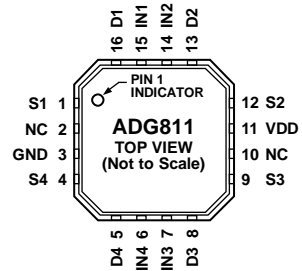


Figure 2. ADG811/ADG812/ADG813 Pin Configuration (16-Lead TSSOP)



NOTES  
 1. NC = NO CONNECT.  
 2. CONNECT EXPOSED PAD TO GND.

Figure 3. ADG811 Pin Configuration (16-Lead LFCSP)

**Table 7. ADG811/ADG812/ADG813 Pin Configuration (16-Lead TSSOP)**

Pin No.	Mnemonic	Definition
1	IN1	Logic control input.
2	D1	Drain Terminal. This pin may be an input or output.
3	S1	Source Terminal. This pin may be an input or output.
4	NC	No Connect.
5	GND	Ground (0 V) reference.
6	S4	Source Terminal. This pin may be an input or output.
7	D4	Drain Terminal. This pin may be an input or output.
8	IN4	Logic Control Input.
9	IN3	Logic Control Input.
10	D3	Drain Terminal. This pin may be an input or output.
11	S3	Source Terminal. This pin may be an input or output.
12	NC	No Connect.
13	VDD	Most Positive Power Supply Potential.
14	S2	Source Terminal. This pin may be an input or output.
15	D2	Drain Terminal. This pin may be an input or output.
16	IN2	Logic Control Input.

**Table 8. ADG811 Pin Configuration (16-Lead LFCSP)**

Pin No.	Mnemonic	Definition
1	S1	Source Terminal. This pin may be an input or output.
2	NC	No Connect.
3	GND	Ground (0 V) Reference.
4	S4	Source Terminal. This pin may be an input or output.
5	D4	Drain Terminal. This pin may be an input or output.
6	IN4	Logic Control Input.
7	IN3	Logic Control Input.
8	D3	Drain Terminal. This pin may be an input or output.
9	S3	Source Terminal. This pin may be an input or output.
10	NC	No Connect.
11	VDD	Most Positive Power Supply Potential.
12	S2	Source Terminal. This pin may be an input or output.
13	D2	Drain Terminal. This pin may be an input or output.
14	IN2	Logic Control Input.
15	IN1	Logic Control Input.
16	D1	Drain Terminal. This pin may be an input or output.
	EPAD	Connect exposed pad to GND.

## TYPICAL PERFORMANCE CHARACTERISTICS

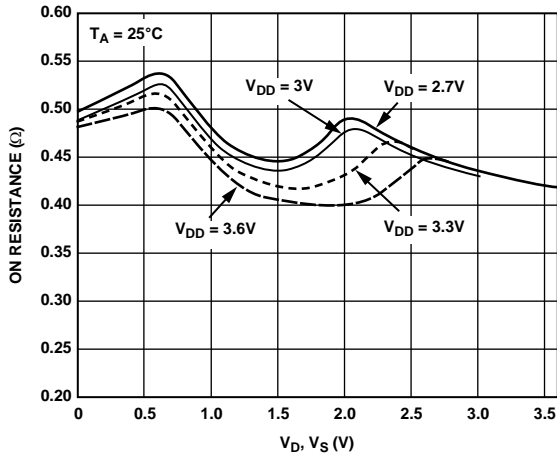


Figure 4. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.7V$  to  $3.6V$

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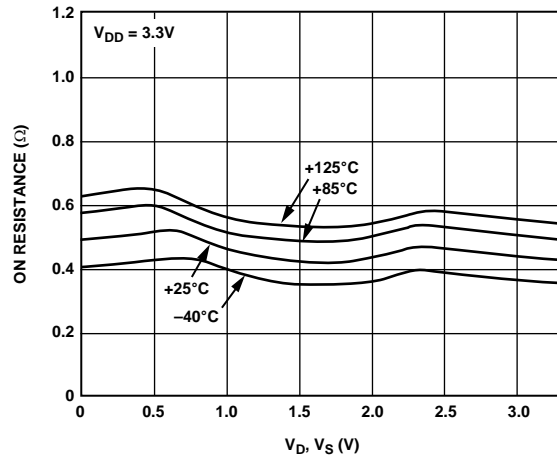


Figure 7. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 3.3V$

04306-A-006

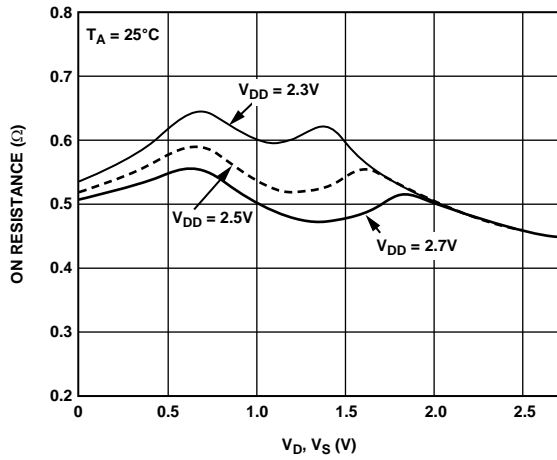


Figure 5. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.5V \pm 0.2V$

04306-A-004

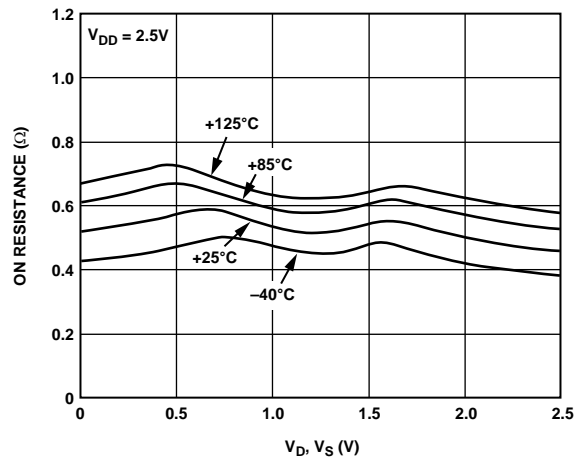


Figure 8. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 2.5V$

04306-A-007

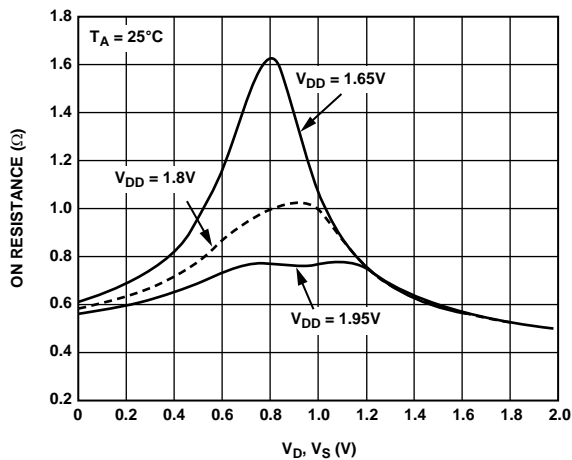


Figure 6. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 1.8V \pm 0.15V$

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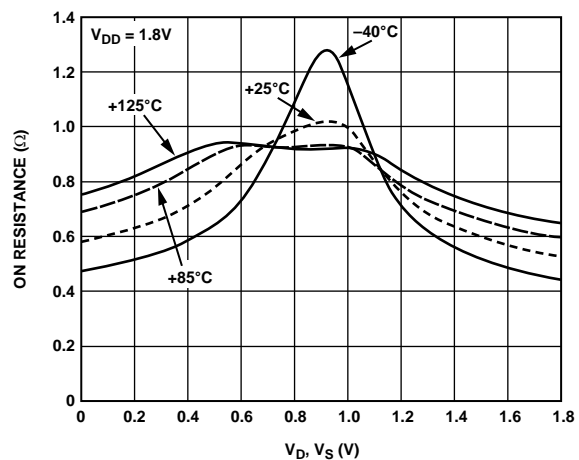


Figure 9. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 1.8V$

04306-A-008



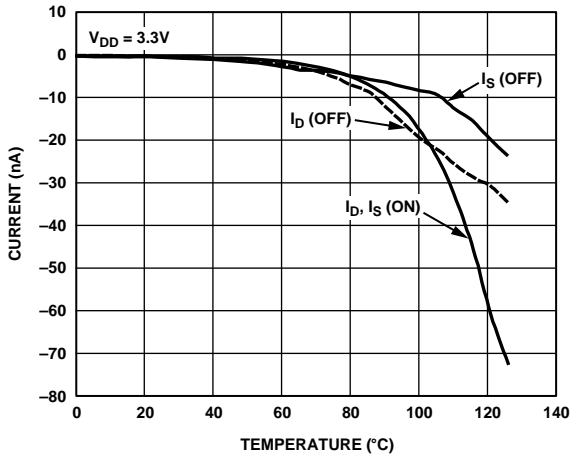


Figure 10. Leakage Current vs. Temperature,  $V_{DD} = 3.3V$

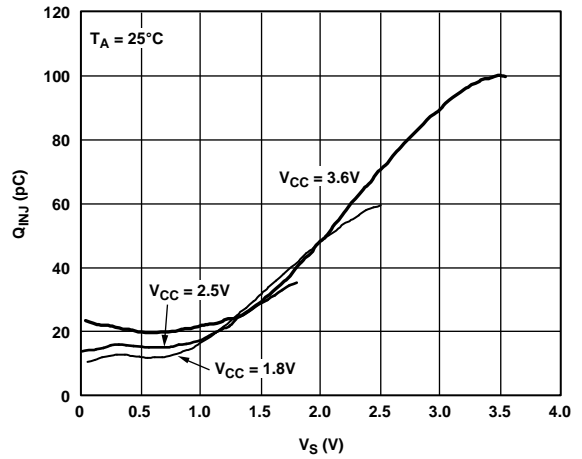


Figure 13. Charge Injection ( $Q_{INJ}$ ) vs. Source Voltage ( $V_S$ )

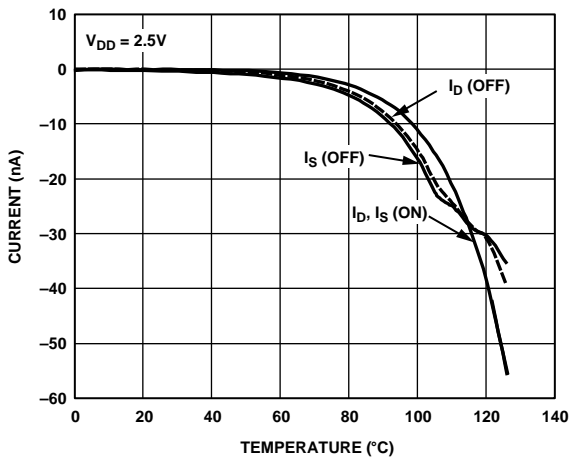


Figure 11. Leakage Current vs. Temperature,  $V_{DD} = 2.5V$

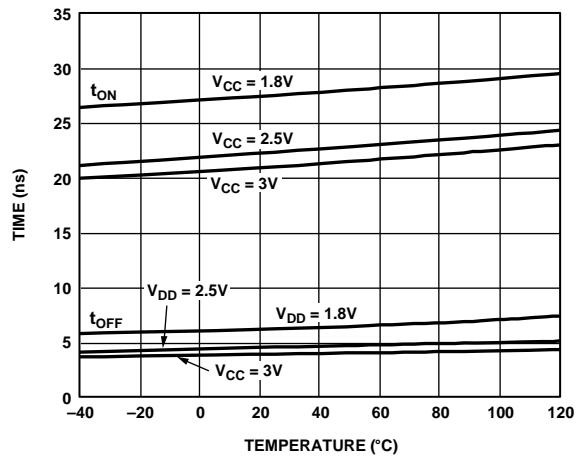


Figure 14.  $t_{ON}/t_{OFF}$  Times vs. Temperature

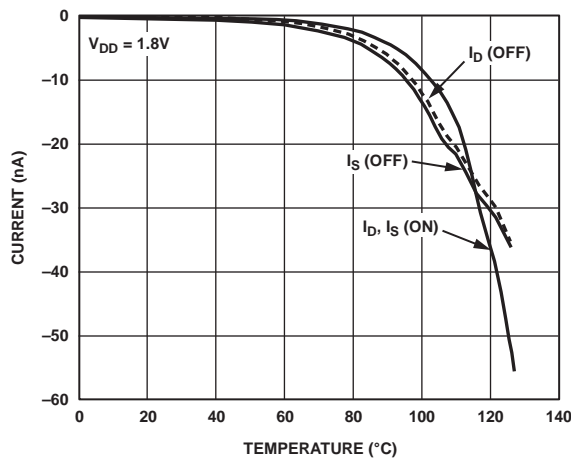


Figure 12. Leakage Current vs. Temperature,  $V_{DD} = 1.8V$

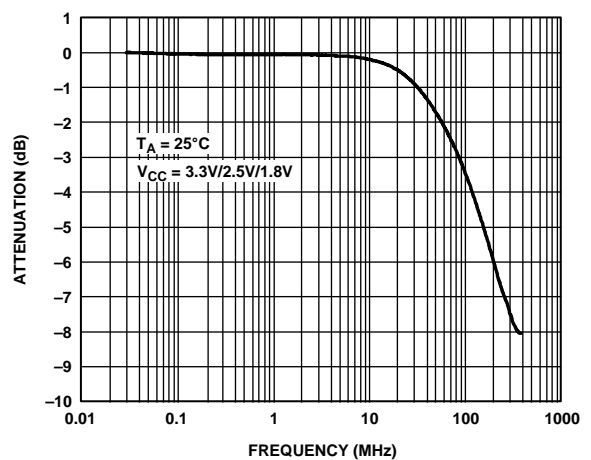


Figure 15. On Response vs. Frequency

04306-A-009

04306-A-012

04306-A-010

04306-A-013

04306-A-011

04306-A-014

# ADG811/ADG812/ADG813

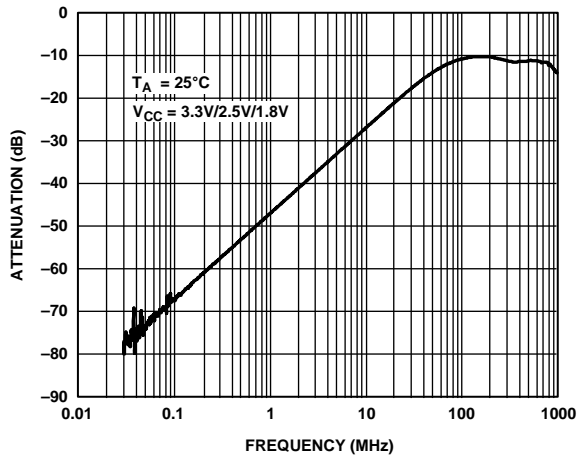


Figure 16. Crosstalk vs. Frequency

04306-A-015

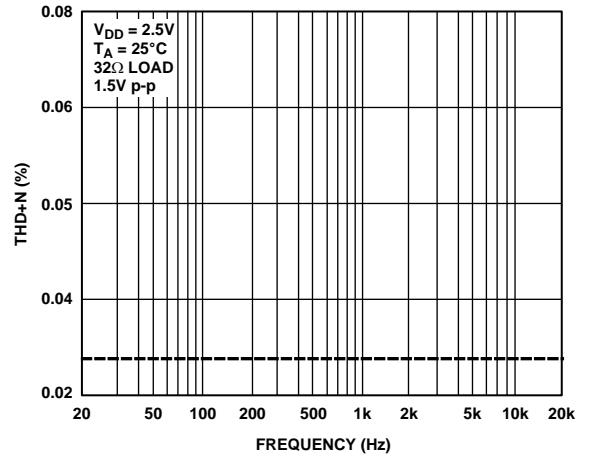


Figure 18. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

04306-A-017

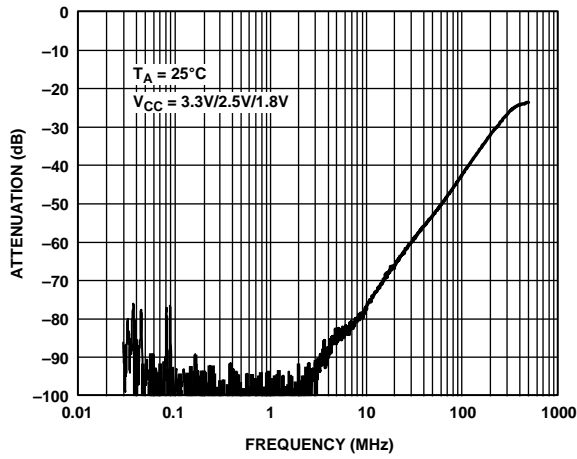


Figure 17. Off Isolation vs. Frequency

04306-A-016

TEST CIRCUITS

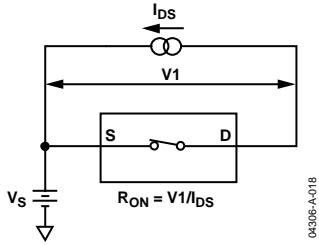


Figure 19. On Resistance

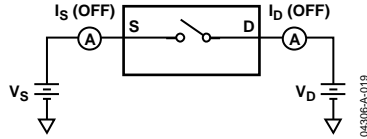


Figure 20. Off Leakage

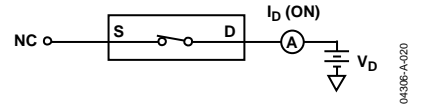


Figure 21. On Leakage

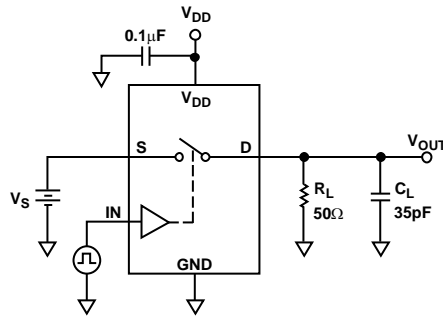


Figure 22. Switching Times

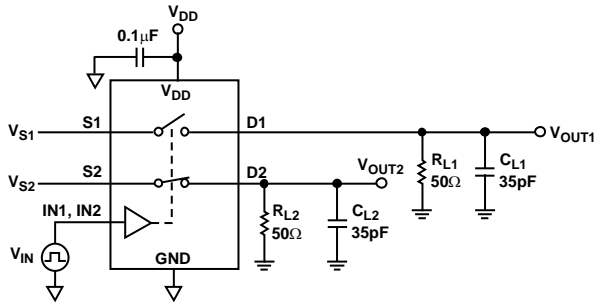
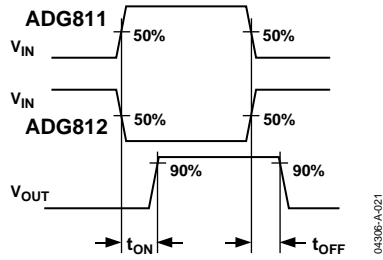


Figure 23. Break-Before-Make Time Delay,  $t_{BBM}$  (ADG813 Only)

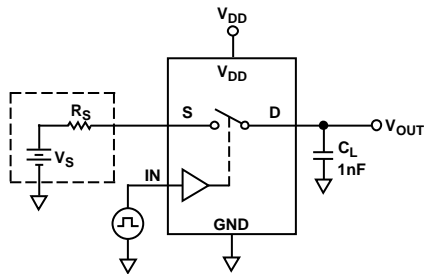
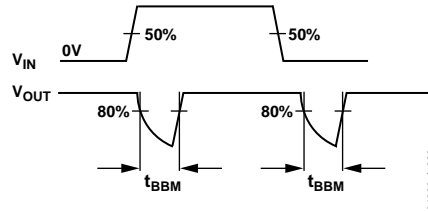
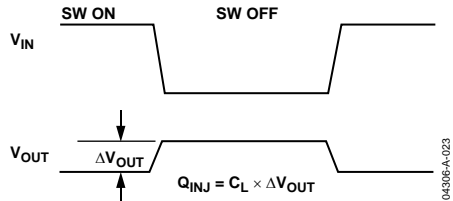
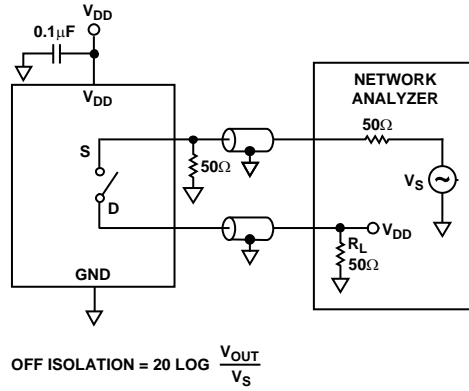


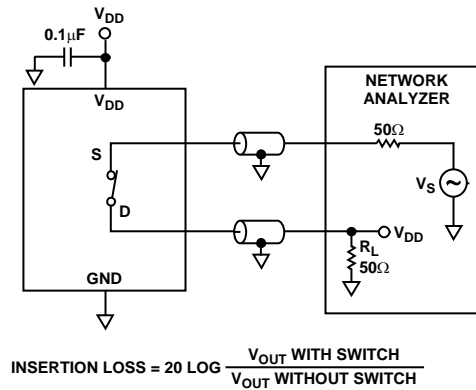
Figure 24. Charge Injection





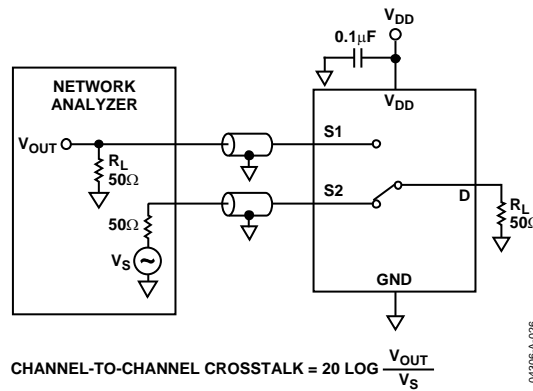
04306-A-024

Figure 25. Off Isolation



04306-A-025

Figure 26. Bandwidth



04306-A-026

Figure 27. Channel-to-Channel Crosstalk

## TERMINOLOGY

### $I_{DD}$

Positive supply current.

### $V_D, V_S$

Analog voltage on Terminal D, Terminal S.

### $R_{ON}$

Ohmic resistance between D and S.

### $R_{FLAT (ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

### $\Delta R_{ON}$

On resistance match between any two channels, that is,  $R_{ON}$  maximum –  $R_{ON}$  minimum.

### $I_S$ (Off)

Source leakage current with the switch off.

### $I_D$ (Off)

Drain leakage current with the switch off.

### $I_D, I_S$ (On)

Channel leakage current with the switch on.

### $V_{INL}$

Maximum input voltage for Logic 0.

### $V_{INH}$

Minimum input voltage for Logic 1.

### $I_{INL}$ ( $I_{INH}$ )

Input current of the digital input.

### $C_S$ (Off)

Off switch source capacitance. Measured with reference to ground.

### $C_D$ (Off)

Off switch drain capacitance. Measured with reference to ground.

### $C_D, C_S$ (On)

On switch capacitance. Measured with reference to ground.

### $C_{IN}$

Digital input capacitance.

### $t_{ON}$

Delay time between the 50% and the 90% points of the digital input and switch on condition.

### $t_{OFF}$

Delay time between the 50% and the 90% points of the digital input and switch off condition.

### $t_{BBM}$

On or off time measured between the 80% points of both switches, when switching from one to another.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on-to-off switching.

### Off Isolation

A measure of unwanted signal coupling through an off switch.

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another because of parasitic capacitance.

### –3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

### On Response

The frequency response of the on switch.

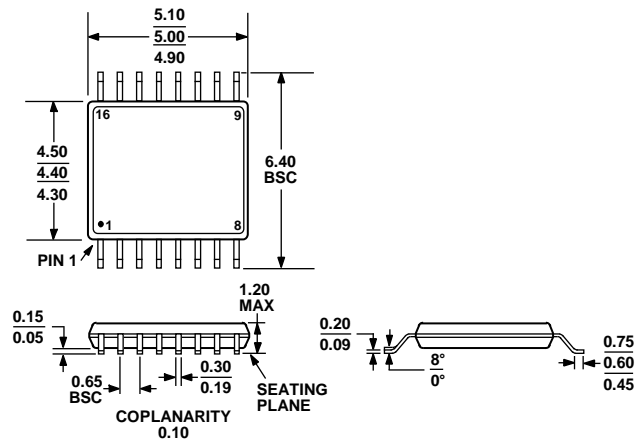
### Insertion Loss

The loss due to the on resistance of the switch.

### THD + N

The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.

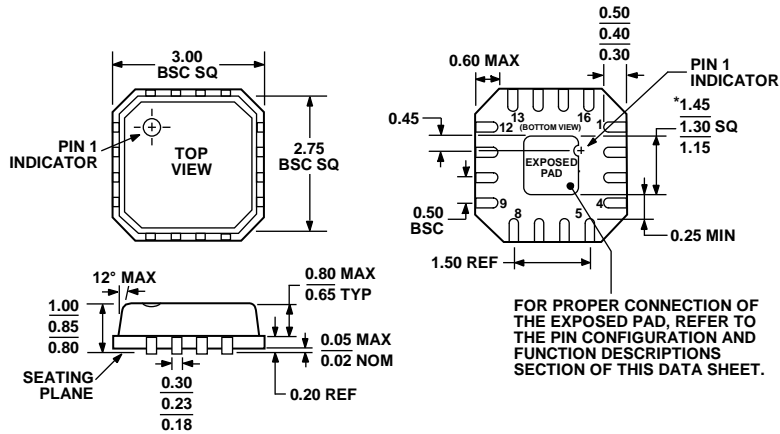
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 28. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



\*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2 EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 29. 16-Lead Lead Frame Chip Scale Package [LFCSP\_VQ] 3 mm × 3 mm Body, Very Thin Quad (CP-16-2)

Dimensions shown in millimeters

072208-A

**ORDERING GUIDE**

<b>Model</b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Package Option</b>
ADG811YRU	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG811YRU-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG811YRU-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG811YRUZ <sup>1</sup>	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG811YCPZ-REEL <sup>1</sup>	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-2
ADG811YCPZ-REEL7 <sup>1</sup>	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-2
ADG812YRU	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG812YRU-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG812YRU-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG812YRUZ <sup>1</sup>	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG812YRUZ-REEL7 <sup>1</sup>	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG813YRU	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG813YRU-REEL	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG813YRU-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG813YRUZ <sup>1</sup>	-40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**