Dual, Ultralow Noise Variable Gain Amplifier

AD604

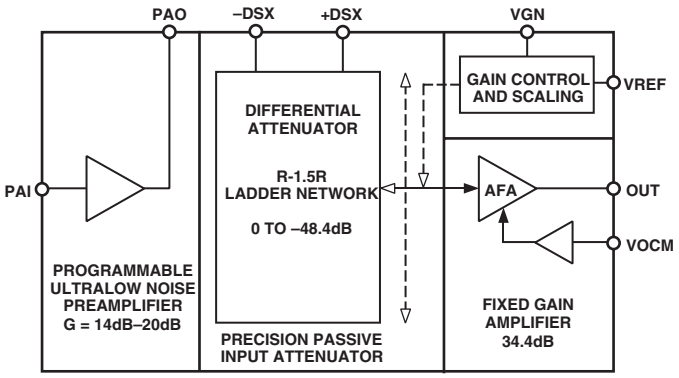
FEATURES

Ultralow Input Noise at Maximum Gain:
0.80 nV/√Hz, 3.0 pA/√Hz
2 Independent Linear-in-dB Channels
Absolute Gain Range per Channel Programmable:
0 dB to 48 dB (Preamp Gain = 14 dB), through
6 dB to 54 dB (Preamp Gain = 20 dB)
±1.0 dB Gain Accuracy
Bandwidth: 40 MHz (–3 dB)
300 kΩ Input Resistance
Variable Gain Scaling: 20 dB/V through 40 dB/V
Stable Gain with Temperature and Supply Variations
Single-Ended Unipolar Gain Control
Power Shutdown at Lower End of Gain Control
Can Drive ADCs Directly

APPLICATIONS

Ultrasound and Sonar Time-Gain Control
High Performance AGC Systems
Signal Measurement

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD604 is an ultralow noise, very accurate, dual-channel, linear-in-dB variable gain amplifier (VGA) optimized for time based variable gain control in ultrasound applications; however, it will support any application requiring low noise, wide bandwidth, variable gain control. Each channel of the AD604 provides a 300 kΩ input resistance and unipolar gain control for ease of use. User determined gain ranges, gain scaling (dB/V), and dc level shifting of output further optimize application performance.

Each channel of the AD604 utilizes a high performance preamplifier that provides an input referred noise voltage of 0.8 nV/√Hz. The very accurate linear-in-dB response of the AD604 is achieved with the differential input exponential amplifier (DSX-AMP) architecture. Each of the DSX-AMPs comprise a variable attenuator of 0 dB to 48.36 dB followed by a high speed fixed gain amplifier. The attenuator is based on a 7-stage R-1.5R ladder network. The attenuation between tap points is 6.908 dB and 48.36 dB for the ladder network.

Each independent channel of the AD604 provides a 48 dB gain range that can be optimized for the application by programming the preamplifier with a single external resistor in the preamp feedback path. The linear-in-dB gain response of the AD604 can be described by the equation

$$G\,(\mathrm{dB}) = \left(Gain\ Scaling\,(\mathrm{dB/V}) \times VGN\,(\mathrm{V})\right) + \left(Preamp\ Gain\,(\mathrm{dB}) - 19\,\mathrm{dB}\right)$$

Preamplifier gains between 5 and 10 (14 dB and 20 dB) provide overall gain ranges per channel of 0 dB through 48 dB and 6 dB through 54 dB. The two channels of the AD604 can be cascaded to provide greater levels of gain range by bypassing the second channel's preamplifier. However, in multiple channel systems, cascading the AD604 with other devices in the AD60x VGA family that do not include a preamplifier may provide a more efficient solution. The AD604 provides access to the output of the preamplifier, allowing for external filtering between the preamplifier and the differential attenuator stage.

The gain control interface of the AD604 provides an input resistance of approximately 2 MΩ and scale factors from 20 dB/V to 30 dB/V for a VREF input voltage of 2.5 V to 1.67 V, respectively. Note that scale factors up to 40 dB/V are achievable with reduced accuracy for scales above 30 dB/V. The gain scales linear-in-dB with control voltages of 0.4 V to 2.4 V with the 20 dB/V scale. Below and above this gain control range, the gain begins to deviate from the ideal linear-in-dB control law. The gain control region below 0.1 V is not used for gain control. In fact when the gain control voltage is <50 mV, the amplifier channel is powered down to 1.9 mA.

The AD604 is available in a 24-lead SSOP, SOIC, and PDIP package and is guaranteed for operation over the –40°C to +85°C temperature range.

REV. A

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AD604–SPECIFICATIONS

Each Amplifier Channel at T_A = 25°C, V_S = ±5 V, R_S = 50 Ω, R_L = 500 Ω, C_L = 5 pF, V_{REF} = 2.50 V (Scaling = 20 dB/V), 0 dB to 48 dB gain range (preamplifier gain = 14 dB), VOCM = 2.5 V, C1 and C2 = 0.1 μF (see Figure 35), unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Preamplifier					
Input Resistance			300		kΩ
Input Capacitance			8.5		pF
Input Bias Current			–27		μA
Peak Input Voltage	Preamp Gain = 14 dB		±400		mV
	Preamp Gain = 20 dB		±200		mV
Input Voltage Noise	VGN = 2.9 V, R_S = 0 Ω				
	Preamp Gain = 14 dB		0.8		$nV/\sqrt{Hz}$
	Preamp Gain = 20 dB		0.73		$nV/\sqrt{Hz}$
Input Current Noise	Independent of Gain		3.0		$pA/\sqrt{Hz}$
Noise Figure	R_S = 50 Ω, f = 10 MHz, VGN = 2.9 V		2.3		dB
	R_S = 200 Ω, f =10 MHz, VGN = 2.9 V		1.1		dB
DSX					
Input Resistance			175		Ω
Input Capacitance			3.0		pF
Peak Input Voltage			2.5 ± 2		V
Input Voltage Noise	VGN = 2.9 V		1.8		$nV/\sqrt{Hz}$
Input Current Noise	VGN = 2.9 V		2.7		$pA/\sqrt{Hz}$
Noise Figure	R_S = 50 Ω, f = 10 MHz, VGN = 2.9 V		8.4		dB
	R_S = 200 Ω, f =10 MHz, VGN = 2.9 V		12		dB
Common-Mode Rejection Ratio	f = 1 MHz, VGN = 2.65 V		–20		dB
OUTPUT CHARACTERISTICS					
–3 dB Bandwidth	Constant with Gain		40		MHz
Slew Rate	VGN = 1.5 V, Output = 1 V Step		170		V/μs
Output Signal Range	R_L ≥ 500 Ω		2.5 ± 1.5		V
Output Impedance	f = 10 MHz		2		Ω
Output Short-Circuit Current			±40		mA
Harmonic Distortion	VGN = 1 V, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		–54		dBc
HD3	f = 1 MHz		–67		dBc
HD2	f = 10 MHz		–43		dBc
HD3	f = 10 MHz		–48		dBc
Two-Tone Intermodulation	VGN = 2.9 V, V_{OUT} = 1 V p-p				
Distortion (IMD)	f = 1 MHz		–74		dBc
	f = 10 MHz		–71		dBc
Third-Order Intercept	f = 10 MHz, VGN = 2.65 V, V_{OUT} = 1 V p-p, Input Referred		–12.5		dBm
1 dB Compression Point	f = 1 MHz, VGN = 2.9 V, Output Referred		15		dBm
Channel-to-Channel Crosstalk	V_{OUT} = 1 V p-p, f = 1 MHz				
	Ch No. 1: VGN = 2.65 V, Inputs Shorted		–30		dB
	Ch No. 2: VGN = 1.5 V (Mid Gain)				dB
Group Delay Variation	1 MHz < f < 10 MHz, Full Gain Range		±2		ns
VOCM Input Resistance			45		kΩ
ACCURACY					
Absolute Gain Error					
0 dB to 3 dB	0.25 V < VGN < 0.400 V	–1.2	+0.75	+3	dB
3 dB to 43 dB	0.400 V < VGN < 2.400 V	–1.0	±0.3	+1.0	dB
43 dB to 48 dB	2.400 V < VGN < 2.65 V	–3.5	–1.25	+1.2	dB
Gain Scaling Error	0.400 V < VGN < 2.400 V		±0.25		dB/V
Output Offset Voltage	VREF = 2.500 V, VOCM = 2.500 V	–50	±30	+50	mV
Output Offset Variation	VREF = 2.500 V, VOCM = 2.500 V		30	50	mV

SPECIFICATIONS

Parameter	Conditions	Min	Typ	Max	Unit
GAIN CONTROL INTERFACE					
Gain Scaling Factor	VREF = 2.5 V, 0.4 V < VGN < 2.4 V	19	20	21	dB/V
	VREF = 1.67 V		30		dB/V
Gain Range	Preamp Gain = 14 dB		0 to 48		dB
	Preamp Gain = 20 dB		6 to 54		dB
Input Voltage (VGN) Range	20 dB/V, VREF = 2.5 V		0.1 to 2.9		V
Input Bias Current			–0.4		μA
Input Resistance			2		MΩ
Response Time	48 dB Gain Change		0.2		μs
VREF Input Resistance			10		kΩ
POWER SUPPLY					
Specified Operating Range	One Complete Channel		±5		V
	One DSX Only		5		V
Power Dissipation	One Complete Channel		220		mW
	One DSX Only		95		mW
Quiescent Supply Current	VPOS, One Complete Channel		32	36	mA
	VPOS, One DSX Only		19	23	mA
	VNEG, One Preamplifier Only	–15	–12		mA
Powered Down	VPOS, VGN < 50 mV, One Channel		1.9	3.0	mA
	VNEG, VGN < 50 mV, One Channel		–150		μA
Power-Up Response Time	48 dB Gain Change, V_{OUT} = 2 V p-p		0.6		μs
Power-Down Response Time			0.4		μs

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

Supply Voltage $\pm V_S$
- Pins 17, 18, 19, 20 (with Pins 16, 22 = 0 V) ..... ±6.5 V

Input Voltages
- Pins 1, 2, 11, 12 ..... VPOS/2 ± 2 V Continuous
- Pins 4, 9 ..... ±2 V
- Pins 5, 8 ..... VPOS, VNEG
- Pins 6, 7, 13, 14, 23, 24 ..... VPOS, 0

Internal Power Dissipation
- PDIP (N) ..... 2.2 W
- SOIC (R) ..... 1.7 W
- SSOP (RS) ..... 1.1 W

Operating Temperature Range ..... –40°C to +85°C

Storage Temperature Range ..... –65°C to +150°C

Lead Temperature, Soldering 60 sec ..... 300°C

θ_{JA}[4]
- AD604AN ..... 105°C
- AD604AR ..... 73°C
- AD604ARS ..... 112°C

θ_{JC}[4]
- AD604AN ..... 35°C
- AD604AR ..... 38°C
- AD604ARS ..... 34°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Pins 1, 2, 11, 12, 13, 14, 23, 24 are part of a single-supply circuit. The part will most likely be damaged if any of these pins are accidentally connected to VN.

[3]When driven from an external low impedance source.

[4]Using MIL STD 883 test method G43-87 with a 1S (2-layer) test board.

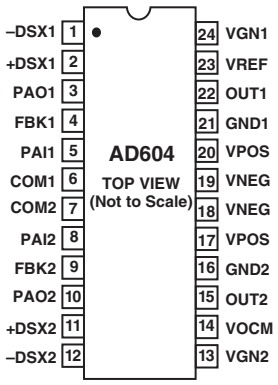
ORDERING GUIDE

Model	Temperature Range	Package Option	Description
AD604AN	–40°C to +85°C	N-24	PDIP
AD604AR	–40°C to +85°C	R-24	SOIC
AD604AR-REEL	–40°C to +85°C	R-24	SOIC
AD604ARS	–40°C to +85°C	RS-24	SSOP
AD604ARS-REEL	–40°C to +85°C	RS-24	SSOP
AD604ARS-REEL7	–40°C to +85°C	RS-24	SSOP
AD604-EB			Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD604 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	–DSX1	CH1 Negative Signal Input to DSX1.
2	+DSX1	CH1 Positive Signal Input to DSX1.
3	PAO1	CH1 Preamplifier Output.
4	FBK1	CH1 Preamplifier Feedback Pin.
5	PAI1	CH1 Preamplifier Positive Input.
6	COM1	CH1 Signal Ground. When connected to positive supply, Preamplifier 1 will shut down.
7	COM2	CH2 Signal Ground. When connected to positive supply, Preamplifier 2 will shut down.
8	PAI2	CH2 Preamplifier Positive Input.
9	FBK2	CH2 Preamplifier Feedback Pin.
10	PAO2	CH2 Preamplifier Output.
11	+DSX2	CH2 Positive Signal Input to DSX2.
12	–DSX2	CH2 Negative Signal Input to DSX2.
13	VGN2	CH2 Gain-Control Input and Power-Down Pin. If grounded, device is off; otherwise, positive voltage increases gain.
14	VOCM	Input to this pin defines the common-mode of the output at OUT1 and OUT2.
15	OUT2	CH2 Signal Output.
16	GND2	Ground.
17	VPOS	Positive Supply.
18	VNEG	Negative Supply.
19	VNEG	Negative Supply.
20	VPOS	Positive Supply.
21	GND1	Ground.
22	OUT1	CH1 Signal Output.
23	VREF	Input to this pin sets gain-scaling for both channels to 2.5 V = 20 dB/V, 1.67 V = 30 dB/V.
24	VGN1	CH1 Gain-Control Input and Power-Down Pin. If grounded, the device is off; otherwise, positive voltage increases gain.

Unless otherwise noted, G (preamp) = 14 dB, VREF = 2.5 V (20 dB/V Scaling), f = 1 MHz, R_L = 500 Ω, C_L = 5 pF, T_A = 25°C, V_{SS} = ±5 V

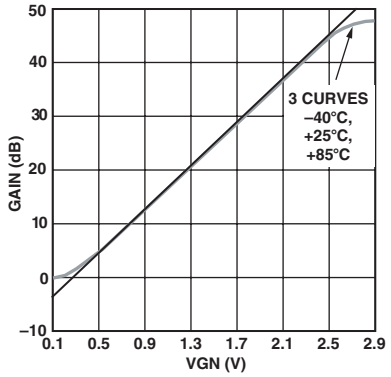


Figure 1. Gain vs. VGN for Three Temperatures

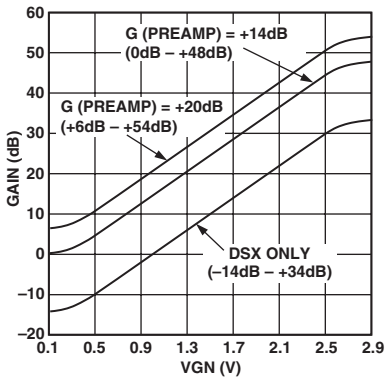


Figure 2. Gain vs. VGN for Different Preamp Gains

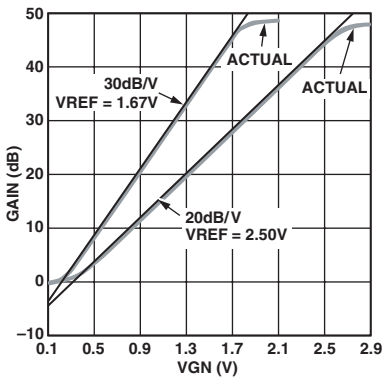


Figure 3. Gain vs. VGN for Different Gain Scalings

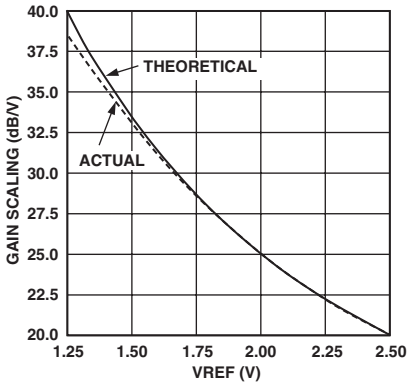


Figure 4. Gain Scaling vs. VREF

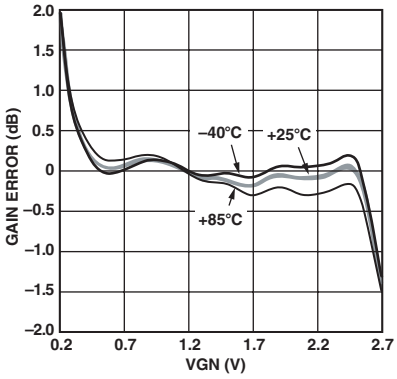


Figure 5. Gain Error vs. VGN at Different Temperatures

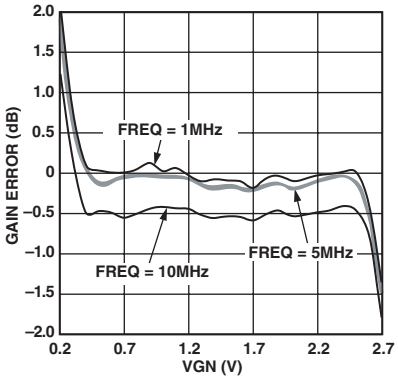


Figure 6. Gain Error vs. VGN at Different Frequencies

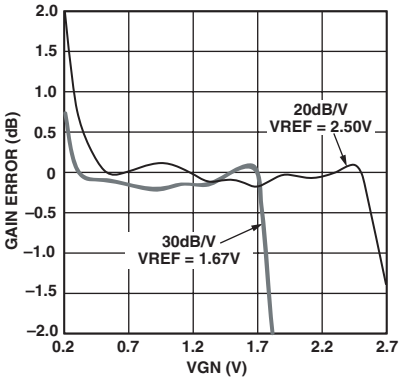


Figure 7. Gain Error vs. VGN for Different Gain Scalings

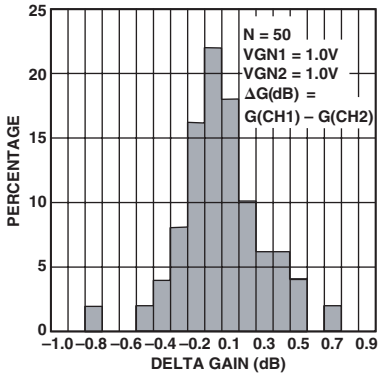


Figure 8. Gain Match; VGN1 = VGN2 = 1.0 V

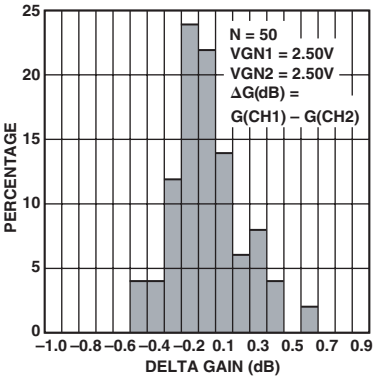


Figure 9. Gain Match: VGN1 = VGN2 = 2.50 V

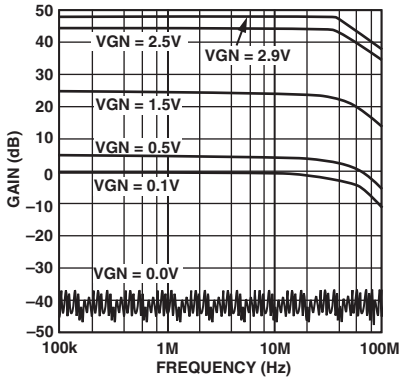


Figure 10. AC Response

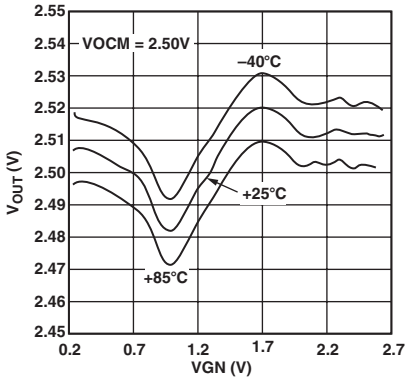


Figure 11. Output Offset vs. VGN

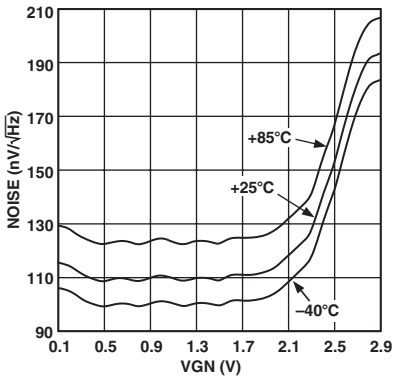


Figure 12. Output Referred Noise vs. VGN

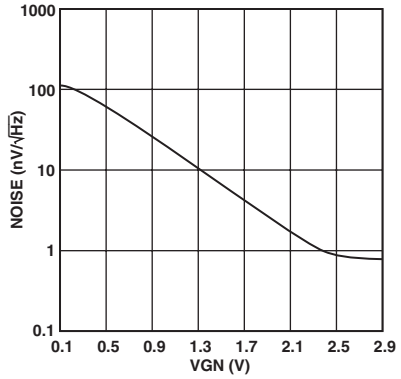


Figure 13. Input Referred Noise vs. VGN

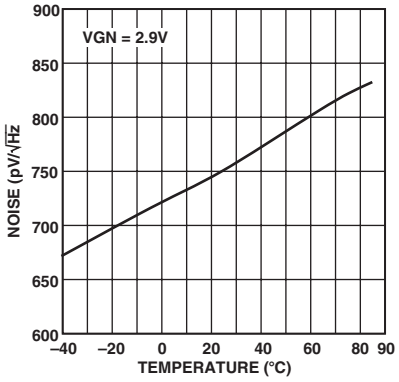


Figure 14. Input Referred Noise vs. Temperature

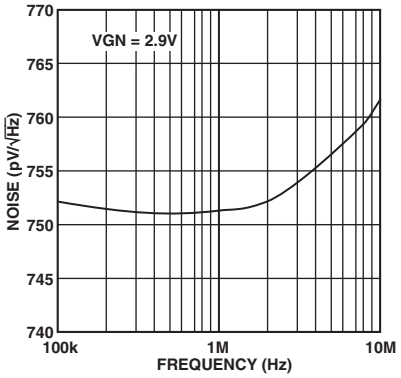


Figure 15. Input Referred Noise vs. Frequency

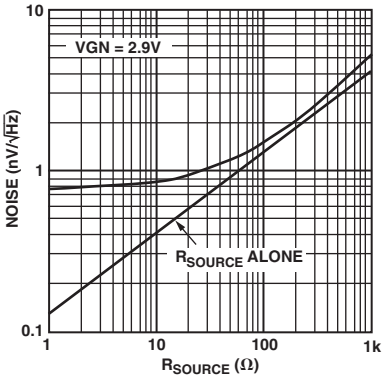


Figure 16. Input Referred Noise vs. R_{SOURCE}

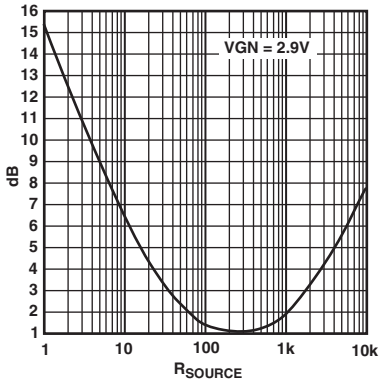


Figure 17. Noise Figure vs. R_{SOURCE}

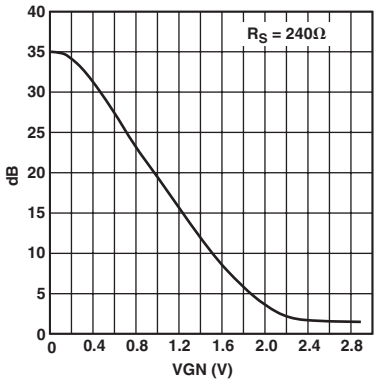


Figure 18. Noise Figure vs. VGN

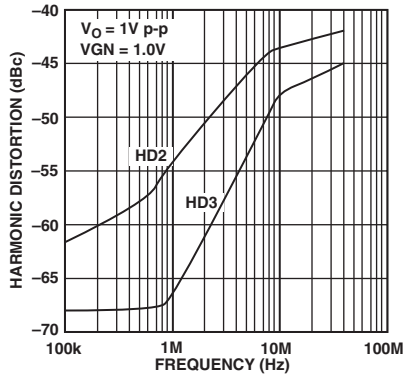


Figure 19. Harmonic Distortion vs. Frequency

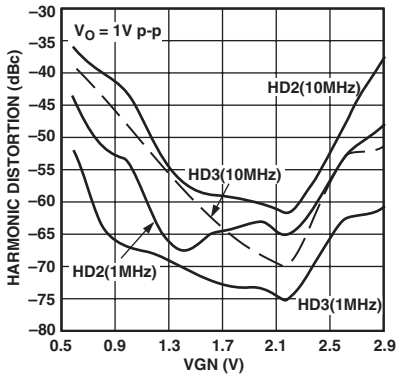


Figure 20. Harmonic Distortion vs. VGN

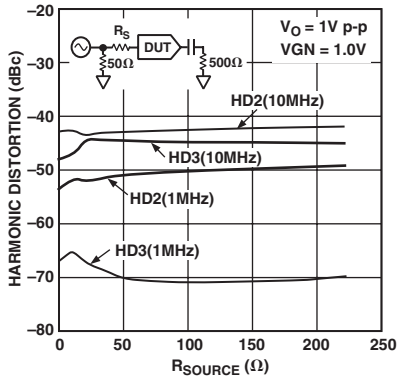


Figure 21. Harmonic Distortion vs. R_{SOURCE}

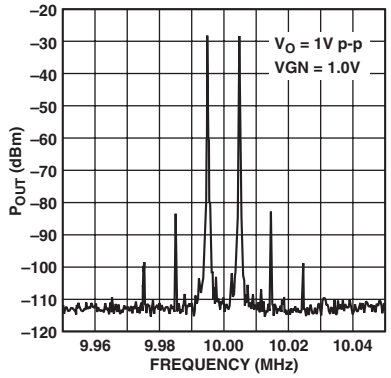


Figure 22. Intermodulation Distortion

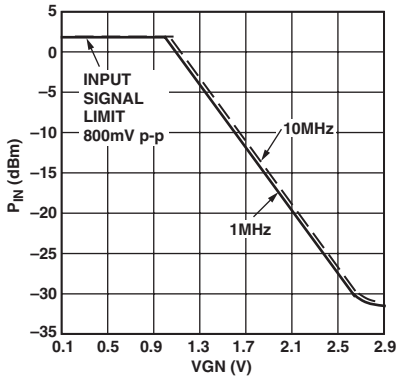


Figure 23. 1 dB Compression vs. VGN

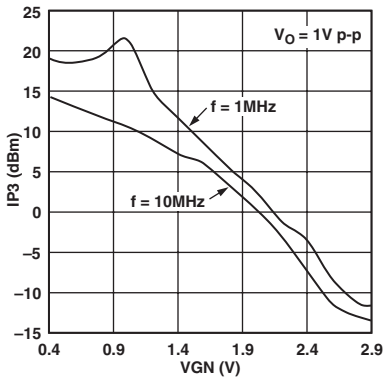


Figure 24. Third-Order Intercept vs. VGN

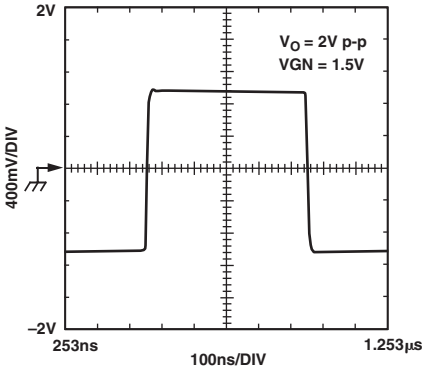


Figure 25. Large Signal Pulse Response

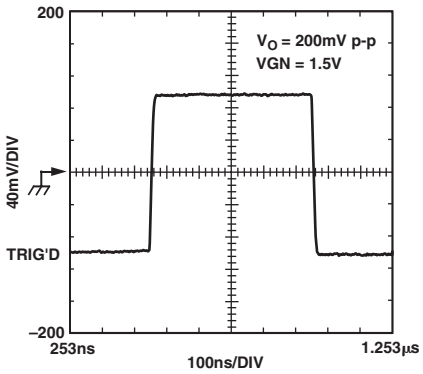


Figure 26. Small Signal Pulse Response

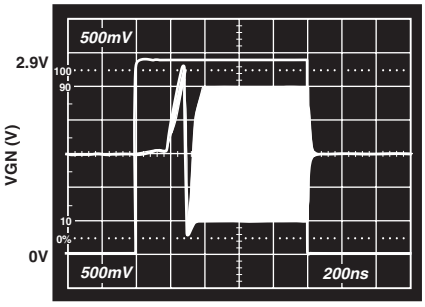


Figure 27. Power-Up/Down Response

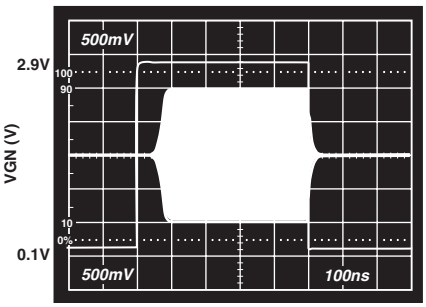


Figure 28. Gain Response

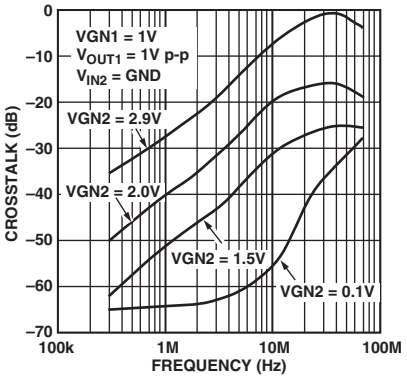


Figure 29. Crosstalk (CH1 to CH2) vs. Frequency

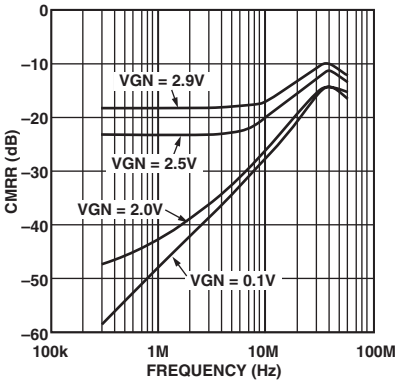


Figure 30. DSX Common-Mode Rejection vs. Frequency

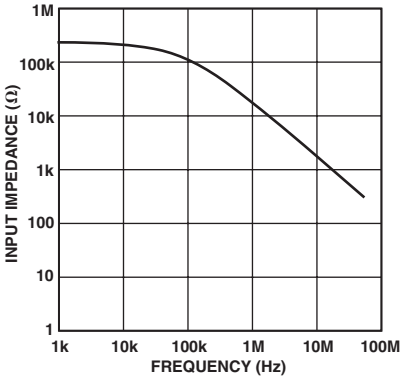


Figure 31. Input Impedance vs. Frequency

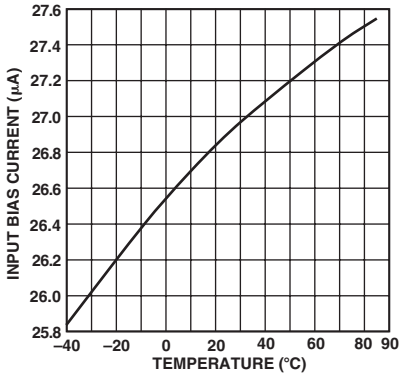


Figure 32. Input Bias Current vs. Temperature

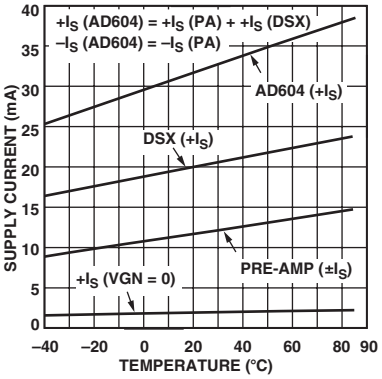


Figure 33. Supply Current (One Channel) vs. Temperature

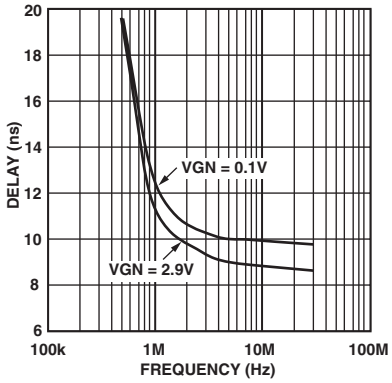


Figure 34. Group Delay vs. Frequency

THEORY OF OPERATION

The AD604 is a dual-channel, variable gain amplifier with an ultralow noise preamplifier. Figure 35 shows the simplified block diagram of one channel. Each channel consists of:

(1) a preamplifier with gain setting Resistors R5, R6, and R7

(2) a single-supply X-AMP® (hereafter called DSX, differential single-supply X-AMP) made up of:

(a) a precision passive attenuator (differential ladder)

(b) a gain control block

(c) a VOCM buffer with supply-splitting Resistors R3 and R4

(d) an active feedback amplifier[1] (AFA) with gain-setting Resistors R1 and R2

The preamplifier is powered by a ±5 V supply, while the DSX uses a single +5 V supply. The linear-in-dB gain response of the AD604 can generally be described by:

$$G\,(\mathrm{dB}) = (Gain\ Scaling\,(\mathrm{dB/V})) \times (Gain\ Control\,(\mathrm{V})) + ((Preamp\ Gain\,(\mathrm{dB})) - 19\,\mathrm{dB}) \quad (1)$$

Each channel provides between 0 dB to 48.4 dB through 6 dB to 54.4 dB of gain depending on the user determined preamplifier gain. The center 40 dB of gain is exactly linear-in-dB while the gain error increases at the top and bottom of the range. The gain of the preamplifier is typically either 14 dB or 20 dB but can be set to intermediate values by a single external resistor (see Preamplifier section for details). The gain of the DSX can vary from –14 dB to +34.4 dB, as is determined by the gain control voltage (VGN). The VREF input establishes the gain scaling; the useful gain scaling range is between 20 dB/V and 40 dB/V for a VREF voltage of 2.5 V and 1.25 V, respectively. For example, if the preamp gain was set to 14 dB and VREF was set to 2.50 V (to establish a gain scaling of 20 dB/V), the gain equation would simplify to

$$G\,(\mathrm{dB}) = (20\,(\mathrm{dB/V})) \times (VGN\,(\mathrm{V})) - 5\,\mathrm{dB}$$

The desired gain can then be achieved by setting the unipolar gain control (VGN) to a voltage within its nominal operating range of 0.25 V to 2.65 V (for 20 dB/V gain scaling). The gain is monotonic for a complete gain control voltage range of 0.1 V to 2.9 V. Maximum gain can be achieved at a VGN of 2.9 V.

Since the two channels are identical, only Channel 1 will be used to describe their operation. VREF and VOCM are the only inputs that are shared by the two channels, and since they are normally ac grounds, crosstalk between the two channels is minimized. For highest gain scaling accuracy, VREF should have an external low impedance voltage source. For low accuracy 20 dB/V applications, the VREF input can be decoupled with a capacitor to ground. In this mode, the gain scaling is determined by the midpoint between $+V_{CC}$ and GND, so care should be taken to control the supply voltage to 5 V. The input resistance looking into the VREF pin is 10 kΩ ± 20%.

The DSX portion of the AD604 is a single-supply circuit, and the VOCM pin is used to establish the dc level of the midpoint of this portion of the circuit. VOCM needs only an external decoupling capacitor to ground to center the midpoint between the supply voltages (5 V, GND); however, if the dc level of the output is important to the user (see the Applications section for AD9050 example), then VOCM can be specifically set. The input resistance looking into the VOCM pin is 45 kΩ ± 20%.

Preamplifier

The input capability of the following single-supply DSX (2.5 ± 2 V for a +5 V supply) limits the maximum input voltage of the preamplifier to ±400 mV for the 14 dB gain configuration or ±200 mV for the 20 dB gain configuration.

The preamplifier's gain can be programmed to 14 dB or 20 dB by either shorting the FBK1 node to PAO1 (14 dB) or by leaving node FBK1 open (20 dB). These two gain settings are very accurate since they are set by the ratio of on-chip resistors. Any intermediate gain can be achieved by connecting the appropriate resistor value between PAO1 and FBK1 according to Equations 2 and 3.

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(R7 \| R_{EXT}) + R5 + R6}{R6} \quad (2)$$

$$R_{EXT} = \frac{[R6 \times G - (R5 + R6)] \times R7}{R7 - (R6 \times G) + (R5 + R6)} \quad (3)$$

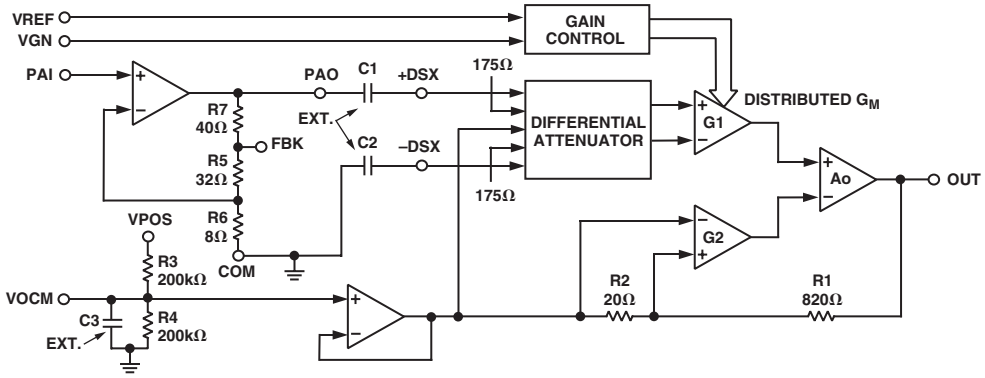
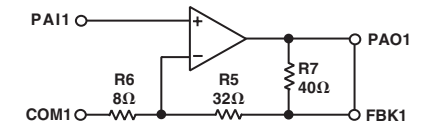


Figure 35. Simplified Block Diagram of a Single Channel of the AD604

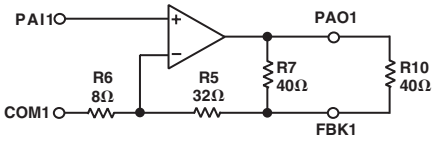
[1]To understand the active-feedback amplifier topology, refer to the AD830 data sheet. The AD830 is a practical implementation of the idea.

Since the internal resistors have an absolute tolerance of ±20%, the gain can be in error by as much as 0.33 dB when R_{EXT} is 30 Ω, where it was assumed that R_{EXT} is exact.

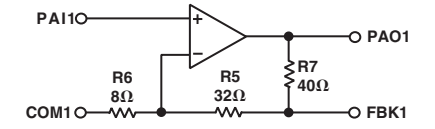
Figure 36 shows how the preamplifier is set to gains of 14, 17.5, and 20 dB. The gain range of a single channel of the AD604 is 0 dB to 48 dB when the preamplifier is set to 14 dB (Figure 36a), 3.5 dB to 51.5 dB for a preamp gain of 17.5 dB (Figure 36b), and 6 dB to 54 dB for the highest preamp gain of 20 dB (Figure 36c).



a. Preamp Gain = 14 dB



b. Preamp Gain = 17.5 dB



c. Preamp Gain = 20 dB

Figure 36. Preamplifier Gain Programmability

For a preamplifier gain of 14 dB, the preamplifier's –3 dB small signal bandwidth is 130 MHz; when the gain is at the high end (20 dB), the bandwidth will be reduced by a factor of two to 65 MHz. Figure 37 shows the ac responses for the three preamp gains discussed above; note that the gain for an R_{EXT} of 40 Ω should be 17.5 dB, but the mismatch between the internal resistors and the external resistor has caused the actual gain for this particular preamplifier to be 17.7 dB. The –3 dB small signal bandwidth of one complete channel of the AD604 (preamplifier and DSX) is 40 MHz and is independent of gain.

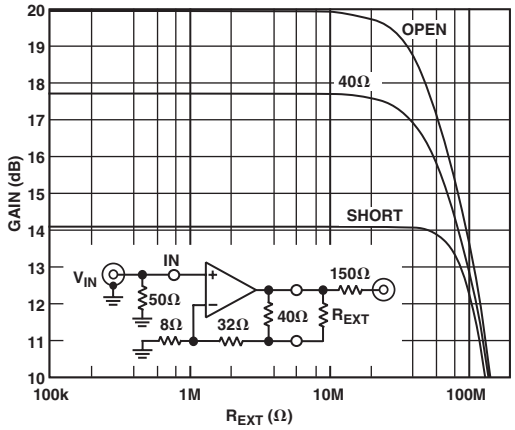


Figure 37. AC Responses for Preamplifier Gains Shown in Figure 36.

To achieve its optimum specifications, power and ground management are critical to the AD604. Large dynamic currents result because of the low resistances needed for the desired noise performance. Most of the difficulty is with the very low gain setting resistors of the preamplifier that allow for a total input referred noise, including the DSX, as low as 0.8 nV/√Hz. The consequently large dynamic currents have to be carefully handled to maintain performance even at large signal levels.

To accommodate these large dynamic currents as well as a ground referenced input, the preamplifier is operated from a dual ±5 V supply. This causes the preamplifier's output to also be ground referenced, which requires a common-mode level shift into the single-supply DSX. The two external coupling capacitors (C1, C2 in Figure 35) connected to nodes PAO1 and +DSX, and –DSX and ground, respectively, perform this function (see the AC Coupling section). In addition, they eliminate any offset that would otherwise be introduced by the preamplifier. It should be noted that an offset of 1 mV at the input of the DSX will get amplified by 34.4 dB (× 52.5) when the gain-control voltage is at its maximum; this equates to 52.5 mV at the output. AC coupling is consequently required to keep the offset from degrading the output signal range.

The internal feedback resistors setting the gain of the preamplifier are so small (nominally 8 Ω and 32 Ω) that even an additional 1 Ω in the "ground" connection at Pin COM1, which serves as the input common-mode reference, will seriously degrade gain accuracy and noise performance. This node is very sensitive and careful attention is necessary to minimize the ground impedance. All connections to node COM1 should be as short as possible.

The preamplifier including the gain setting resistors has a noise performance of 0.71 nV/√Hz and 3 pA/√Hz. Note that a significant portion of the total input referred voltage noise is due to the feedback resistors. The equivalent noise resistance presented by R5 and R6 in parallel is nominally 6.4 Ω, which contributes 0.33 nV/√Hz to the total input referred voltage noise. The larger portion of the input referred voltage noise is coming from the amplifier with 0.63 nV/√Hz. The current noise is independent of gain and depends only on the bias current in the input stage of the preamplifier—it is 3 pA/√Hz.

The preamplifier can drive 40 Ω (the nominal feedback resistors) and the following 175 Ω ladder load of the DSX with low distortion. For example, at 10 MHz and ±1 V at the output, the preamplifier has less than –45 dB of second and third harmonic distortion when driven from a low (25 Ω) source resistance.

In some cases, one may need more than 48 dB of gain range, in which case two AD604 channels could be cascaded. Since the preamplifier has limited input signal range, consumes over half (120 mW) of the total power (220 mW), and its ultralow noise is not necessary after the first AD604 channel, a shutdown mechanism that disables only the preamplifier is built in. All that is required to shut down the preamplifier is to tie the COM1 and/or COM2 pin to the positive supply. The DSX will be unaffected and can be used as before (see the Applications section for further details).

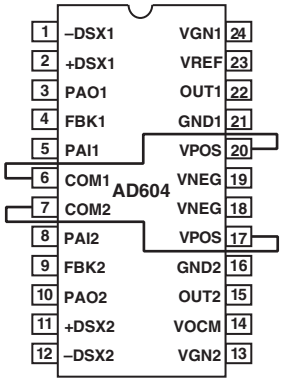


Figure 38. Shutdown of Preamplifiers Only

Differential Ladder (Attenuator)

The attenuator before the fixed gain amplifier of the DSX is realized by a differential 7-stage R-1.5R resistive ladder network with an untrimmed input resistance of 175 Ω single-ended or 350 Ω differential. The signal applied at the input of the ladder network (Figure 39) is attenuated by 6.908 dB per tap; thus, the attenuation at the first tap is 0 dB, at the second, 13.816 dB, and so on, all the way to the last tap where the attenuation is 48.356 dB. A unique circuit technique is used to interpolate continuously between the tap points, thereby providing continuous attenuation from 0 to –48.36 dB. Think of the ladder network together with the interpolation mechanism as a voltage-controlled potentiometer.

Since the DSX is a single-supply circuit, some means of biasing its inputs must be provided. Node MID together with the VOCM buffer perform this function. Without internal biasing, the user would have had to dc bias the inputs externally. If not done carefully, the biasing network can introduce additional noise and offsets. By providing internal biasing, the user is relieved of this task and only needs to ac couple the signal into the DSX. It should be made clear again that the input to the DSX is still fully differential if driven differentially, i.e., pins +DSX and –DSX see the same signal but with opposite polarity (see the Ultralow Noise, Differential Input-Differential Output VGA section). What changes is the load as seen by the driver; it is 175 Ω when each input is driven single ended, but 350 Ω when driven differentially. This can be easily explained when thinking of the ladder network as just two 175 Ω resistors connected back-to-back with the middle node, MID, being biased by the VOCM buffer. A differential signal applied between nodes +DSX and –DSX results in zero current into node MID, but a single-ended signal applied to either input, +DSX or –DSX while the other input is ac grounded causes the current delivered by the source to flow into the VOCM buffer via node MID.

The ladder resistor value of 175 Ω was chosen to provide the optimum balance between the load driving capability of the preamplifier and the noise contribution of the resistors. One feature of the X-AMP architecture is that the output referred noise is constant versus gain over most of the gain range. This can be easily explained by looking at Figure 39 and observing that the tap resistance is equal for all taps after only a few taps away from the inputs. The resistance seen looking into each tap is 54.4 Ω, which makes 0.95 nV/$\sqrt{\text{Hz}}$ of Johnson noise spectral density. Since there are two attenuators, the overall noise contribution of the ladder network is $\sqrt{2}$ times 0.95 nV/$\sqrt{\text{Hz}}$ or 1.34 nV/$\sqrt{\text{Hz}}$, a large fraction of the total DSX noise. The rest of the DSX circuit components contribute another 1.20 nV/$\sqrt{\text{Hz}}$, which together with the attenuator produces 1.8 nV/$\sqrt{\text{Hz}}$ of total DSX input referred noise.

AC Coupling

As already mentioned, the DSX portion of the AD604 is a single-supply circuit and therefore its inputs need to be ac-coupled to accommodate ground based signals. External Capacitors C1 and C2 in Figure 35 level shift the ground referenced preamplifier output from ground to the dc value established by VOCM (nominal 2.5 V). C1 and C2, together with the 175 Ω looking into each of the DSX inputs (+DSX and –DSX), act as high-pass filters with corner frequencies depending on the values chosen for C1 and C2. For example, if C1 and C2 are 0.1 μF, then together with the 175 Ω input resistance seen into each side of the differential ladder of the DSX, a –3 dB high-pass corner at 9.1 kHz is formed.

If the AD604 output needs to be ground referenced, another ac coupling capacitor is required for level shifting. This capacitor also eliminates any dc offsets contributed by the DSX. With a nominal load of 500 Ω and a 0.1 μF coupling capacitor, this adds a high-pass filter with –3 dB corner frequency at about 3.2 kHz.

The choice for all three of these coupling capacitors depends on the application. They should allow the signals of interest to pass unattenuated, while at the same time they can be used to limit the low frequency noise in the system.

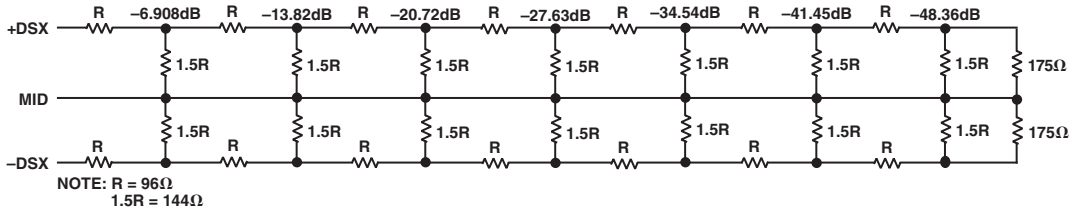


Figure 39. R–1.5R Dual Ladder Network.

Gain Control Interface

The gain-control interface provides an input resistance of approximately 2 MΩ at Pin VGN1 and gain scaling factors from 20 dB/V to 40 dB/V for VREF input voltages of 2.5 V to 1.25 V respectively. The gain scales linearly-in-dB for the center 40 dB of gain range, that is for VGN equal to 0.4 V to 2.4 V for the 20 dB/V scale and 0.2 V to 1.2 V for the 40 dB/V scale. Figure 40 shows the ideal gain curves for a nominal preamplifier gain of 14 dB, which are described by the following equations:

$$G\left(20\ \text{dB/V}\right) = 20 \times VGN - 5,\ VREF = 2.500\,\text{V} \quad (4)$$

$$G\left(20\ \text{dB/V}\right) = 30 \times VGN - 5,\ VREF = 1.666\,\text{V} \quad (5)$$

$$G\left(20\ \text{dB/V}\right) = 40 \times VGN - 5,\ VREF = 1.250\,\text{V} \quad (6)$$

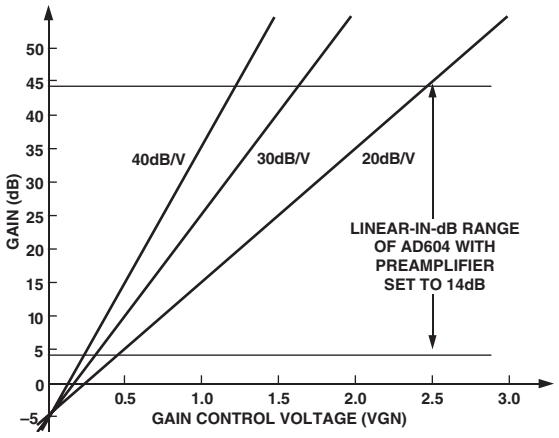


Figure 40. Ideal Gain Curves vs. VREF

From these equations, it can be seen that all gain curves intercept at the same –5 dB point; this intercept will be +6 dB higher (+1 dB) if the preamplifier gain is set to +20 dB or +14 dB, lower (–19 dB) if the preamplifier is not used at all. Outside of the central linear range, the gain starts to deviate from the ideal control law but still provides another 8.4 dB of range. For a given gain scaling, *VREF* can be calculated as shown in Equation 7:

$$VREF = \frac{2.500\,\text{V} \times 20\,\text{dB/V}}{Gain\ Scale} \quad (7)$$

Usable gain control voltage ranges are 0.1 V to 2.9 V for 20 dB/V scale and 0.1 V to 1.45 V for the 40 dB/V scale. VGN voltages of less than 0.1 V are not used for gain control since below 50 mV the channel (preamp and DSX) is powered down. This can be used to conserve power and at the same time gate off the signal. The supply current for a powered-down channel is 1.9 mA; the response time to power the device on or off is less than 1 µs.

Active Feedback Amplifier (Fixed Gain Amp)

To achieve single-supply operation and a fully differential input to the DSX, an active-feedback amplifier (AFA) is utilized. The AFA is basically an op amp with two g_m stages; one of the active stages is used in the feedback path (therefore the name), while the other is used as a differential input. Note that the differential input is an open-loop g_m stage that requires it to be highly linear over the expected input signal range. In this design, the g_m stage that senses the voltages on the attenuator is a distributed one; for example, there are as many g_m stages as there are taps on the ladder network. Only a few of them are on at any one time, depending on the gain-control voltage.

The AFA makes a differential input structure possible since one of its inputs (G1) is fully differential; this input is made up of a distributed g_m stage. The second input (G2) is used for feedback. The output of G1 will be some function of the voltages sensed on the attenuator taps which is applied to a high gain amplifier (A0). Because of negative feedback, the differential input to the high gain amplifier has to be zero; this in turn implies that the differential input voltage to G2 times g_{m2} (the transconductance of G2) has to be equal to the differential input voltage to G1 times g_{m1} (the transconductance of G1). Therefore, the overall gain function of the AFA is

$$\frac{V_{OUT}}{V_{ATTEN}} = \frac{g_{m1}}{g_{m2}} \times \frac{R1 + R2}{R2} \quad (8)$$

where V_{OUT} is the output voltage, V_{ATTEN} is the effective voltage sensed on the attenuator, $(R1+R2)/R2 = 42$, and $g_{m1}/g_{m2} = 1.25$; the overall gain is thus 52.5 (34.4 dB).

The AFA has additional features: (1) inverting the signal by switching the positive and negative input to the ladder network, (2) the possibility of using the DSX1 input as a second signal input, (3) fully differential high impedance inputs when both preamplifiers are used with one DSX (the other DSX could still be used alone), and (4) independent control of the DSX common-mode voltage. Under normal operating conditions, it is best to connect a decoupling capacitor to Pin VOCM in which case the common-mode voltage of the DSX is half the supply voltage; this allows for maximum signal swing. Nevertheless, the common-mode voltage can be shifted up or down by directly applying a voltage to VOCM. It can also be used as another signal input, the only limitation being the rather low slew rate of the VOCM buffer.

If the dc level of the output signal is not critical, another coupling capacitor is normally used at the output of the DSX; again this is done for level shifting and to eliminate any dc offsets contributed by the DSX (see the AC Coupling section).

APPLICATIONS

The most basic circuit in Figure 41 shows the connections for one channel of the AD604. The signal is applied at Pin 5. RGN is normally 0, in which case the preamplifier is set to a gain of 5 (14 dB). When Pin FBK1 is left open, the preamplifier is set to a gain of 10 (20 dB) and the gain range shifts up by 6 dB. The ac coupling capacitors before Pins –DSX1 and +DSX1 should be selected according to the required lower cutoff frequency. In this example, the 0.1 µF capacitors together with the 175 Ω seen looking into each of the DSX input pins provide a –3 dB high-pass corner of about 9.1 kHz. The upper cutoff frequency is determined by the bandwidth of the channel, which is 40 MHz. Note that the signal can be simply inverted by connecting the output of the preamplifier to Pin –DSX1 instead of +DSX1; this is due to the fully differential input of the DSX.

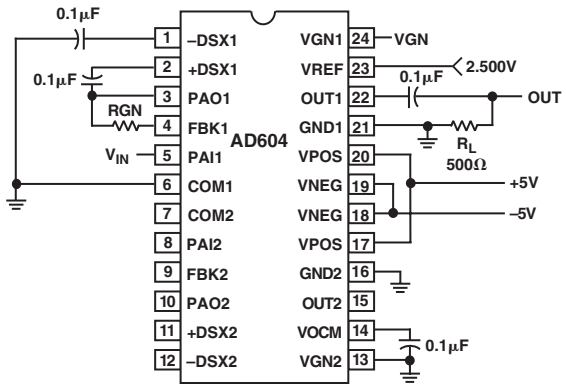


Figure 41. Basic Connections for a Single Channel

As shown here, the output is ac coupled for optimum performance. In the case of connecting to the AD9050, ac coupling can be eliminated as long as Pin VOCM is biased by the same 3.3 V common-mode voltage as the AD9050 (see Figure 50).

Pin VREF requires a voltage of 1.25 V to 2.5 V, with between 40 dB/V and 20 dB/V gain scaling, respectively. Voltage VGN controls the gain; its nominal operating range is from 0.25 V to 2.65 V for 20 dB/V gain scaling and 0.125 V to 1.325 V for 40 dB/V scaling. When this pin is taken to ground, the channel will power down and disable its output.

Pin COM1 is the main signal ground for the preamplifier and needs to be connected with as short a connection as possible to the input ground. Since the internal feedback resistors of the preamplifier are very small for noise reasons (8 Ω and 32 Ω nominally), it is of *utmost* importance to keep the resistance in this connection to a minimum. Furthermore, excessive inductance in this connection may lead to oscillations.

As a consequence of the AD604's ultralow noise and wide bandwidth, large dynamic currents flow to and from the power supply. To ensure the stability of the part, extreme attention to supply decoupling is required. A large storage capacitor in parallel with a smaller high frequency capacitor connected right at the supply pins, together with a ferrite bead coming from the supply should be used to ensure high frequency stability.

To provide for additional flexibility, Pin COM1 can be used to depower the preamplifier. When COM1 is connected to VP, the preamplifier is off, yet the DSX portion can be used independently. This may be of value when one desires to cascade the two DSX stages in the AD604. In this case, the first DSX output signal with respect to noise is large and using the second preamplifier at this point would waste power (see AGC amplifier application).

An Ultralow Noise AGC Amplifier with 82 dB to 96 dB Gain Range

Figure 42 shows an implementation of an AGC amplifier with 82 dB of gain range using a single AD604. First, the connections for the two channels of the AD604 are discussed; second, how the detector circuitry that closes the loop works is discussed.

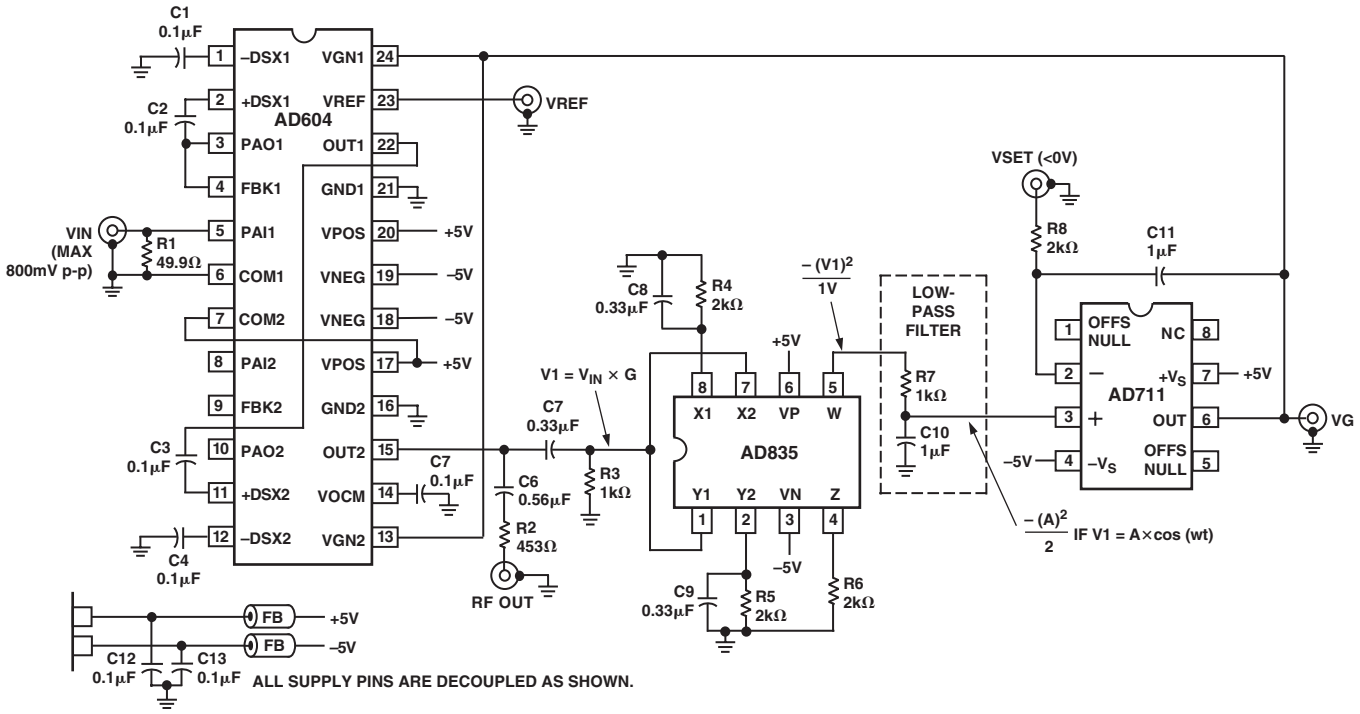


Figure 42. AGC Amplifier with 82 dB of Gain Range

The signal is applied to connector VIN, and since the signal source was 50 Ω, a terminating resistor (R1) of 50 Ω was added. The signal is then amplified by 14 dB (Pin FBK1 shorted to PAO1) through the Channel 1 preamplifier and is further processed by the Channel 1 DSX. Next the signal is applied directly to the Channel 2 DSX. The second preamplifier is powered down by connecting its COM2 pin to the positive supply as explained in the Preamplifier section. Capacitors C1 and C2 level shift the signal from the preamplifier into the first DSX and at the same time eliminate any offset contribution of the preamp. C3 and C4 have the same offset cancellation purpose for the second DSX. Each set of capacitors together with the 175 Ω input resistance of the corresponding DSX provides a high-pass filter with –3 dB corner frequency of about 9.1 kHz. Pin VOCM is decoupled to ground by a 0.1 μF capacitor, while VREF can be externally provided; in this application, the gain scale is set to 20 dB/V by applying 2.500 V. Since each of the DSX amplifiers operates from a single 5 V supply, the output is ac coupled via C6 and C7. The output signal can be monitored at the connector labeled RF OUT.

Figures 43 and 44 show the gain range and gain error for the AD604 connected as shown. The gain range is –14 dB to +82 dB; the useful range is 0 dB to +82 dB if the RF output amplitude is controlled to ±400 mV (+2 dBm). The main limitation on the lower end of the signal range is the input capability of the preamplifier. This can be overcome by adding an attenuator in front of the preamplifier, but that would defeat the advantage of the ultralow noise preamplifier. It should be noted that the second preamplifier is not used since its ultralow noise and the associated high power consumption are overkill after the first DSX stage. It is disabled in this application by connecting the COM2 pin to the positive supply. Nevertheless, the second preamplifier can be used if so desired, and the useful gain range will shift up by 14 dB to encompass 0 dB to 96 dB of gain. For the same +2 dBm output, this allows signals as small as –94 dBm to be measured.

To achieve the highest gains, the input signal has to ultimately be bandlimited to reduce the noise; this is especially true if the second preamplifier is used. If the maximum signal at Pin OUT2 of the AD604 is limited to ±400 mV (+2 dBm), the input signal level at the AGC threshold is +25 μV rms (–79 dBm). The circuit as shown has about 40 MHz of noise bandwidth; the 0.8 nV/$\sqrt{\text{Hz}}$ of input referred voltage noise spectral density of the AD604 results in an rms noise of 5.05 μV in the 40 MHz bandwidth. The 50 Ω termination resistor, together with the 50 Ω source resistance of the signal generator, combine to an effective resistance as seen by the input of the preamplifier of 25 Ω, which makes 4.07 μV of rms noise in 40 MHz. The noise floor of this channel is consequently the rms sum of these two main noise sources, 6.5 μV rms. This means that the minimum detectable signal (MDS) for this circuit is +6.5 μV rms (–90.7 dBm). As a general rule, the measured signal should be about a factor-of-three larger than the noise floor, in this case 19.5 μV rms. As we can see, the 25 μV rms signal that this AGC circuit can correct for is just slightly above the MDS. Of course, the sensitivity of the input can be improved by bandlimiting the signal; if the noise bandwidth is reduced by a factor-of-four to 10 MHz, the noise floor of the AGC circuit with a 50 Ω termination resistor will drop to +3.25 μV rms (–96.7 dBm). Further noise improvement can be achieved by an input matching network or by transformer coupling of the input signal.

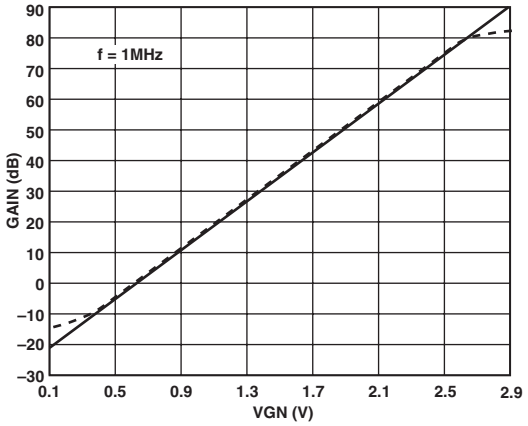


Figure 43. AD604 Cascaded Gain vs. VGN

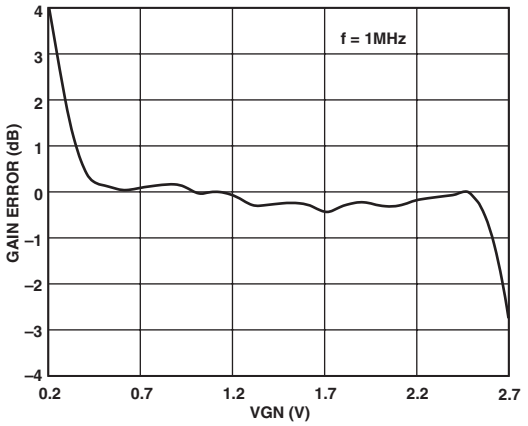


Figure 44. AD604 Cascaded Gain Error vs. VGN

The descriptions of the detector circuitry functions, comprised of a squarer, a low-pass filter, and an integrator, will follow. At this point, it is necessary to make some assumptions about the input signal. The following explanation of the detector circuitry presumes an amplitude modulated RF carrier where the modulating signal is at a much lower frequency than the RF signal. The AD835 multiplier functions as the detector by squaring the output signal presented to it by the AD604. A low-pass filter following the squaring operation removes the RF signal component at twice the incoming signal frequency, while passing the low frequency AM information. The following integrator with a time constant of 2 ms set by R8 and C11 integrates the error signal presented by the low-pass filter and changes VG until the error signal is equal to V_{SET}.

For example, if the signal presented to the detector is V1 = A×cos(wt) as indicated in Figure 42, the output of the squarer is $-(V1)^2/1$ V. The reason for all the minus signs in the detection circuitry comes from the necessity of providing negative feedback in the control loop; actually if V_{SET} becomes greater than 0 V, the control loop provides positive feedback. Squaring A×cos(wt) results in two terms, one at dc and one at 2w; the following low-pass filter passes only the $-(A)^2/2$ dc term. This dc voltage is now forced equal to the voltage, V_{SET}, by the control loop. The squarer, together with the low-pass filter, functions as a mean-square detector. As should be evident by controlling the value of V_{SET}, we can set the amplitude of the voltage V1 at the input of the AD835; if V_{SET} equals –80 mV, the AGC output signal amplitude will be ±400 mV.

Figure 45 shows the control voltage, VGN, versus the input power at frequencies of 1 MHz (solid line) and 10 MHz (dashed line) at an output regulated level of 2 dBm (800 mV p-p). The AGC threshold is evident at a P_{IN} of about –79 dBm; the highest input power that could still be accommodated was about +3 dBm. At this level, the output starts being distorted because of clipping in the preamplifier.

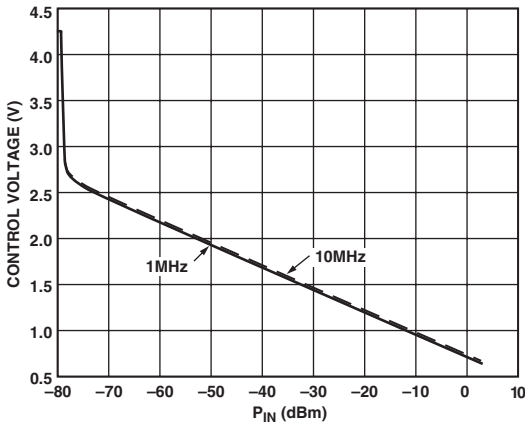


Figure 45. Control Voltage vs. Input Power of Circuit in Figure 42

As mentioned already, the second preamplifier can be used to extend the range of the AGC circuit in Figure 42. Figure 46 shows the modifications that need to be made to Figure 44 to achieve 96 dB of gain and dynamic range. Because of the extremely high gain, the bandwidth needs to be limited to reject some of the noise; furthermore, limiting the bandwidth will help suppress high frequency oscillations. The added components act as a low-pass filter and dc block (C5 level shifts the output of the first DSX from 2.5 V to ground); the ferrite bead has an impedance of about 5 Ω at 1 MHz, 30 Ω at 10 MHz, and 70 Ω at 100 MHz. Together with R2 and C6, the bead makes a low-pass filter that attenuates higher frequencies; at 1 MHz the attenuation is about –0.2 dB, while at 10 MHz it increases to –6 dB, on to –28 dB at 100 MHz. Signals now have to be less than about 1 MHz to not be significantly affected by the added circuitry. Figure 47 shows the control voltage versus the input power at 1 MHz to the circuit in Figure 46; note that the AGC threshold is at –95 dBm. The output signal level was set to 800 mV p-p by applying –80 mV to the V_{SET} connector.

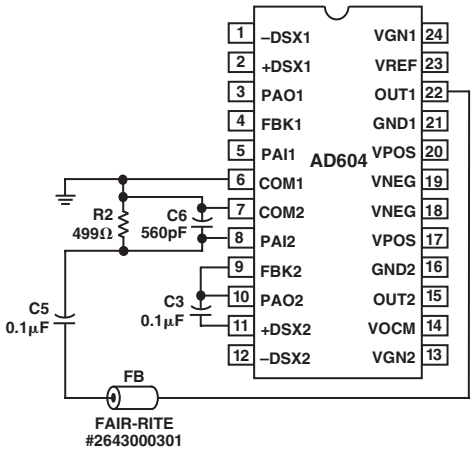


Figure 46. Modifications of AGC Amplifier to Create 96 dB of Gain Range

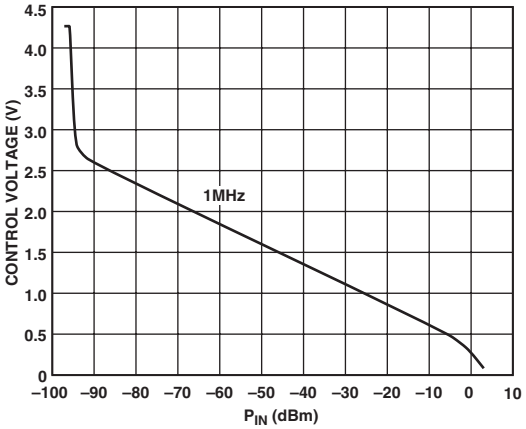


Figure 47. Control Voltage vs. Input Power of Circuit in Figure 46

Ultralow Noise, Differential Input-Differential Output VGA

Figure 48 shows how to use both preamplifiers and DSXs to create a high impedance, differential input-differential output variable gain amplifier. This application takes advantage of the differential inputs to the DSXs. It should be pointed out that the input is not *truly* differential, in the sense that the common-mode voltage needs to be at ground to achieve maximum input signal swing. This has mainly to do with the limited output swing capability of the output drivers of the preamplifiers; they clip around ±2.2 V due to having to drive an effective load of about 30 Ω. If a different input common-mode voltage needs to be accommodated, ac coupling (as was done in Figure 46) is recommended. The differential gain range of this circuit runs from 6 dB to 54 dB. This is 6 dB higher than each individual channel of the AD604 because the DSX inputs now see twice the signal amplitude compared to when they are driven single ended.

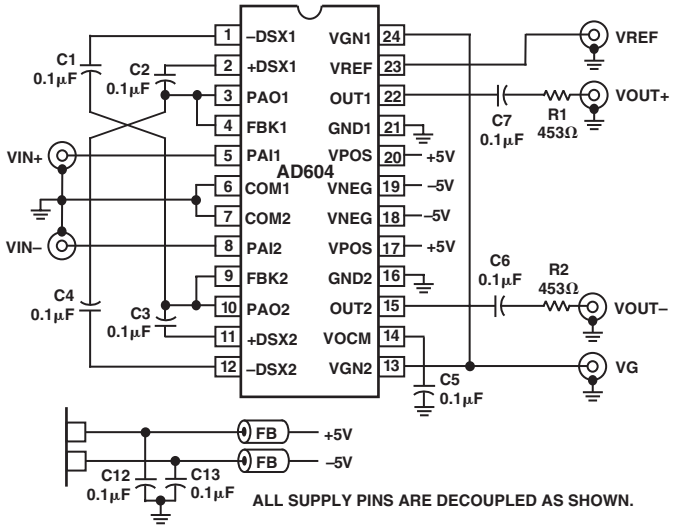


Figure 48. Ultralow Noise, Differential Input–Differential Output VGA

Figure 49 displays the output signals VOUT+ and VOUT– after a –20 dB attenuator formed between the 453 Ω resistors shown in Figure 48 and the 50 Ω loads presented by the oscilloscope plug-in. R1 and R2 were inserted to ensure a nominal load of 500 Ω at each output. The differential gain of the circuit was set to 20 dB by applying a control voltage, VGN, of 1 V; the gain scaling was 20 dB/V for a VREF of 2.500 V; the input frequency was 10 MHz and the differential input amplitude 100 mV p-p. The resulting differential output amplitude was 1 V p-p as can be seen on the scope photo when reading the vertical scale as 200 mV/div.

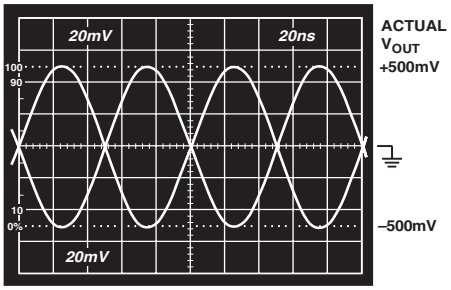


Figure 49. Output of VGA in Figure 48 for V_G = 1 V

Medical Ultrasound TGC Driving the AD9050, a 10-Bit, 40 MSPS ADC

The AD604 is an ideal candidate for the time gain control (TGC) amplifier that is required in medical ultrasound systems to limit the dynamic range of the signal that is presented to the ADC. Figure 50 shows a schematic of an AD604 driving an AD9050 in a typical medical ultrasound application.

The gain is controlled by means of a digital byte that is input to an AD7226 DAC that outputs the analog gain control signal. The output common-mode voltage of the AD604 is set to VPOS/2 by means of an internal voltage divider. The VOCM pin is bypassed with a 0.1 μF capacitor to ground.

The DSX output is optionally filtered and then buffered by an AD9631 op amp, a low distortion, low noise amplifier. The op amp output is ac-coupled into the self-biasing input of an AD9050 ADC that is capable of outputting 10 bits at a 40 MSPS sampling rate.

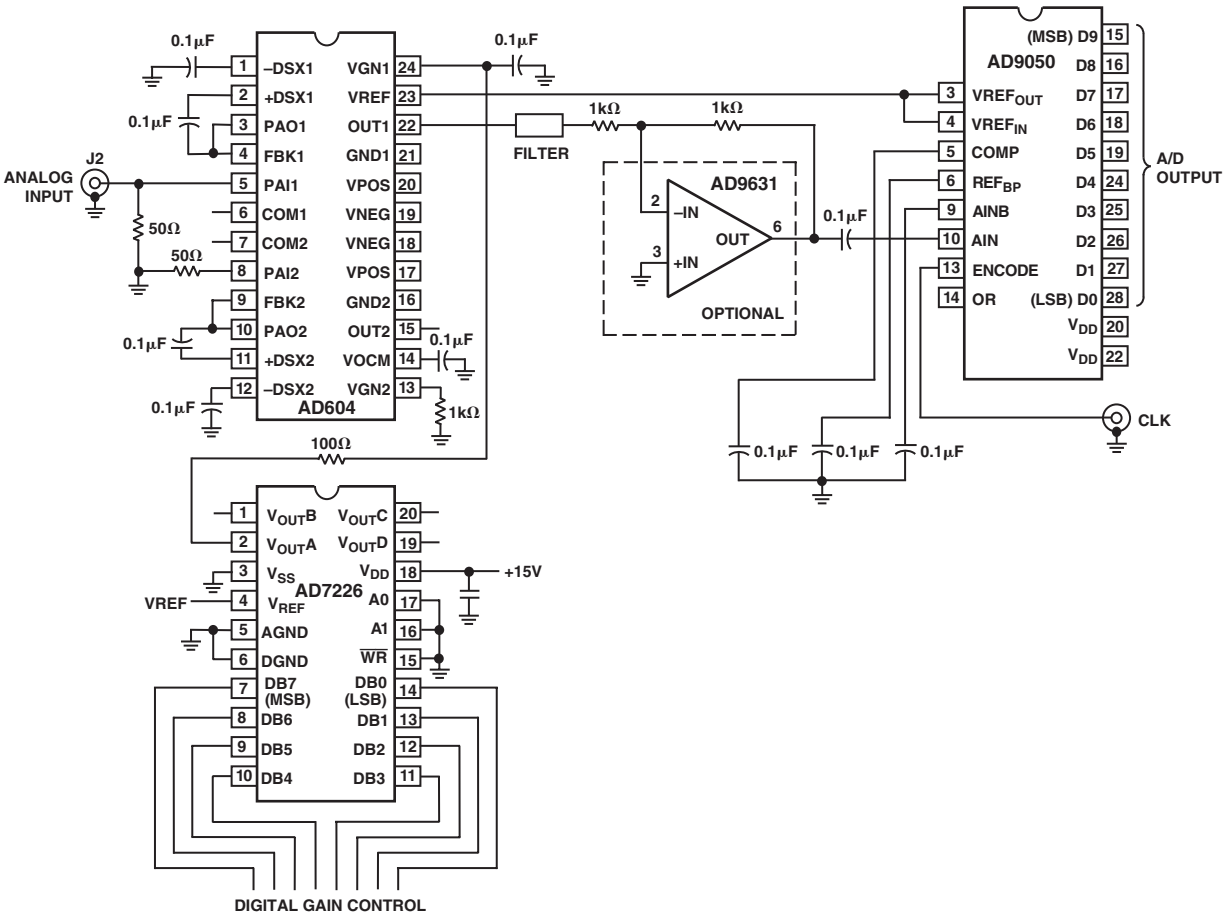


Figure 50. TGC Circuit for Medical Ultrasound Application

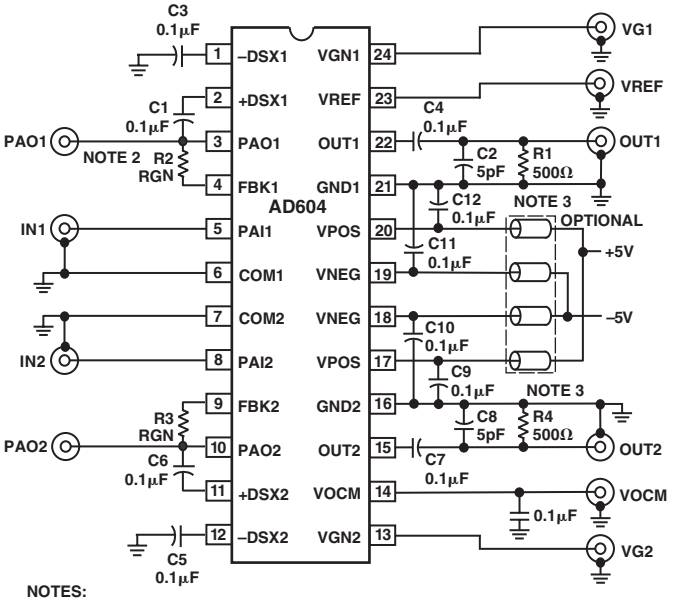


Figure 51. Basic Test Board

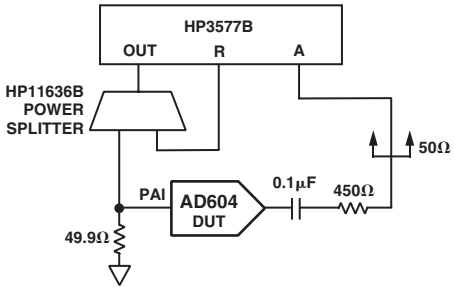
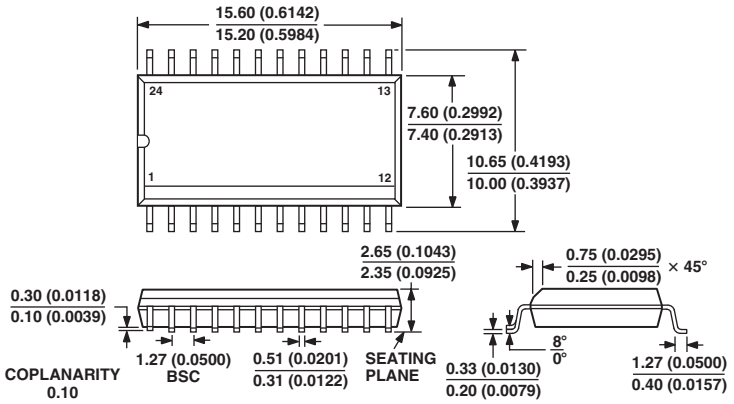


Figure 52. Setup for Gain Measurements

OUTLINE DIMENSIONS

24-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-24)

Dimensions shown in millimeters and (inches)

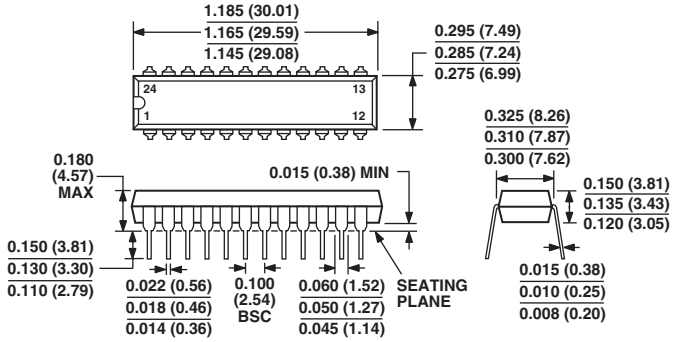


COMPLIANT TO JEDEC STANDARDS MS-013AD

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

24-Lead Plastic Dual In-Line Package [PDIP]
(N-24)

Dimensions shown in inches and (millimeters)

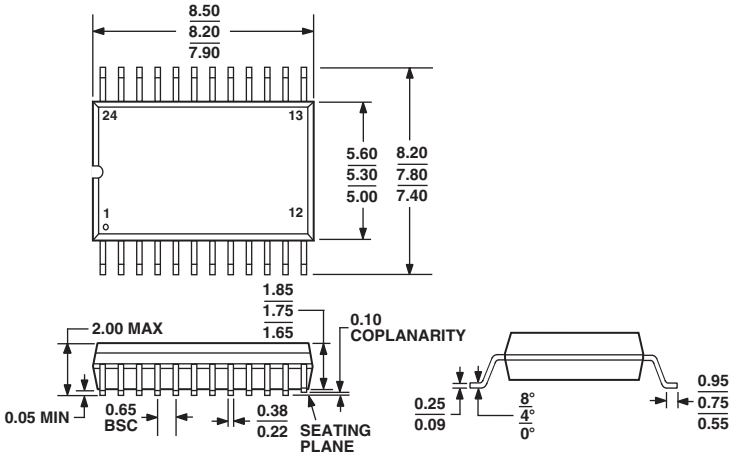


COMPLIANT TO JEDEC STANDARDS MO-095AG

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

24-Lead Shrink Small Outline Package [SSOP]
(RS-24)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-150AG

Revision History

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C00540–0–1/04(A)