

74ABT16245B

16-bit bus transceiver; 3-state

Rev. 4 — 19 August 2014

Product data sheet

1. General description

The 74ABT16245B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16245B device is a dual octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two output enable (1OE, 2OE) inputs for easy cascading and two direction (1DIR, 2DIR) inputs for direction control.

2. Features and benefits

- 16-bit bidirectional bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- Output capability: +64 mA / -32 mA
- Live insertion/extraction permitted
- Latch-up performance: JESD 78 Class II
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ CDM JESD22-C101C exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16245BDL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ABT16245BDGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1



4. Functional diagram

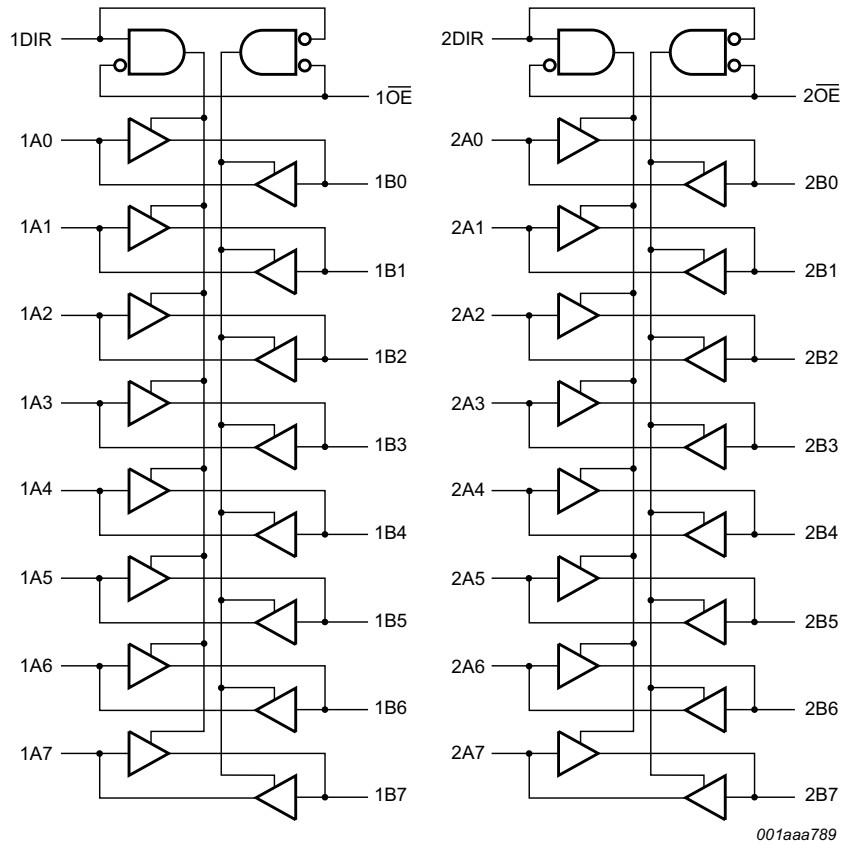


Fig 1. Logic symbol

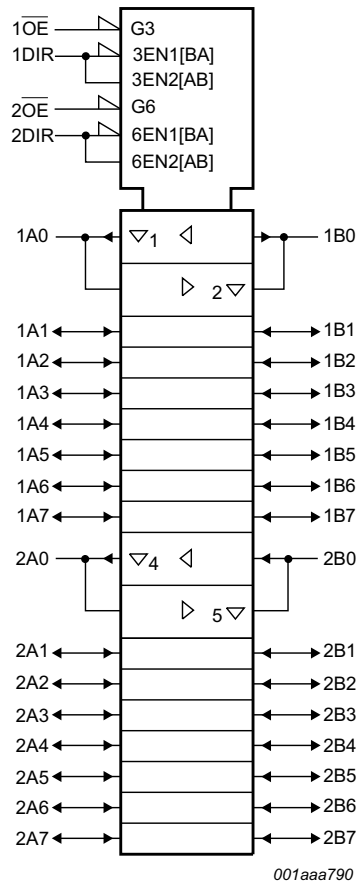


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

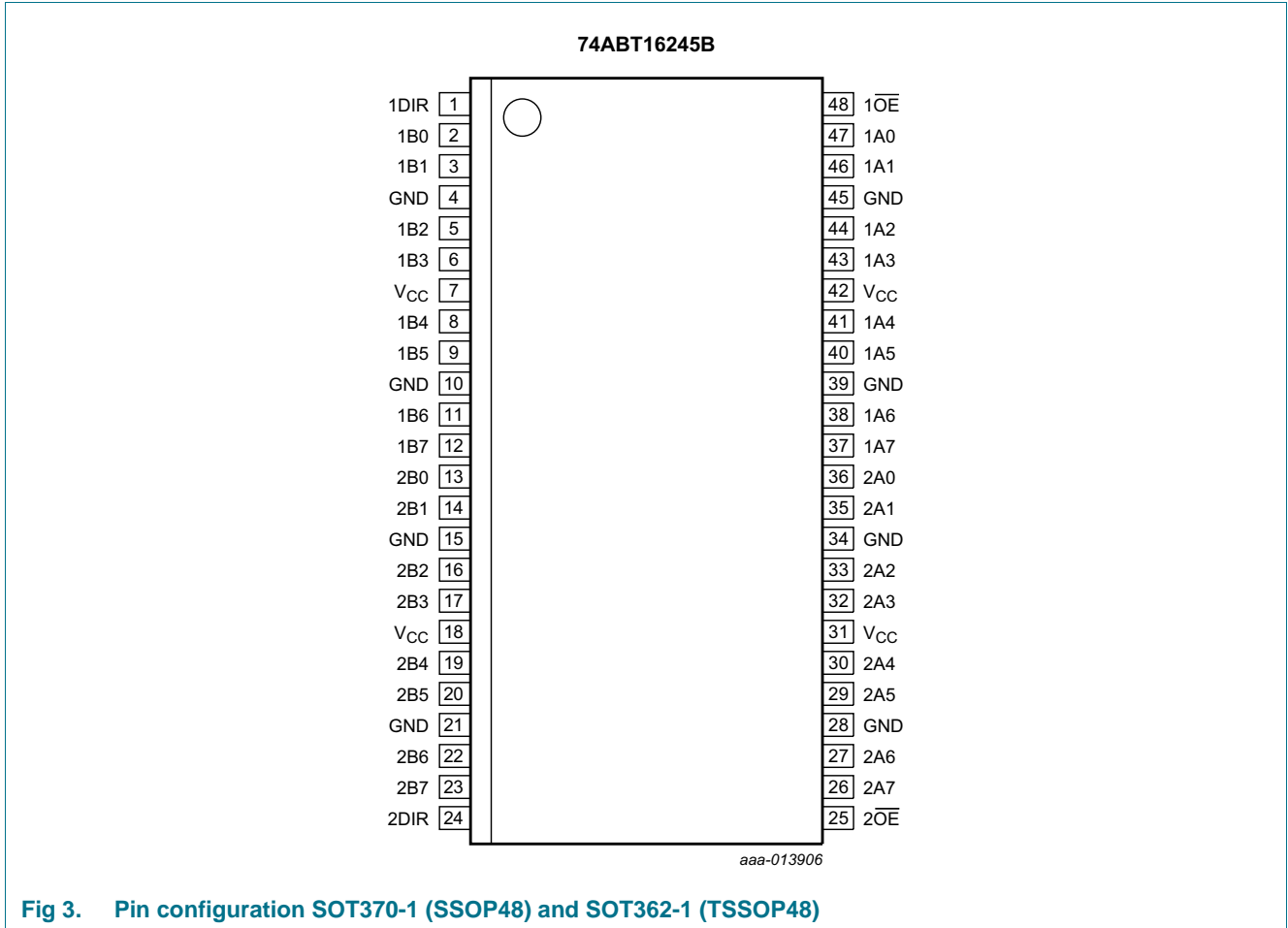


Fig 3. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
1OE, 2OE	48, 25	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

6. Functional description

Table 3. Function table^[1]

Inputs		Outputs	
nOE	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		^[1] -1.2	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	^[1] -0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _j	junction temperature		^[2] -	150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		4.5	5.5	V
V _I	input voltage		0	V _{CC}	V
V _{IH}	HIGH-level input voltage		2.0	-	V
V _{IL}	LOW-level input voltage		-	0.8	V
I _{OH}	HIGH-level output current		-32	-	mA
I _{OL}	LOW-level output current		-	64	mA
Δt/ΔV	input transition rise and fall rate		-	10	ns/V
T _{amb}	ambient temperature	in free air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-1.2	-0.9	-	-1.2	-	V
V _{OH}	HIGH-level output voltage	V _I = V _{IL} or V _{IH}						
		V _{CC} = 4.5 V; I _{OH} = -3 mA	2.5	2.9	-	2.5	-	V
		V _{CC} = 5.0 V; I _{OH} = -3 mA	3.0	3.4	-	3.0	-	V
		V _{CC} = 4.5 V; I _{OH} = -32 mA	2.0	2.4	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}	-	0.42	0.55	-	0.55	V
I _I	input leakage current	control pins; V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	±0.01	±1.0	-	±1.0	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O ≤ 4.5 V	-	±5.0	±100	-	±100	µA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} = 2.0 V; V _O = 0.5 V; V _I = GND or V _{CC} ; nOE = HIGH [1]	-	±5.0	±50	-	±50	µA
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V; V _I = V _{IL} or V _{IH}						
		output HIGH-state at V _O = 5.5 V	-	0.1	10	-	10	µA
		output LOW-state at V _O = 0 V	-	-0.1	-10	-	-10	µA
I _{LO}	output leakage current	HIGH-state; V _O = 5.5 V; V _{CC} = 5.5 V; V _I = GND or V _{CC}	-	5.0	50	-	50	µA
I _O	output current	V _{CC} = 5.5 V; V _O = 2.5 V [2]	-50	-92	-180	-50	-180	mA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = GND or V _{CC}						
		outputs HIGH-state	-	0.30	0.7	-	0.7	mA
		outputs LOW-state	-	10	19	-	19	mA
		outputs 3-state	-	0.30	0.7	-	0.7	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 5.5 V [3][4]						
		outputs enabled; one data input at 3.4 V and other inputs at V _{CC} or GND	-	400	700	-	700	µA
		outputs disabled; one data input at 3.4 V and other inputs at V _{CC} or GND	-	100	250	-	250	µA
		control pins; outputs disabled; one enable input at 3.4 V and other inputs at V _{CC} or GND	-	400	700	-	700	µA
C _I	input capacitance	V _I = 0 V or V _{CC}	-	4	-	-	-	pF
C _{I/O}	input/output capacitance	outputs disabled; V _O = 0 V or V _{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 µs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

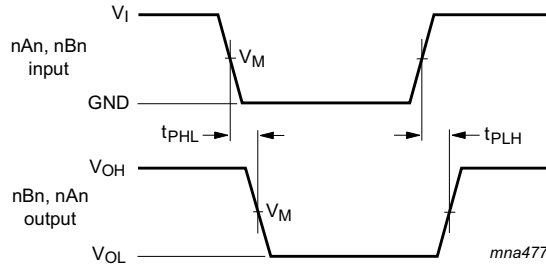
[4] This data sheet limit may vary among suppliers.

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V. For test circuit, see [Figure 6](#).

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			–40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	nAn to nBn; see Figure 4	1.0	2.0	3.2	1.0	3.5	ns
t _{PHL}	HIGH to LOW propagation delay	nAn to nBn; see Figure 4	1.0	2.3	3.5	1.0	4.0	ns
t _{PZH}	OFF-state to HIGH propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 5	1.0	3.0	4.4	1.0	5.1	ns
t _{PZL}	OFF-state to LOW propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 5	1.7	4.0	5.2	1.7	6.1	ns
t _{PHZ}	HIGH to OFF-state propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 5	1.7	3.5	4.9	1.7	5.4	ns
t _{PLZ}	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 5	1.5	3.2	4.4	1.5	5.0	ns

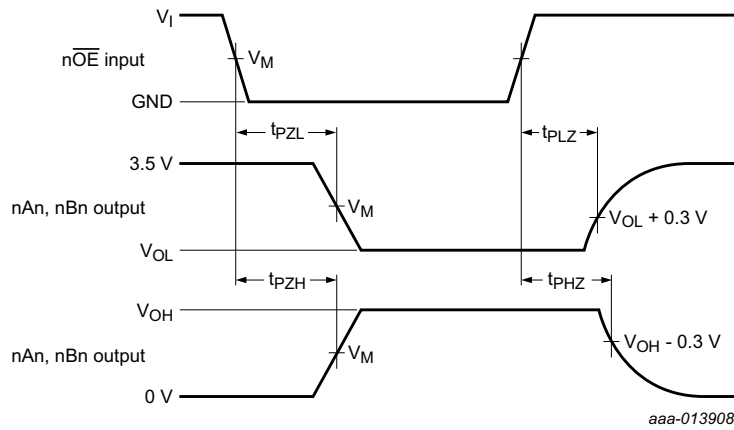
11. Waveforms



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 4. Input (nAn) to output (nBn) propagation delay times

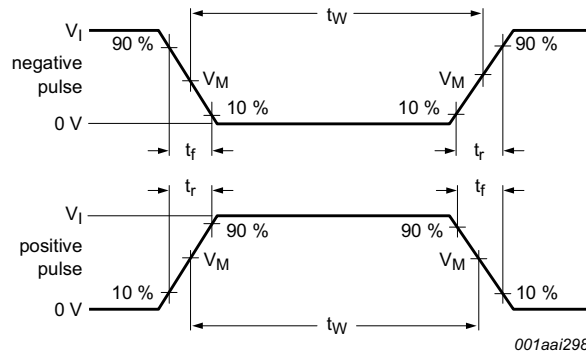


$V_M = 1.5\text{ V}$

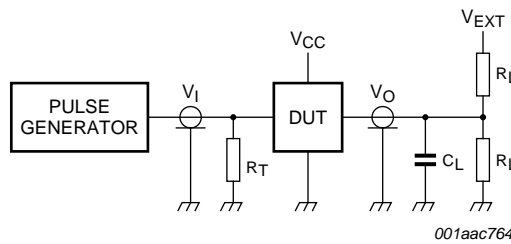
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. 3-state output enable and disable times

12. Test information



$V_M = 1.5\text{ V}$
 a. Input pulse definition



Test data is given in [Table 8](#).
 Definitions test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 b. Test circuit for 3-state outputs

Fig 6. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

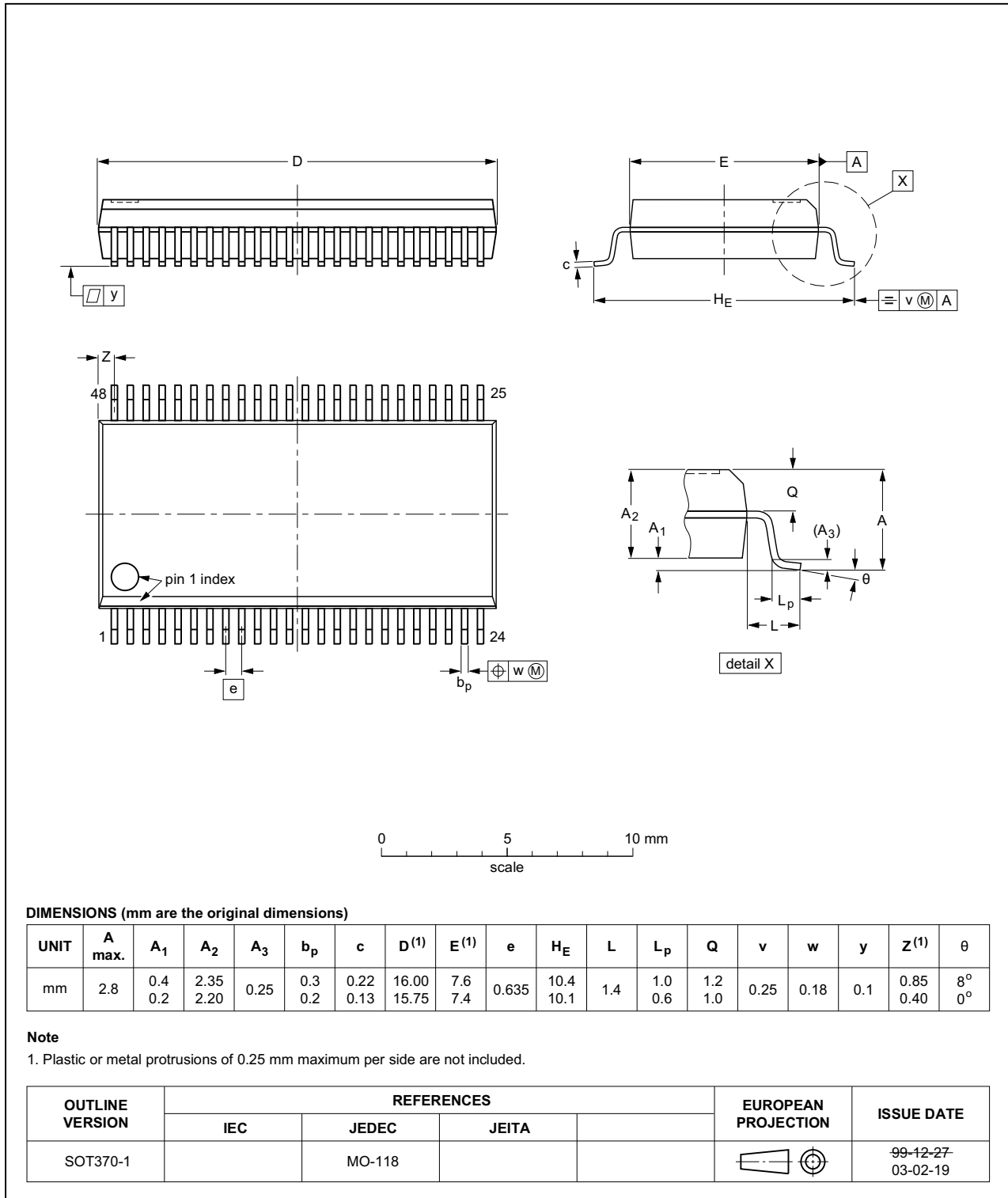


Fig 7. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

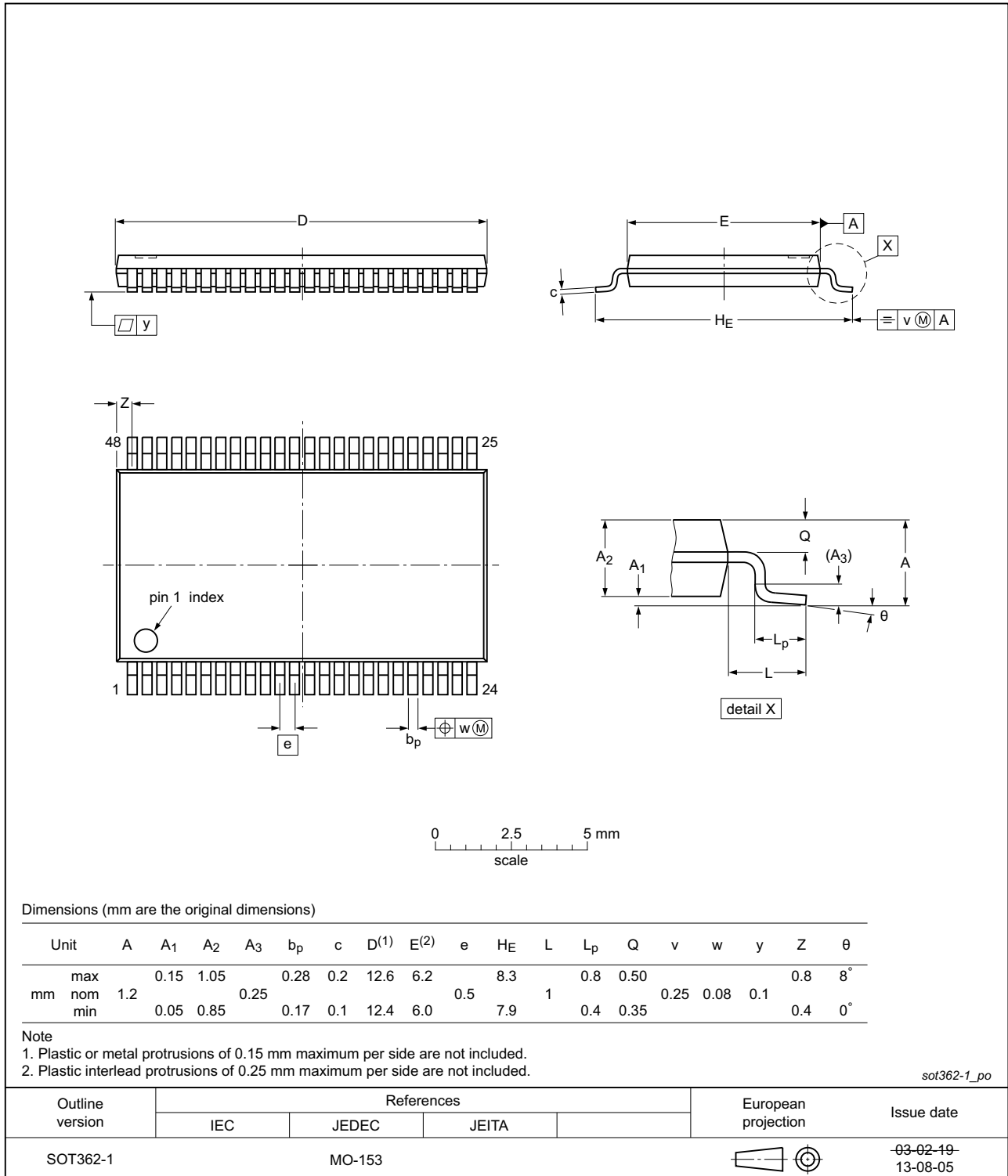


Fig 8. Package outline SOT362-1 (TSSOP48)

14. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16245B v.4	20140819	Product data sheet	-	74ABT_H16245B v.3
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Type number 74ABTH16245BDL removed.			
74ABT_H16245B v.3	20021213	Product data sheet	-	74ABT_H16245B v.2
74ABT_H16245B v.2	19980225	Product data sheet	-	74ABT_H16245B v.1
74ABT_H16245B v.1	19961120	Product data sheet	-	-

15. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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