

## 64-BIT AC-PDP DRIVER

The  $\mu$ PD16337 is a high-voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 64-bit bi-directional shift register (16 bit  $\times$  4 circuits), 64-bit latch and high-voltage CMOS driver. The logic block is designed to operate at 5-V power supply, enabling direct connection to a microcontroller. In addition, the  $\mu$ PD16337 achieves low power dissipation by employing CMOS structure while having a high withstand voltage output (150 V, 40 mA MAX.)

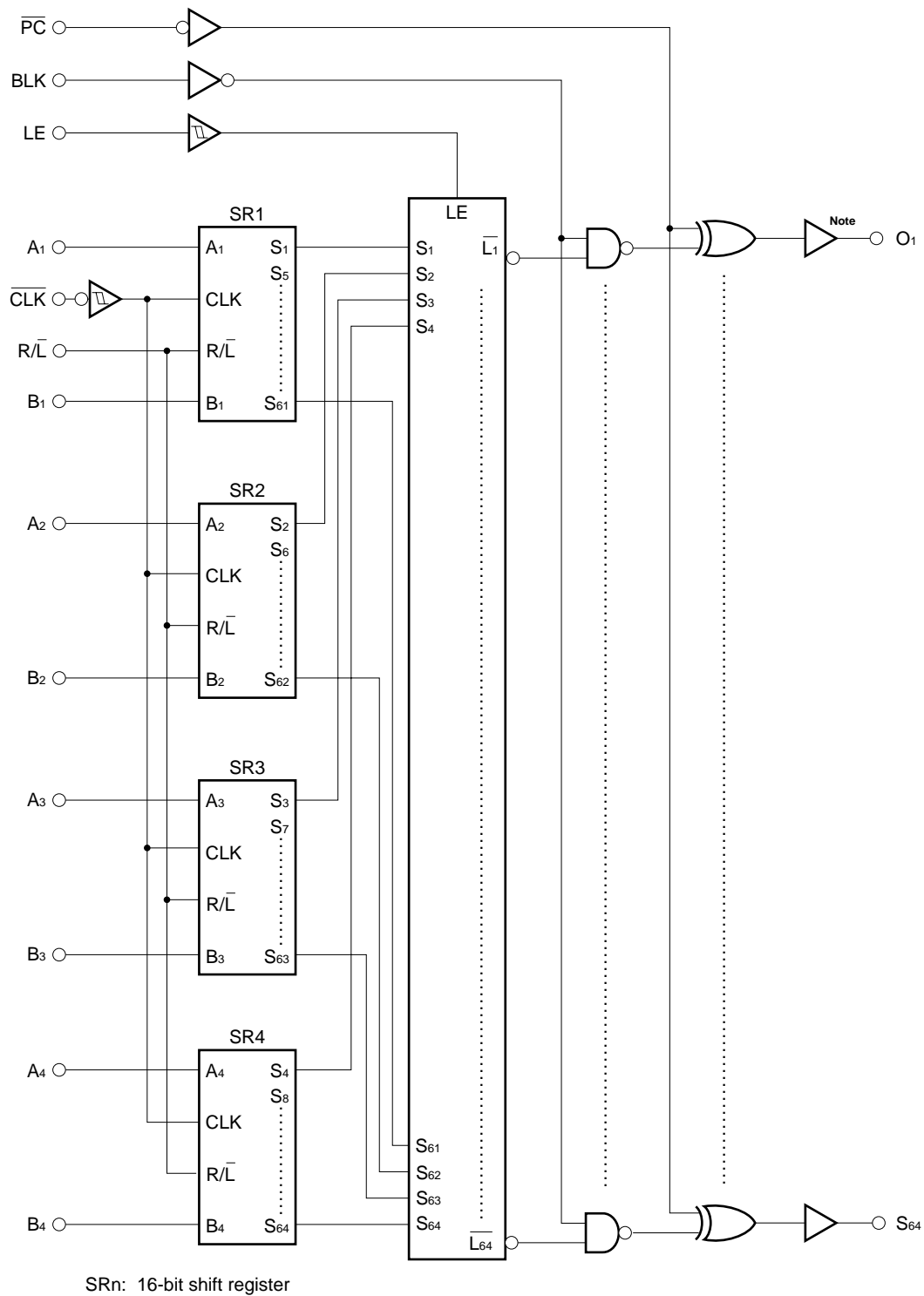
## FEATURES

- Built in four 16-bit bi-directional shift register circuits
- Data control with transfer clock (external) and latch
- High-speed data transfer ( $f_{\max.} = 20$  MHz MIN. at cascade connection)
- Wide operating temperature range ( $T_A = -40$  to  $+85^\circ\text{C}$ )
- High withstand output voltage (150 V, 40 mA MAX.)
- 5-V CMOS input interface
- High withstand voltage CMOS structure
- Capable of reversing all driver outputs by PC pin

## ORDERING INFORMATION

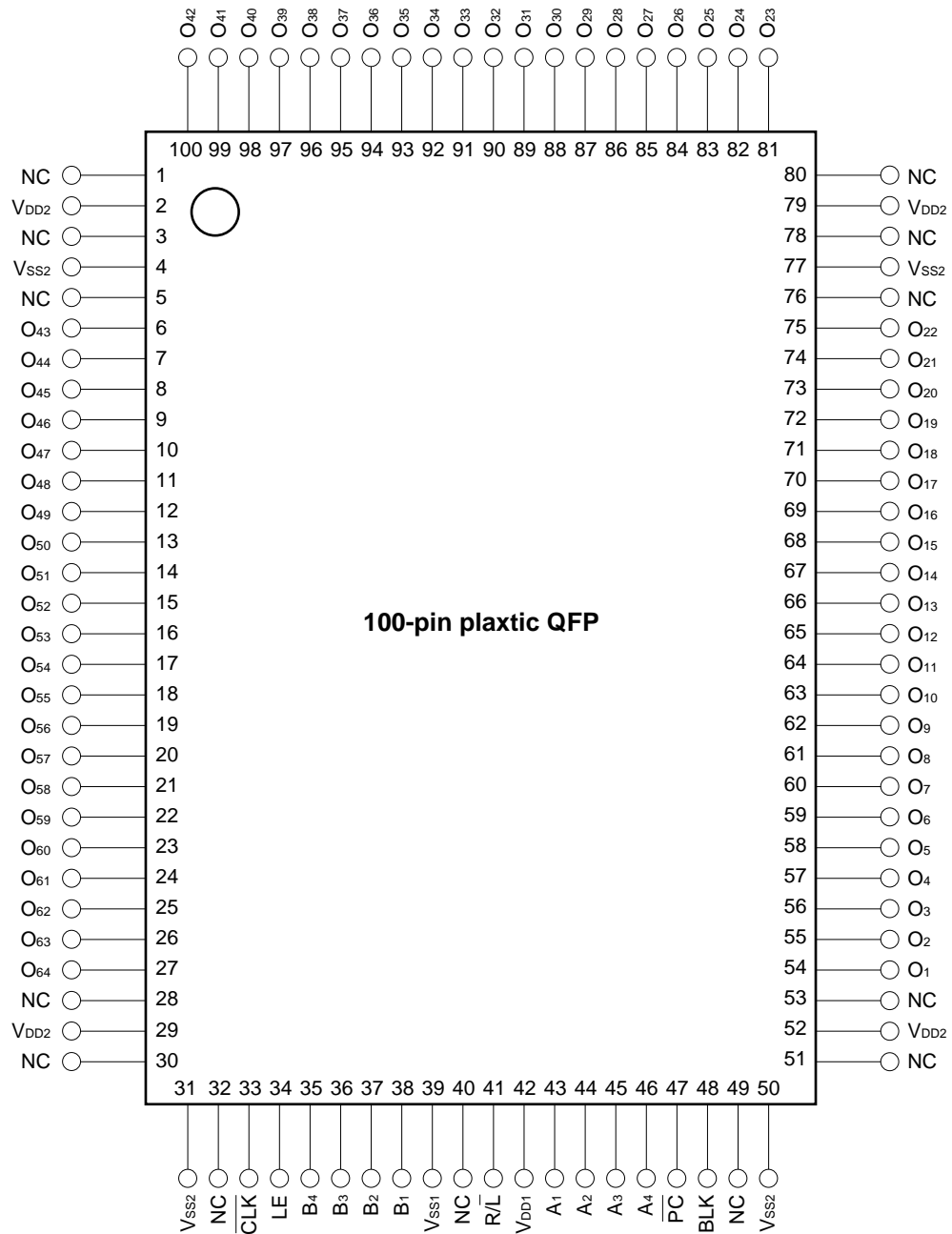
Part Number	Package
$\mu$ PD16337GF-3BA	100-pin plastic QFP

BLOCK DIAGRAM



**Note** High withstand voltage CMOS driver, 150 V, ±40 mA (MAX.)

PIN CONFIGURATION (Top View)



- Cautions**
1. Pin 40 is connected to the lead frame, and therefore must be left open.
  2. Ensure that the V<sub>DD1</sub>, V<sub>DD2</sub>, V<sub>SS1</sub> and V<sub>SS2</sub> pins are all used, and that V<sub>SS1</sub> and V<sub>SS2</sub> are used at the same potential.
  3. To prevent latch up breakdown, the power should be turned on in the order V<sub>DD1</sub>, logic signal, V<sub>DD2</sub>. It should be turned off in the opposite order.

PIN DESCRIPTION

Symbol	Pin Name	Pin Number	Description
$\overline{PC}$	Polarity change input	47	$\overline{PC} = L$ : All driver output invert
BLK	Blank input	48	BLK = H: All output = H or L
LE	Latch enable input	34	Automatically executes latch by setting High at rising edge of the clock
A <sub>1</sub> to A <sub>4</sub>	RIGHT data input/output	43 to 46	When $\overline{R/L} = H$ , A <sub>1</sub> to A <sub>4</sub> : Input B <sub>1</sub> to B <sub>4</sub> : Output
B <sub>1</sub> to B <sub>4</sub>	LEFT data input/output	38 to 35	When $\overline{R/L} = L$ , A <sub>1</sub> to A <sub>4</sub> : Output B <sub>1</sub> to B <sub>4</sub> : Input
$\overline{CLK}$	Clock input	33	Shift executed on fall
$\overline{R/L}$	Shift control input	41	Right shift mode when R/L = H SR <sub>1</sub> : A <sub>1</sub> → S <sub>1</sub> ... S <sub>61</sub> → B <sub>1</sub> (Same direction for SR <sub>2</sub> -SR <sub>4</sub> ) Left shift mode when R/L = L SR <sub>1</sub> : B <sub>1</sub> → S <sub>61</sub> ... S <sub>1</sub> → A <sub>1</sub> (Same direction for SR <sub>2</sub> -SR <sub>4</sub> )
O <sub>1</sub> to O <sub>64</sub>	High withstand voltage output	54 to 75, 81 to 100, 6 to 27	130 V, 40 mA MAX.
V <sub>DD1</sub>	Power supply for logic block	42	5 V ±10%
V <sub>DD2</sub>	Power supply for driver block	2, 29, 52, 79	30 to 130 V
V <sub>SS1</sub>	Logic GND	39	Connect to system GND
V <sub>SS2</sub>	Driver GND	4, 31, 50, 77	Connect to system GND
NC	Non-connection	1, 3, 5, 28, 30, 32, 40, 49, 51, 53, 76, 78, 80	Non-connection Ensure that pin 40 is left open.

**TRUTH TABLE 1 (Shift Register Block)**

Input		Output		Shift Register
R/L	CLK	A	B	
H	↓	Input	Output <sup>Note 1</sup>	Right shift execution
H	H or L		Output	Hold
L	↓	Output <sup>Note 2</sup>	Input	Left shift execution
L	H or L	Output		Hold

- Notes**
1. The data of S<sub>57</sub>, S<sub>58</sub>, S<sub>59</sub>, S<sub>60</sub> shifts to S<sub>61</sub>, S<sub>62</sub>, S<sub>63</sub>, S<sub>64</sub> and is output from B<sub>1</sub>, B<sub>2</sub>, B<sub>3</sub>, B<sub>4</sub> at the falling edge of the clock, respectively.
  2. The data of S<sub>5</sub>, S<sub>6</sub>, S<sub>7</sub>, S<sub>8</sub> shifts to S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>, S<sub>4</sub> and is output from A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub>, A<sub>4</sub> at the falling edge of the clock, respectively.

**TRUTH TABLE 2 (Latch Block)**

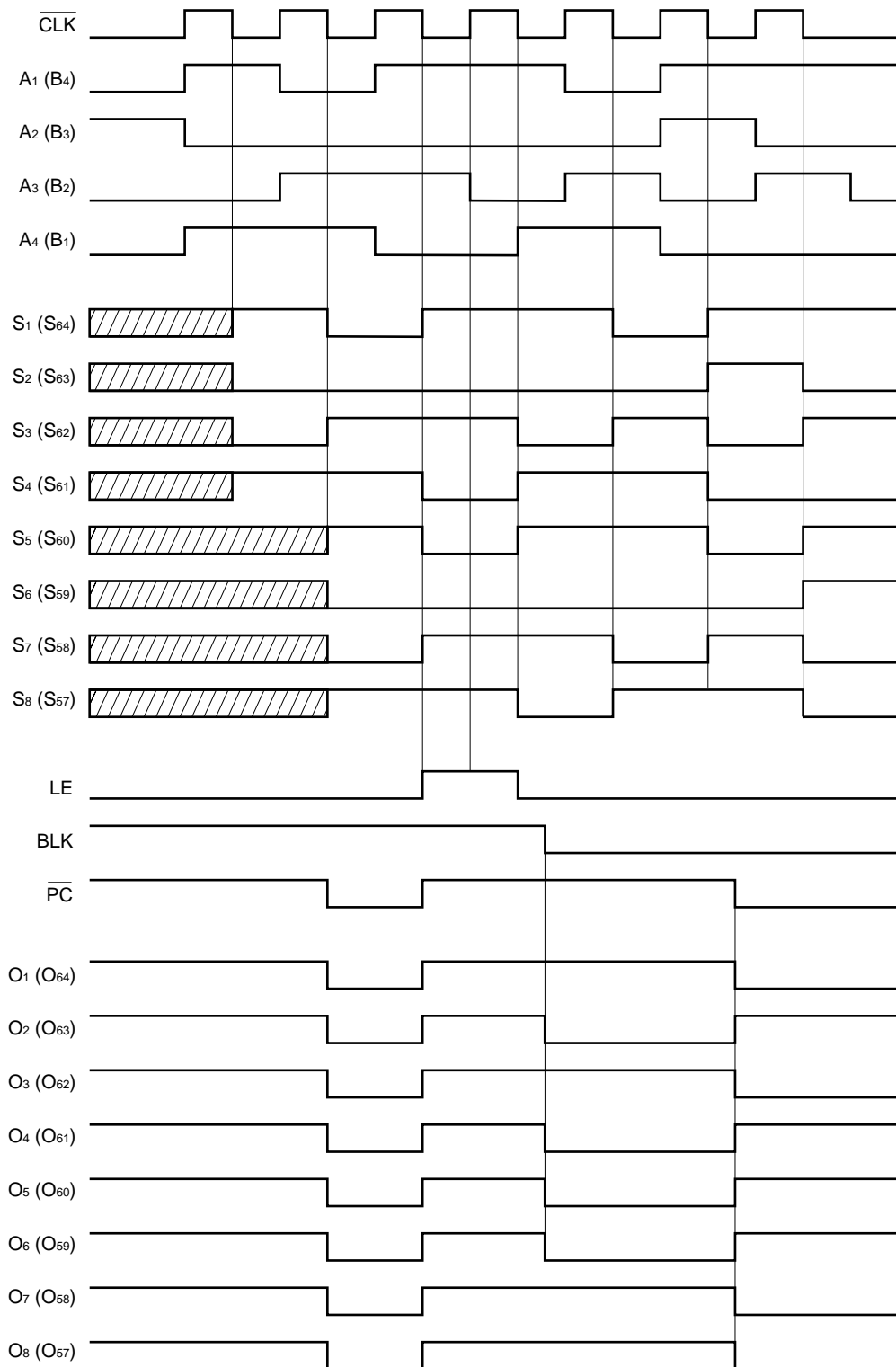
LE	CLK	Output State of Latch Block ( $\overline{L}_n$ )
H	↑	Latch S <sub>n</sub> data and hold output data
	↓	Hold latch data
L	×	Hold latch data

**TRUTH TABLE 3 (Driver Block)**

$\overline{L}_n$	BLK	$\overline{PC}$	Output State of Driver Block
×	H	H	H (All driver outputs: H)
×	H	L	L (All driver outputs: L)
×	L	H	Output latch data ( $\overline{L}_n$ )
×	L	L	Output reversed latch data ( $\overline{L}_n$ )

×: H or L, H: High level, L: Low level

**TIMING CHART (Right shift)**



**Remark** Values in parentheses in the above chart are when  $R/\bar{L} = L$ .

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Ratings	Unit
Logic Block Supply Voltage	V <sub>DD1</sub>	-0.5 to +7.0	V
Driver Block Supply Voltage	V <sub>DD2</sub>	-0.5 to +150	V
Logic Block Input Voltage	V <sub>I</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Block Output Current	I <sub>O2</sub>	40	mA
Input Current	I <sub>I</sub>	±25	mA
Power Dissipation	P <sub>D</sub>	1300 <sup>Note</sup>	mW
Operating Ambient Temperature	T <sub>A</sub>	-40 to +85	°C
Storage Temperature	T <sub>stg</sub>	-65 to +150	°C

**Note** Derate at -13 mW/°C at T<sub>A</sub> = 25°C or higher

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = -40 to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Block Supply Voltage	V <sub>DD1</sub>	4.5	5.0	5.5	V
Driver Block Supply Voltage	V <sub>DD2</sub>	30		130	V
High-Level Input Voltage	V <sub>IH</sub>	0.7 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-Level Input Voltage	V <sub>IL</sub>	0		0.2 V <sub>DD1</sub>	V
Driver Output Current	I <sub>OH2</sub>			-30	mA
	I <sub>OL2</sub>			+30	mA

**ELECTRICAL SPECIFICATIONS (T<sub>A</sub> = 25°C, V<sub>DD1</sub> = 5.0 V, V<sub>DD2</sub> = 130 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V <sub>OH1</sub>	Logic, I <sub>OH1</sub> = -1.0 mA	0.9 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-Level Output Voltage	V <sub>OL1</sub>	Logic, I <sub>OL1</sub> = 1.0 mA	0		0.1 V <sub>DD1</sub>	V
High-Level Output Voltage	V <sub>OH21</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OH2</sub> = -10 mA	123			V
	V <sub>OH22</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OH2</sub> = -30 mA	110			V
Low-Level Output Voltage	V <sub>OL21</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OL2</sub> = 10 mA			5.0	V
	V <sub>OL22</sub>	O <sub>1</sub> to O <sub>64</sub> , I <sub>OL2</sub> = 30 mA			15	V
Input Leakage Current	I <sub>IL</sub>	V <sub>1</sub> = V <sub>DD1</sub> or V <sub>SS1</sub>			±1.0	μA
High-Level Input Voltage	V <sub>IH</sub>		0.7 V <sub>DD1</sub>			V
Low-Level Input Voltage	V <sub>IL</sub>				0.2 V <sub>DD1</sub>	V
Static Current Dissipation	I <sub>DD1</sub>	Logic, T <sub>A</sub> = -40 to +85°C			100	μA
	I <sub>DD1</sub>	Logic, T <sub>A</sub> = 25°C			10	μA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = -40 to +85°C			1000	μA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = 25°C			100	μA

**SWITCHING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5.0\text{ V}$ ,  $V_{DD2} = 130\text{ V}$ ,  $V_{SS1} = V_{SS2} = 0\text{ V}$ , logic  $C_L = 15\text{ pF}$ , driver  $C_L = 50\text{ pF}$ ,  $t_r = t_f = 6.0\text{ ns}$ )

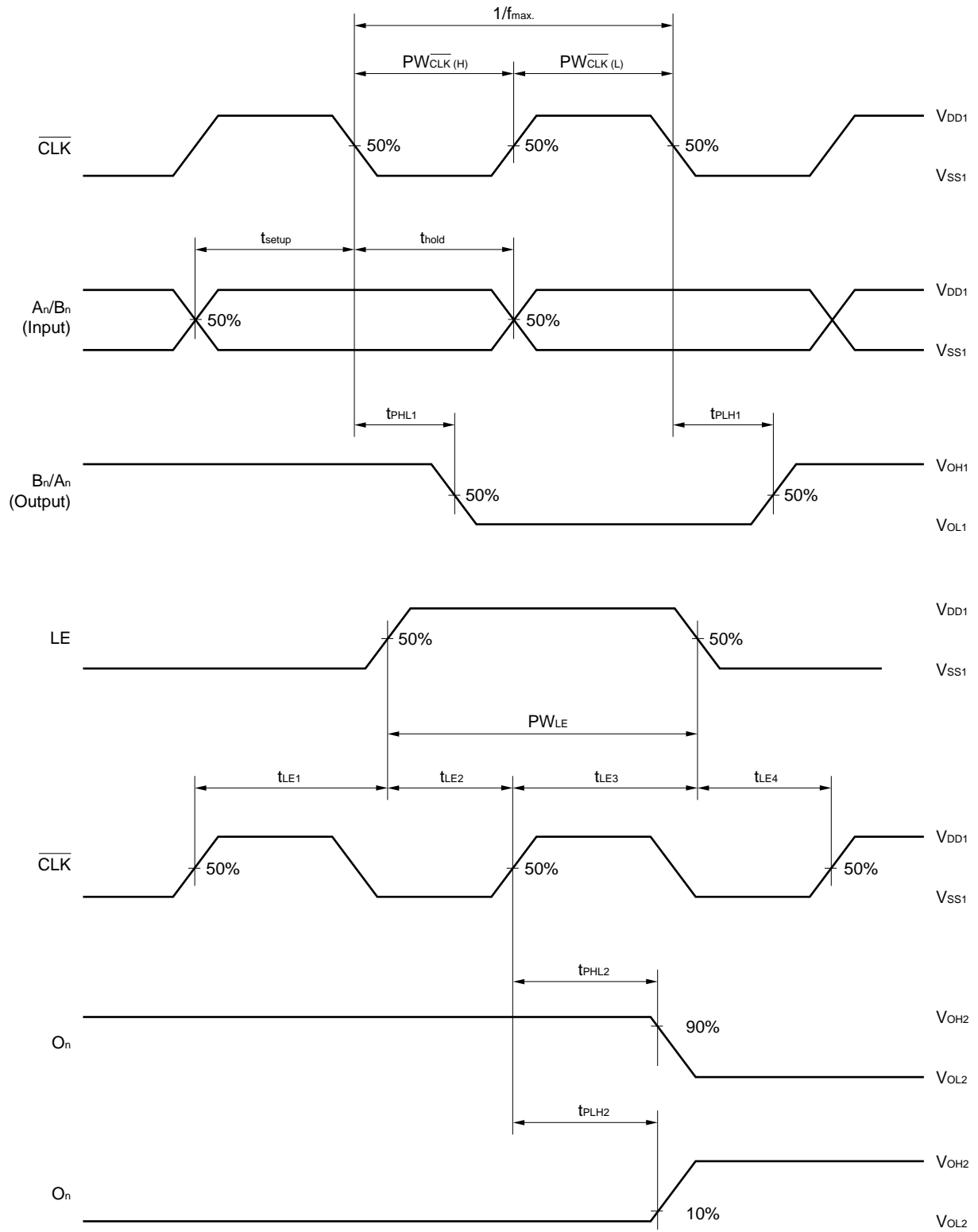
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transmission Delay Time	$t_{PHL1}$	$\overline{\text{CLK}} \downarrow \rightarrow \text{A/B}$			40	ns
	$t_{PLH1}$				40	ns
	$t_{PHL2}$	$\overline{\text{CLK}} \uparrow (\text{LE} = \text{H}) \rightarrow \text{O}_1 \text{ to } \text{O}_{64}$			180	ns
	$t_{PLH2}$				180	ns
	$t_{PHL3}$	$\text{BLK} \rightarrow \text{O}_1 \text{ to } \text{O}_{64}$			165	ns
	$t_{PLH3}$				165	ns
	$t_{PHL4}$	$\overline{\text{PC}} \rightarrow \text{O}_1 \text{ to } \text{O}_{64}$			160	ns
	$t_{PLH4}$				160	ns
Rise Time	$t_{TLH}$	$\text{O}_1 \text{ to } \text{O}_{64}$			200	ns
Fall Time	$t_{THL}$	$\text{O}_1 \text{ to } \text{O}_{64}$			200	ns
Maximum Clock Frequency	$f_{\text{max}}$	When data is read, duty 50% $T_A = -40 \text{ to } +85^\circ\text{C}$ $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$	25			MHz
		When a cascade connection is made with a duty of 50% $T_A = -40 \text{ to } +85^\circ\text{C}$ $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$	20			MHz
Input Capacitance	$C_i$				15	pF

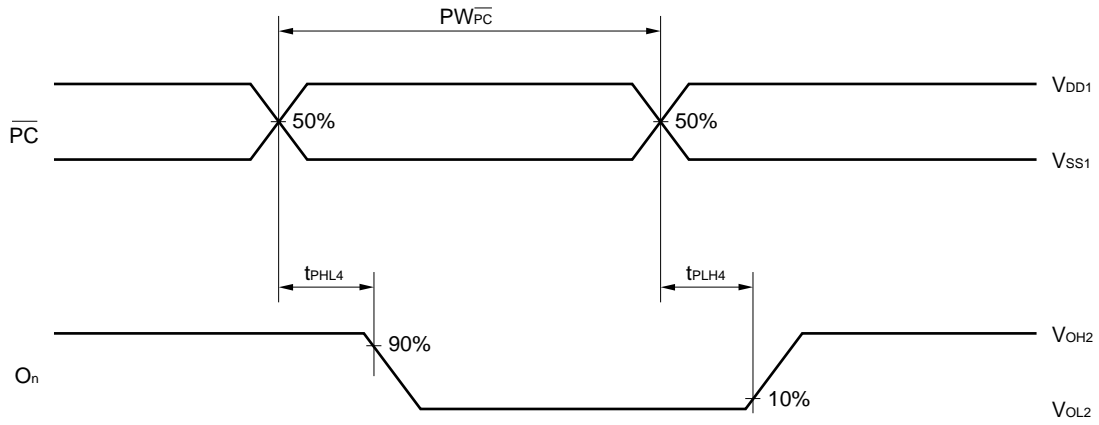
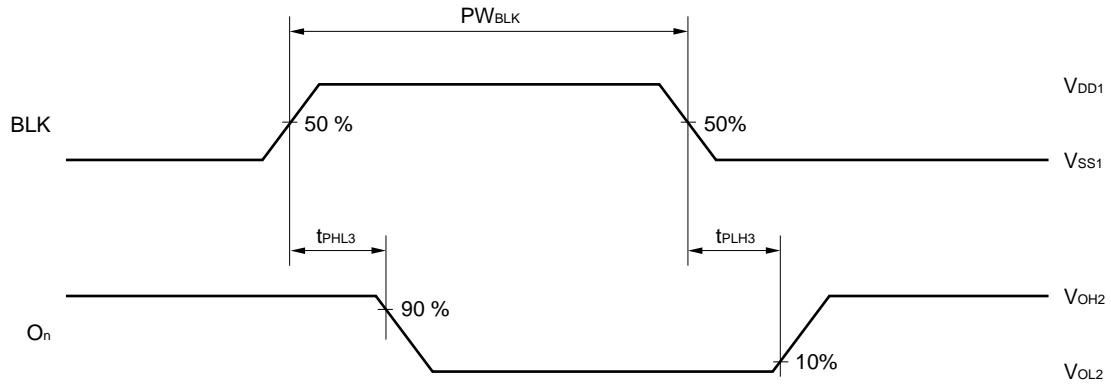
**TIMMING REQUIREMENT** ( $T_A = -40 \text{ to } +85^\circ\text{C}$ ,  $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$ ,  $V_{SS1} = V_{SS2} = 0\text{ V}$ ,  $t_r = t_f = 6.0\text{ ns}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	$PW_{\overline{\text{CLK}}}$		20			ns
Latch Enable Pulse Width	$PW_{\text{LE}}$		30			ns
Blank Pulse Width	$PW_{\text{BLK}}$		500			ns
$\overline{\text{PC}}$ Pulse Width	$PW_{\overline{\text{PC}}}$		500			ns
Data Setup Time	$t_{\text{setup}}$		10			ns
Data Hold Time	$t_{\text{hold}}$		10			ns
Latch Enable Time 1	$t_{\text{LE1}}$		20			ns
Latch Enable Time 2	$t_{\text{LE2}}$		10			ns
Latch Enable Time 3	$t_{\text{LE3}}$		20			ns
Latch Enable Time 4	$t_{\text{LE4}}$		10			ns



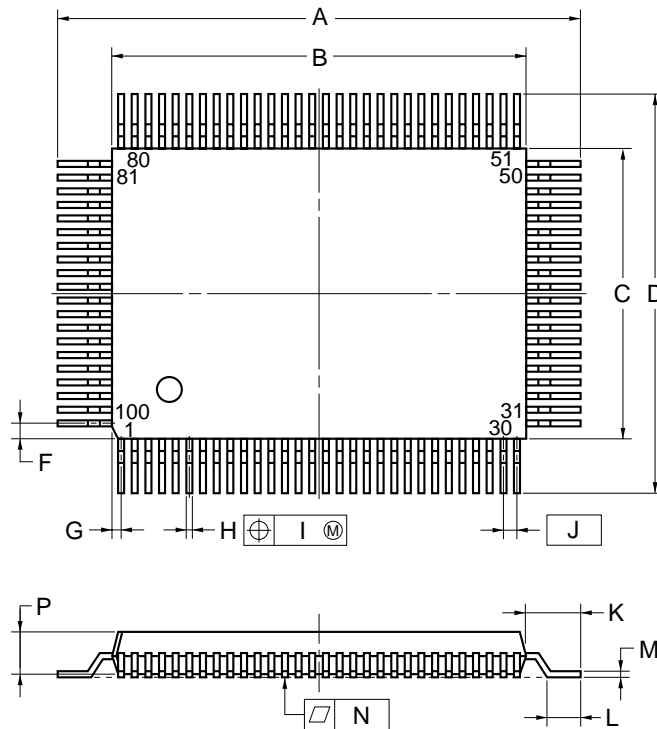
SWITCHING CHARACTERISTICS WAVEFORM



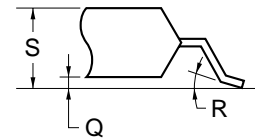


PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	0.913 <sup>+0.009</sup> <sub>-0.008</sub>
B	20.0±0.2	0.787 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S100GF-65-3BA-3

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the conditions recommended below.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

**SURFACE MOUNT TYPE**

For details of recommended soldering conditions, refer to the information document “Semiconductor Device Mounting Technology Manual” (C10535E).

**μPD16337GF-3BA**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. MAX. (at 210°C or above), Number of times: Twice, Time limit: None <sup>Note</sup>	IR30-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. MAX. (at 200°C or above), Number of times: Twice, Time limit: None <sup>Note</sup>	VP15-00-2
Pin partial heating	Pin partial temperature: 300°C MAX., Duration: 10 sec. MAX., Time limit: None <sup>Note</sup>	

**Note** For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

**Caution** Use of more than one soldering method should be avoided (except in the case of pin partial heating).

**REFERENCES**

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)  
Quality Grade on NEC Semiconductor Devices (C11531E)

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Anti-radioactive design is not implemented in this product.



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Datasheets for electronics components.