

## ISOx5 Isolated 3.3-V Half- and Full-Duplex RS-485 Transceivers

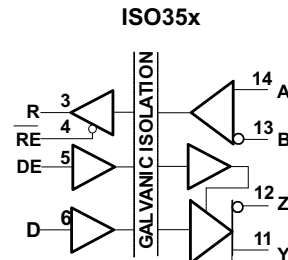
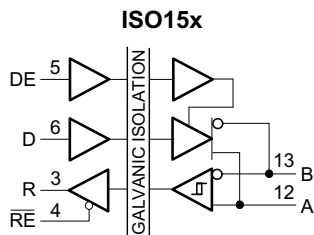
### 1 Features

- Meets or Exceeds TIA/EIA RS-485 Requirements
- 1/8 Unit Load – Up to 256 Nodes on a Bus
- Signaling Rates up to 1 Mbps
- Thermal Shutdown Protection
- Low Bus Capacitance – 16 pF (Typical)
- 50 kV/μs Typical Transient Immunity
- Fail-safe Receiver for Bus Open, Short, Idle
- 3.3-V Inputs are 5-V Tolerant
- Safety and Regulatory Approvals
  - 4000- $V_{PK}$   $V_{IOTM}$ , 560- $V_{PK}$   $V_{IORM}$  per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1
  - 2500  $V_{RMS}$  Isolation Rating per UL 1577
  - 2500  $V_{RMS}$  Isolation Rating per CSA CA5A and IEC 60950-1

### 2 Applications

- Security Systems
- Chemical Production
- Factory Automation
- Motor and Motion Control
- HVAC and Building Automation Networks
- Networked Security Stations

### 4 Simplified Schematics



### 3 Description

The ISO15 is an isolated half-duplex differential line transceiver while the ISO35 is an isolated full-duplex differential line driver and receiver for TIA/EIA 485/422 applications. The ISO15M and ISO35M have extended ambient temperature ratings of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  while the ISO15 and ISO35 are specified over  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical barrier of the device is tested to provide isolation of 4000  $V_{PK}$  per VDE and 2500  $V_{RMS}$  per UL and CSA between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO15	SOIC (16)	10.30 mm x 7.50 mm
ISO35		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Simplified Schematics</b> ..... 1 <b>5 Revision History</b> ..... 2 <b>6 Pin Configuration and Functions</b> ..... 4 <b>7 Specifications</b> ..... 5 7.1 Absolute Maximum Ratings ..... 5 7.2 ESD Ratings..... 5 7.3 Recommended Operating Conditions..... 5 7.4 Thermal Information ..... 6 7.5 Dissipation Ratings ..... 6 7.6 Supply Current ..... 6 7.7 Driver Electrical Characteristics ..... 6 7.8 Receiver Electrical Characteristics ..... 7 7.9 Driver Switching Characteristics ..... 7 7.10 Receiver Switching Characteristics..... 7 7.11 Typical Characteristics ..... 8 <b>8 Parameter Measurement Information</b> ..... 9	<b>9 Detailed Description</b> ..... 13 9.1 Overview ..... 13 9.2 Functional Block Diagrams ..... 13 9.3 Feature Description..... 14 9.4 Device Functional Modes..... 15 <b>10 Application and Implementation</b> ..... 18 10.1 Application Information..... 18 10.2 Typical Application ..... 18 <b>11 Power Supply Recommendations</b> ..... 20 <b>12 Layout</b> ..... 20 12.1 Layout Guidelines ..... 20 12.2 Layout Example ..... 21 <b>13 Device and Documentation Support</b> ..... 22 13.1 Documentation Support ..... 22 13.2 Related Links ..... 22 13.3 Trademarks ..... 22 13.4 Electrostatic Discharge Caution..... 22 13.5 Glossary ..... 22 <b>14 Mechanical, Packaging, and Orderable Information</b> ..... 22
---	--

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision F (January 2012) to Revision G

Page

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... 1
- Changed VDE standard to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12. .... 1

### Changes from Revision E (April 2010) to Revision F

Page

- Changed the FEATURES From: 4000- $V_{peak}$  560- $V_{peak}$   $V_{IORM}$  per IEC....Rev 2) To: 4000- $V_{PK}$   $V_{IOTM}$ , 560- $V_{PK}$  $V_{IORM}$ , IEC 60747-5-2 (VDE 0884, Rev 2)..... 1
- Changed Description From: The symmetrical isolation.....interface. To; The symmetrical isolation barrier of the device is tested to provide isolation of 4000  $V_{PK}$  per VDE and 2500  $V_{RMS}$  per UL and CSA between ....interface. .... 1
- Changed CTI From:  $\geq 175$  V To:  $\geq 400$  V..... 7
- Changed the Regulatory Information Table..... 7

### Changes from Revision D (March 2009) to Revision E

Page

- Added devices ISO15M and ISO35M to the data sheet ..... 1
- Changed Description - From: The ISO15 and ISO35 are qualified for use from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . To: The ISO15M and ISO35M have extended ambient temperature ratings of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  while the ISO15 and ISO35 are specified over  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ..... 1
- Added Added Ambient Temp information in the RECOMMENDED OPERATING CONDITIONS table..... 5
- Added ISO15M and ISO35M to the Operating junction temperature in the RECOMMENDED OPERATING CONDITIONS table ..... 5
- Changed the DRIVER ELECTRICAL table,  $I_{OZ}$  High-impedance state output current - Test Condition  $V_Y$  or  $V_Z = 12$  V,  $V_{CC} = 0$  values From: TYP = -10 , MAX = - To: TYP = -, MAX = 90. .... 6
- Changed the DRIVER ELECTRICAL table,  $I_{OZ}$  High-impedance state output current - Test Condition  $V_Y$  or  $V_Z = -7$

V values From: TYP = -, MAX = 90 To: TYP = -10, MAX = - .....	6
• Added I <sub>A</sub> or I <sub>B</sub> limits for the ISO15M ans ISO35M devices .....	7
• Added t <sub>r</sub> , t <sub>f</sub> limits for the ISO15M ans ISO35M devices .....	7
• Added pulse skew limits for the ISO15M ans ISO35M devices .....	7
• Added t <sub>r</sub> , t <sub>f</sub> for the ISO15M ans ISO35M devices.....	7
• Added the Driver output pins Note for <a href="#">Figure 3</a> through <a href="#">Figure 6</a> .....	9
• Changed the Driver output pins Note for <a href="#">Figure 7</a> through <a href="#">Figure 8</a> .....	10

---

<b>Changes from Revision C (December 2008) to Revision D</b>	<b>Page</b>
--	-------------

• Changed Propagation delay values From: $\mu$ s To: ns in the DRIVER SWITCHING table.....	7
--	---

---

<b>Changes from Revision B (July 2008) to Revision C</b>	<b>Page</b>
--	-------------

• Added added IEC.....Approved.....	1
• Added added CSA information column back in table.....	7

---

<b>Changes from Revision A (June 2008) to Revision B</b>	<b>Page</b>
--	-------------

• Changed From: 4000-Vpeak Isolation To: 4000-Vpeak Isolation, 560-Vpeak VIORM UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2) .....	1
• Changed <a href="#">Figure 15</a> , Full-Duplex Common-Mode Transient Immunity Test Circuit.....	12

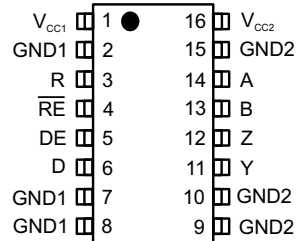
---

<b>Changes from Original (May 2008) to Revision A</b>	<b>Page</b>
---	-------------

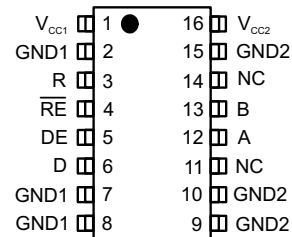
• Changed L(101) Minimum air gap (Clearance) From 7.7mm To 8.34mm. ....	7
• Changed From 40014131 To 40016131 .....	7
• Deleted CSA information from the Regulatory Information Table. ....	7

## 6 Pin Configuration and Functions

**ISO35x DW Package  
16-Pin SOIC  
Top View**



**ISO15x DW Package  
16-Pin SOIC  
Top View**



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	ISO15x NO.	ISO35x NO.		
V <sub>CC1</sub>	1	1	–	Logic side power supply
GND1	2,7,8	2,7,8	–	Logic side ground; internally connected
R	3	3	O	Receiver output
$\overline{RE}$	4	4	I	Receiver logic-low enable
DE	5	5	I	Driver logic-high enable input
D	6	6	I	Driver input
GND2	9,10,15	9,10,15	–	Bus side ground; internally connected
NC	11,14	–	–	Not connected internally; may be left floating
A	12	14	I/O	ISO15x: Noninverting bus input / output
			I	ISO35x: Noninverting bus input
B	13	13	I/O	ISO15x: Inverting bus input / output
			I	ISO35x: Inverting bus input
Y	–	11	O	Noninverting bus output
Z	–	12	O	Inverting bus output
V <sub>CC2</sub>	16	16	–	Bus side power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

		MAX	MAX	UNIT
$V_{CC}$	Input supply voltage. <sup>(2)</sup> $V_{CC1}$ , $V_{CC2}$	-0.3	6	V
$V_O$	Voltage at any bus I/O terminal	-9	14	V
$V_{IT}$	Voltage input, transient pulse, A, B, Y, and Z (through 100 $\Omega$ , see <a href="#">Figure 13</a> )	-50	50	V
$V_I$	Voltage input at any D, DE or $\overline{RE}$ terminal	-0.5	7	V
$I_O$	Receiver output current	-10	10	mA
$T_J$	Maximum junction temperature		170	$^{\circ}$ C
$T_{stg}$	Storage temperature	-65	150	$^{\circ}$ C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values

### 7.2 ESD Ratings

		VALUE	UNIT		
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Bus pins and GND1	$\pm$ 6000	V
			Bus pins and GND2	$\pm$ 16000	
			All pins	$\pm$ 4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	$\pm$ 1000		
		Machine model ANSI/ESDS5.2-1996	$\pm$ 200		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT	
$V_{CC}$	Supply Voltage, $V_{CC1}$ , $V_{CC2}$	3.15	3.3	3.6	V	
$V_{OC}$	Voltage at either bus I/O terminal	A, B	-7	12	V	
$V_{IH}$	High-level input voltage	D, DE, $\overline{RE}$	2	$V_{CC}$	V	
$V_{IL}$	Low-level input voltage		0	0.8		
$V_{ID}$	Differential input voltage	A with respect to B	-12	12	V	
$R_L$	Differential input resistance	54	60		$\Omega$	
$I_O$	Output current	Driver	-60	60	mA	
		Receiver	-8	8		
$1/t_{UI}$	Signaling rate	ISO15x and ISO35x		1	Mbps	
$T_A$	Ambient temperature	ISO15 and ISO35	-40	25	85	$^{\circ}$ C
		ISO15M and ISO35M	-55	25	125	
$T_J$	Operating junction temperature	ISO15 and ISO35	-40		150	$^{\circ}$ C
		ISO15M and ISO35M	-55		150	

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UNIT	ISO15, ISO35	
			DW (SOIC)	
			16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	High-K board	79.6	°C/W
		Low-K board	168	
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		39.7	
R <sub>θJB</sub>	Junction-to-board thermal resistance		44.6	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		11.8	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		44	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Dissipation Ratings

		VALUE	UNIT
P <sub>D</sub>	Device Power Dissipation	V <sub>CC1</sub> = V <sub>CC2</sub> = 3.6 V, T <sub>J</sub> = 150°C, C <sub>L</sub> = 15 pF, Input a 0.5 MHz 50% duty cycle square wave	220 mW

## 7.6 Supply Current

over recommended operating condition (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>CC1</sub>	Logic-side supply current	ISO35x and ISO15x	$\overline{RE}$ at 0 V or V <sub>CC</sub> , DE at 0 V, No load (driver disabled)			8	mA
			$\overline{RE}$ at 0 V or V <sub>CC</sub> , DE at V <sub>CC</sub> , No Load (driver enabled)			8	
I <sub>CC2</sub>	Bus-side supply current	ISO35x and ISO15x	$\overline{RE}$ at 0 V or V <sub>CC</sub> , DE at 0 V, No load (driver disabled)			15	mA
			$\overline{RE}$ at 0 V or V <sub>CC</sub> , DE at V <sub>CC</sub> , No Load (driver enabled)			19	

## 7.7 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Differential output voltage magnitude	I <sub>O</sub> = 0 mA, no load		2.5		V <sub>CC</sub>	V
		R <sub>L</sub> = 54 Ω, See <a href="#">Figure 3</a>		1.5	2		
		R <sub>L</sub> = 100 Ω (RS-422), See <a href="#">Figure 3</a>		2	2.3		
		V <sub>test</sub> from -7 V to +12 V, See <a href="#">Figure 4</a>		1.5			
Δ V <sub>OD</sub>	Change in magnitude of the differential output voltage	See <a href="#">Figure 3</a> and <a href="#">Figure 4</a>		-0.2	0	0.2	V
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	See <a href="#">Figure 5</a>		1	2.6	3	V
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage			-0.1		0.1	
V <sub>OC(pp)</sub>	Peak-to-peak common-mode output voltage	See <a href="#">Figure 5</a>			0.5		V
I <sub>I</sub>	Input current	D, DE, V <sub>I</sub> at 0 V or V <sub>CC1</sub>		-10		10	μA
I <sub>OZ</sub>	High-impedance state output current	ISO15	See receiver input current				μA
		ISO35	V <sub>Y</sub> or V <sub>Z</sub> = 12 V	Other input at 0 V		90	
			V <sub>Y</sub> or V <sub>Z</sub> = 12 V, V <sub>CC</sub> = 0			90	
			V <sub>Y</sub> or V <sub>Z</sub> = -7 V			-10	
	V <sub>Y</sub> or V <sub>Z</sub> = -7 V, V <sub>CC</sub> = 0			-10			
I <sub>OS</sub>	Short-circuit output current	V <sub>A</sub> or V <sub>B</sub> at -7 V		-250		250	mA
		V <sub>A</sub> or V <sub>B</sub> at 12 V					
C <sub>OD</sub>	Differential output capacitance	V <sub>I</sub> = 0.4 sin(4E6πt) + 0.5 V, DE at 0 V			16		pF
CMTI	Common-mode transient immunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, See <a href="#">Figure 14</a> and <a href="#">Figure 15</a>		25	50		kV/μs

## 7.8 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{IT(+)}$	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$			-20	mV	
$V_{IT(-)}$	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$	-200			mV	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			50		mV	
$V_O$	Output voltage	$V_{ID} = 200 \text{ mV}$ , See <a href="#">Figure 9</a>	$I_O = -8 \text{ mA}$	2.4		V	
			$I_O = 8 \text{ mA}$		0.4		
$I_{OZ}$	High-impedance state output current	$V_I = -7 \text{ to } 12 \text{ V}$ , Other input = 0 V	-1		1	$\mu\text{A}$	
$I_A$ or $I_B$	Bus input current	$-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	Other input at 0 V	$V_A$ or $V_B = 12 \text{ V}$	50	100	$\mu\text{A}$
				$V_A$ or $V_B = 12 \text{ V}$ , $V_{CC} = 0$	50	100	
		$85^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		$V_A$ or $V_B = 12 \text{ V}$		200	
				$V_A$ or $V_B = 12 \text{ V}$ , $V_{CC} = 0$		200	
		$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		$V_A$ or $V_B = -7 \text{ V}$	-100	-40	
				$V_A$ or $V_B = -7 \text{ V}$ , $V_{CC} = 0$	-100	-30	
$I_{IH}$	High-level input current, $\overline{RE}$	$V_{IH} = 2 \text{ V}$	-10			$\mu\text{A}$	
$I_{IL}$	Low-level input current, $\overline{RE}$	$V_{IL} = 0.8 \text{ V}$	-10			$\mu\text{A}$	
$R_{ID}$	Differential input resistance	A, B	48			k $\Omega$	
$C_{ID}$	Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{V}$ , DE at 0 V		16		pF	

## 7.9 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

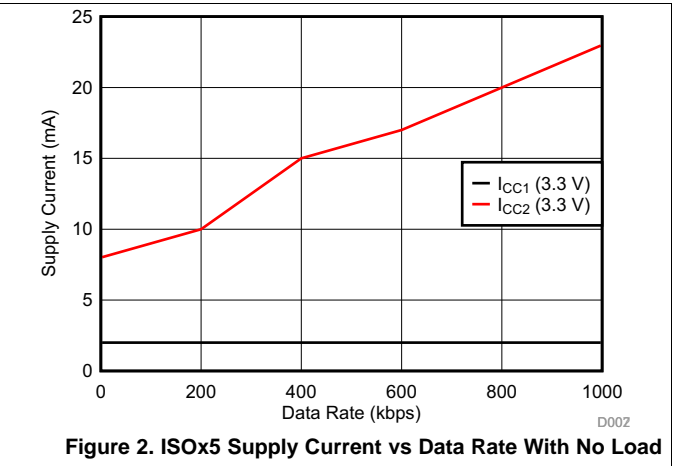
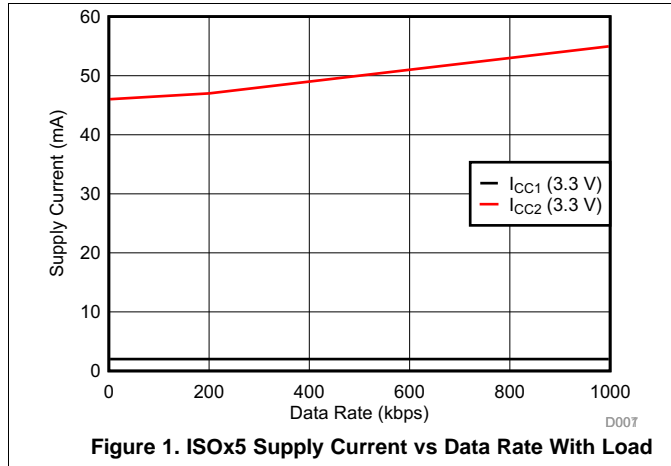
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay	See <a href="#">Figure 6</a>			340	ns
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )		6			
$t_r$ , $t_f$	Differential output signal rise time, fall time		ISO15 and ISO35	120	180	
		ISO15M and ISO35M	120	180	350	
$t_{PHZ}$	Propagation delay, high-level-to-high-impedance output	See <a href="#">Figure 7</a>			205	ns
$t_{PZH}$	Propagation delay, high-impedance-to-high-level output		530			
$t_{PLZ}$	Propagation delay, low-level to high-impedance output	See <a href="#">Figure 8</a>			330	ns
$t_{PZL}$	Propagation delay, standby-to-low-level output		530			

## 7.10 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO15x and ISO35x			100	ns
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )	ISO15 and ISO35			13	
		ISO15M and ISO35M			18	
$t_r$ , $t_f$	Output signal rise and fall time	ISO15 and ISO35		2	4	
		ISO15M and ISO35M		2	6	
$t_{PZH}$ , $t_{PZL}$	Propagation delay, high-impedance-to-high-level output Propagation delay, high-impedance-to-low-level output	DE at 0 V, See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>		13	25	ns
$t_{PHZ}$ , $t_{PLZ}$	Propagation delay, high-level-to-high-impedance output Propagation delay, low-level to high-impedance output			13	25	

## 7.11 Typical Characteristics





## 8 Parameter Measurement Information

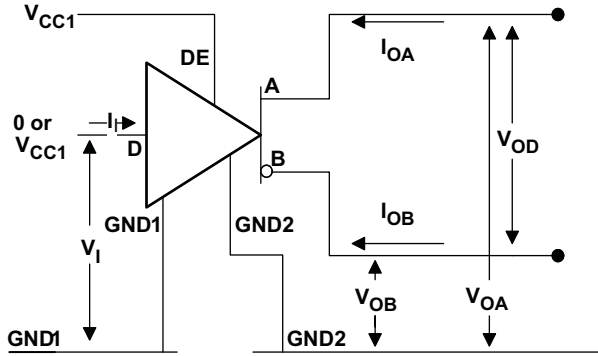


Figure 3. Driver  $V_{OD}$  Test and Current Definitions

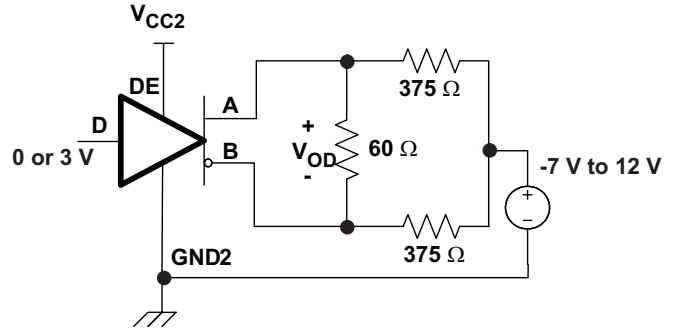


Figure 4. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit

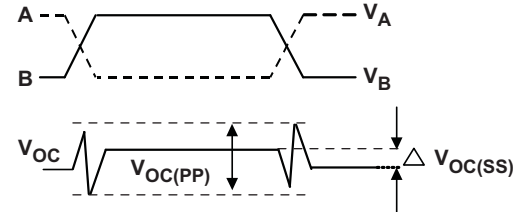
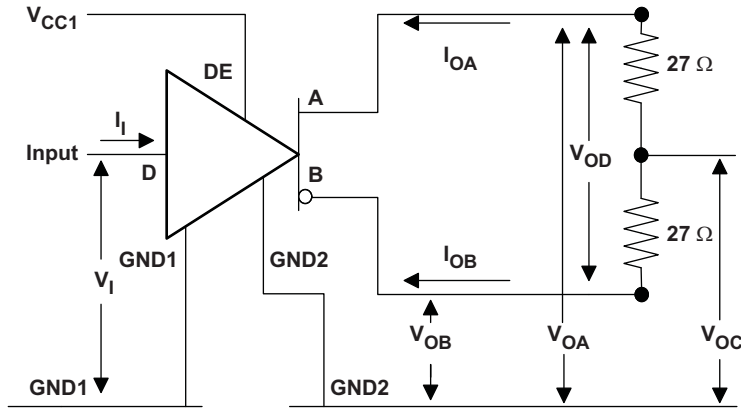
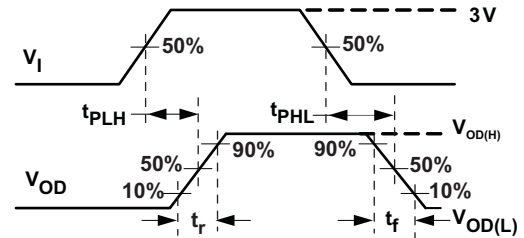
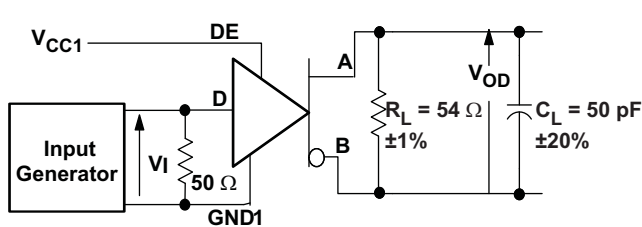


Figure 5. Test Circuit and Waveform Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% duty cycle,  $t_r < 6\text{ns}$ ,  $t_f < 6\text{ns}$ ,  $Z_0 = 50 \Omega$   
 $C_L$  includes fixture and Instrumentation Capacitance

Figure 6. Driver Switching Test Circuit and Voltage Waveforms

### NOTE

Driver output pins are A and B for the ISO15 (see Figure 3 through Figure 6). These correspond to ISO35 pins Y and Z

Parameter Measurement Information (continued)

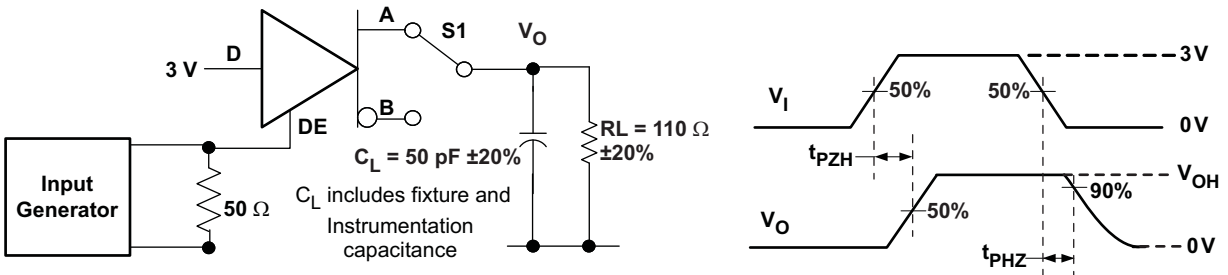


Figure 7. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

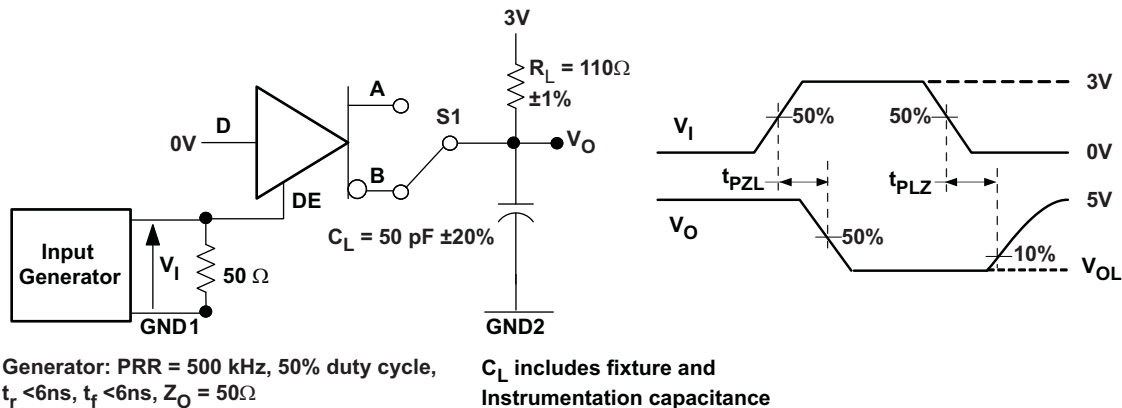


Figure 8. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

NOTE

Driver output pins are A and B for the ISO15 (see Figure 7 through Figure 8). These correspond to ISO35 pins Y and Z

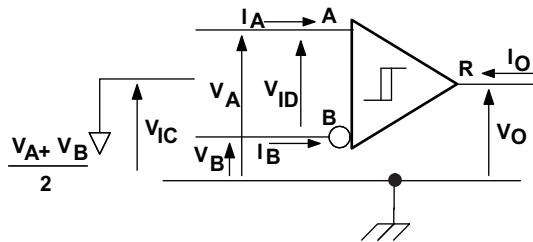


Figure 9. Receiver Voltage and Current Definitions

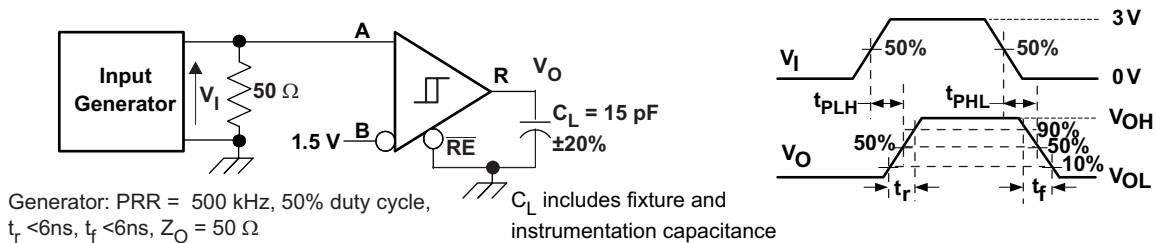


Figure 10. Receiver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

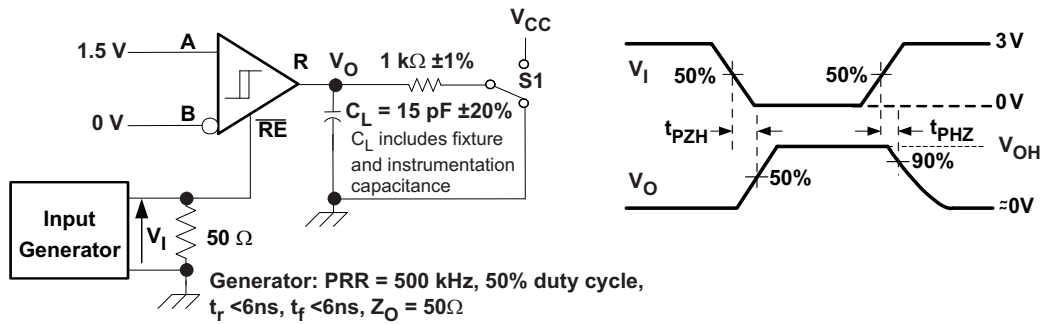


Figure 11. Receiver Enable Test Circuit and Waveforms, Data Output High

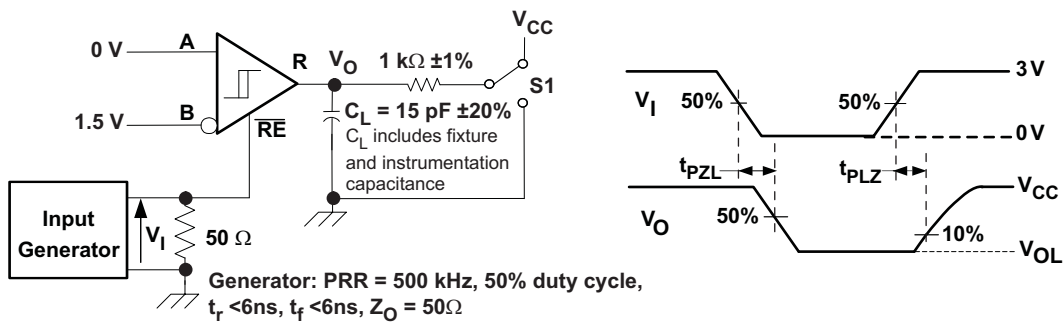
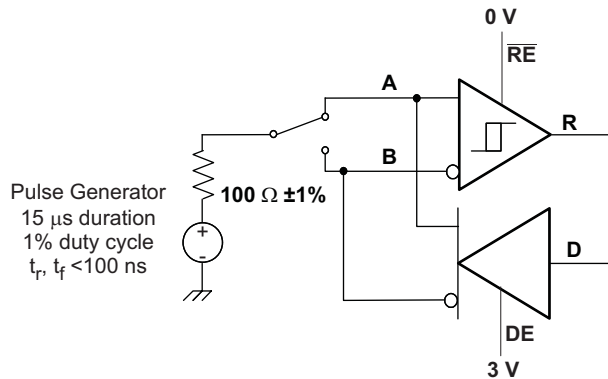


Figure 12. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only.  
Data stability at the R output is not specified.

Figure 13. Transient Overvoltage Test Circuit

Parameter Measurement Information (continued)

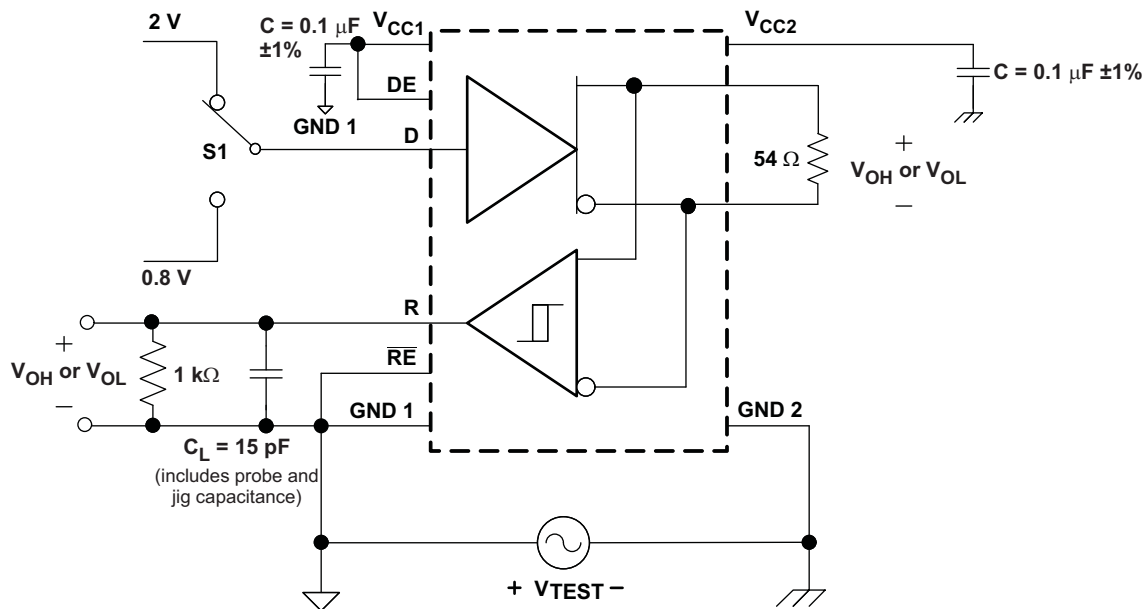


Figure 14. Half-Duplex Common-Mode Transient Immunity Test Circuit

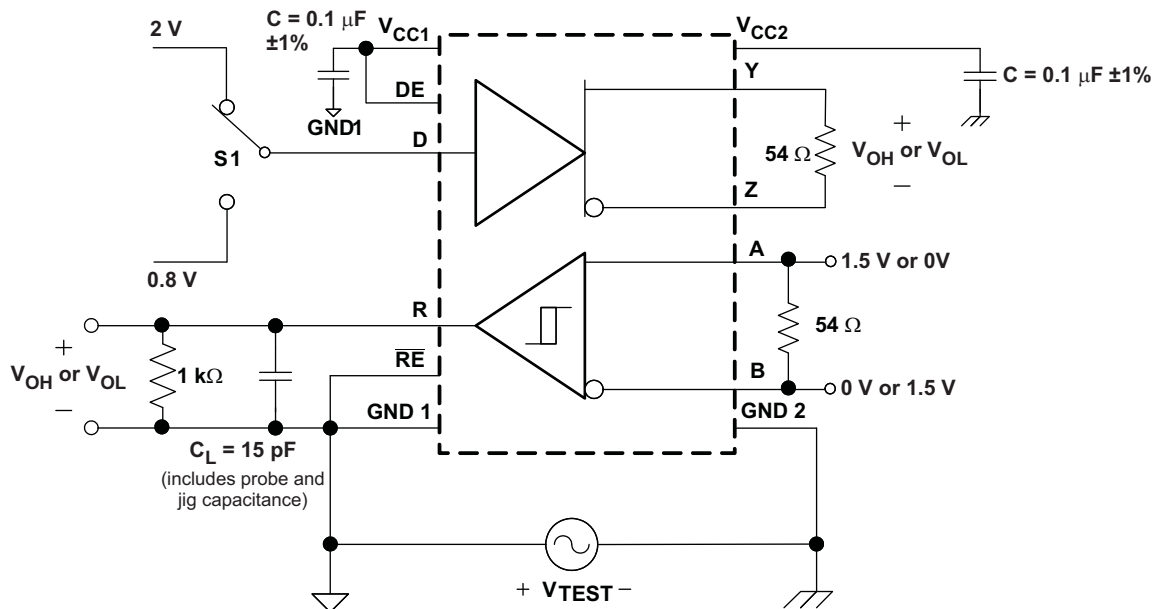


Figure 15. Full-Duplex Common-Mode Transient Immunity Test Circuit

## 9 Detailed Description

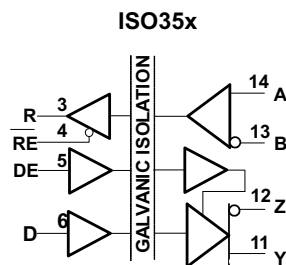
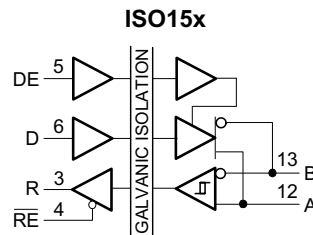
### 9.1 Overview

The ISO15 and ISO15M are isolated half-duplex differential line drivers and receivers while the ISO35 and ISO35M are isolated full-duplex differential line transceivers for TIA/EIA 485/422 applications. They are rated to provide galvanic isolation of up to 2500  $V_{rms}$  for 60 sec as per the standard. They have active-high driver enables and active-low receiver enables to control the data flow.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as  $V_{OD} = V_{(Y)} - V_{(Z)}$  is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and  $V_{OD}$  is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to  $V_{CC}$ , thus, when left open while the driver is enabled, output Y turns high and Z turns low.

When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_{(A)} - V_{(B)}$  is positive and higher than the positive input threshold,  $V_{IT+}$ , the receiver output, R, turns high. When  $V_{ID}$  is negative and less than the negative and lower than the negative input threshold,  $V_{IT-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{IT+}$  and  $V_{IT-}$  the output is indeterminate. When RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

### 9.2 Functional Block Diagrams



## 9.3 Feature Description

### 9.3.1 Insulation and Safety-Related Package Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance) <sup>(1)</sup>	Shortest terminal to terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage) <sup>(1)</sup>	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
DTI	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R <sub>IO</sub>	Isolation resistance	Input to output, V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C, all pins on each side of the barrier tied together creating a two-terminal device		>10 <sup>12</sup>		Ω
C <sub>IO</sub>	Barrier capacitance input to output	V <sub>I</sub> = 0.4 sin (4E6πt)		2		pF
C <sub>I</sub>	Input capacitance to ground	V <sub>I</sub> = 0.4 sin (4E6πt)		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

### 9.3.2 DIN V VDE V 0884-10 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)<sup>(2)</sup>

PARAMETER	TEST CONDITIONS	SPECIFICATION	UNIT
V <sub>IOTM</sub>	Transient overvoltage	Method a, t = 60 s, Qualification test	4000
V <sub>IORM</sub>	Maximum working insulation voltage		560
V <sub>PR</sub>	Input to output test voltage	Method b1, V <sub>PR</sub> = V <sub>IORM</sub> × 1.875, 100% Production test with t = 1 s, Partial discharge < 5 pC	1050
R <sub>S</sub>	Insulation resistance	V <sub>IO</sub> = 500 V at T <sub>S</sub>	>10 <sup>9</sup>
	Pollution degree		2

(2) Climatic Classification 40/125/21

### 9.3.3 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-IV
	Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-III
	Rated mains voltage ≤ 400 V <sub>RMS</sub>	I-II

### 9.3.4 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Approved under CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program <sup>(1)</sup>
Basic insulation, 4000 V <sub>PK</sub> Maximum transient overvoltage, 560 V <sub>PK</sub> Maximum working voltage	2500 V <sub>RMS</sub> Isolation rating, 396 V <sub>PK</sub> Basic working voltage per CSA 60950-1-07 and IEC 60950-1 (2nd Ed)	Single Protection, 2500 V <sub>RMS</sub>
Certificate number: 40016131	Master contract number: 220991	File number: E181974

(1) Production tested ≥3000 V<sub>RMS</sub> for 1 second in accordance with UL 1577.

### 9.3.5 Safety-Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		MIN	TYP	MAX	UNIT	
$I_S$	Safety input, output, or supply current	DW-16	$\theta_{JA} = 168\text{ }^\circ\text{C/W}$ , $V_I = 3.6\text{ V}$ , $T_J = 170\text{ }^\circ\text{C}$ , $T_A = 25\text{ }^\circ\text{C}$		240	mA
$T_S$	Maximum case temperature	DW-16			150	$^\circ\text{C}$

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in [Thermal Information](#) is that of a device installed in a Low-Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

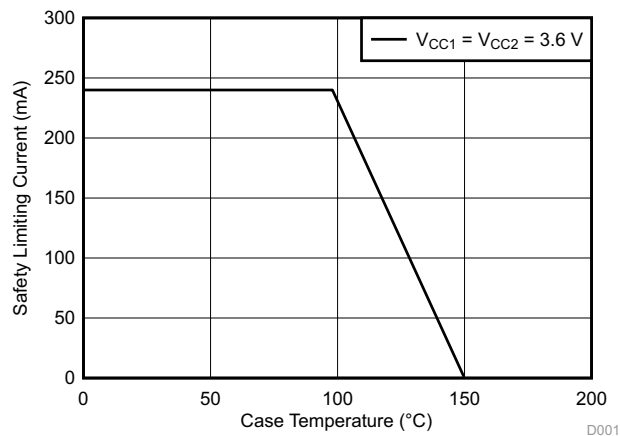


Figure 16. DW-16  $\theta_{JC}$  Thermal Derating Curve per VDE

### 9.4 Device Functional Modes

Table 1. Driver Function Table<sup>(1)</sup>

$V_{CC1}$	$V_{CC2}$	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS <sup>(2)</sup>	
				Y / A	Z / B
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Hi-Z	Hi-Z
PU	PU	X	OPEN	Hi-Z	Hi-Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Hi-Z	Hi-Z
PU	PD	X	X	Hi-Z	Hi-Z
PD	PD	X	X	Hi-Z	Hi-Z

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, Hi-Z = High Impedance (off)  
 (2) Driver output pins are Y and Z for full-duplex devices and A & B for half-duplex devices.

**Table 2. Receiver Function Table<sup>(1)</sup>**

$V_{CC1}$	$V_{CC2}$	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ( $\overline{RE}$ )	OUTPUT (R)
PU	PU	$-0.01\text{ V} \leq V_{ID}$	L	H
PU	PU	$-0.2\text{ V} < V_{ID} < -0.01\text{ V}$	L	?
PU	PU	$V_{ID} \leq -0.2\text{ V}$	L	L
PU	PU	X	H	Hi-Z
PU	PU	X	OPEN	Hi-Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Hi-Z
PU	PD	X	L	H

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, Hi-Z = High Impedance (off), ? = Indeterminate



9.4.1 Device I/O Schematics

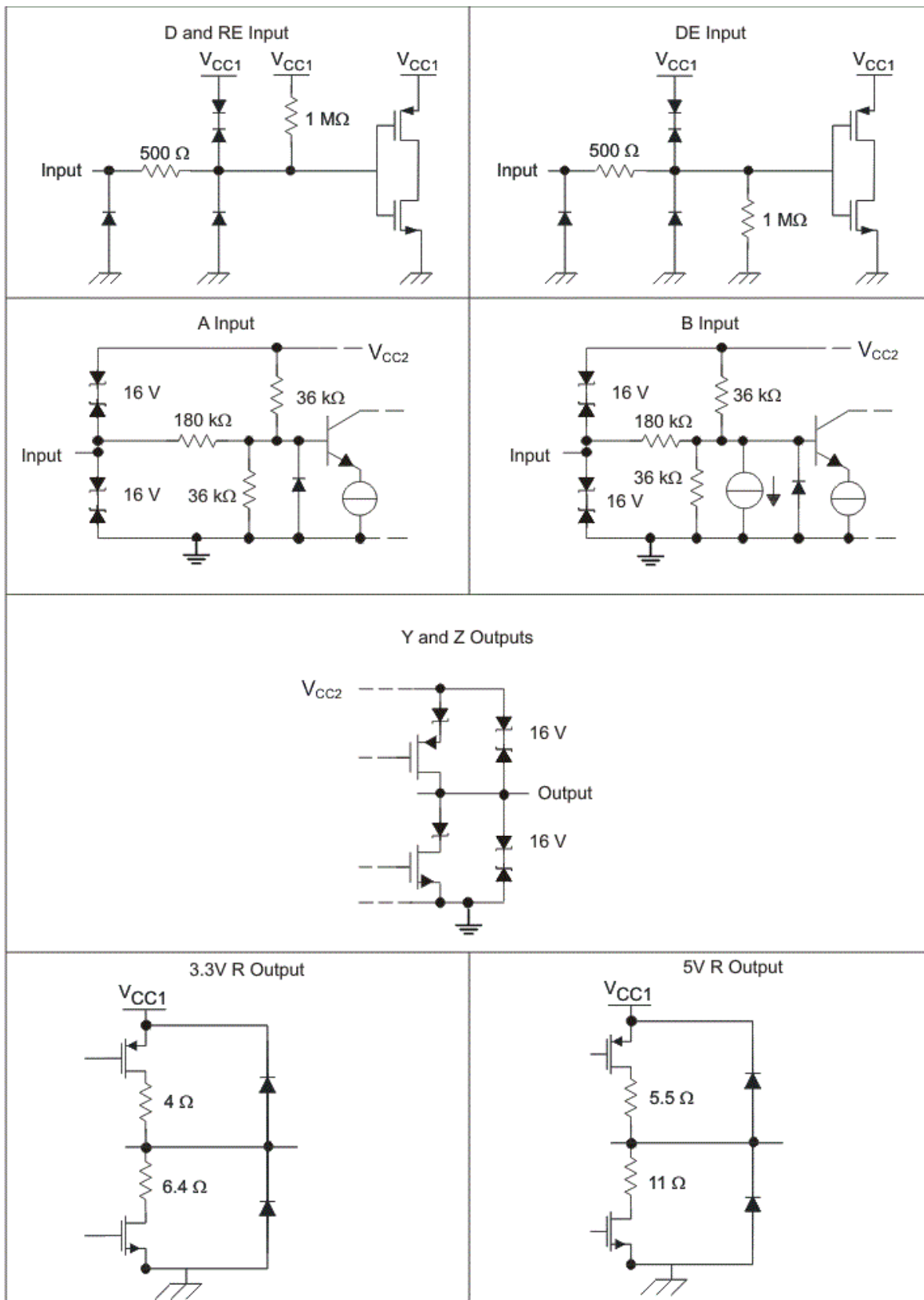


Figure 17. Device I/O Schematics

## 10 Application and Implementation

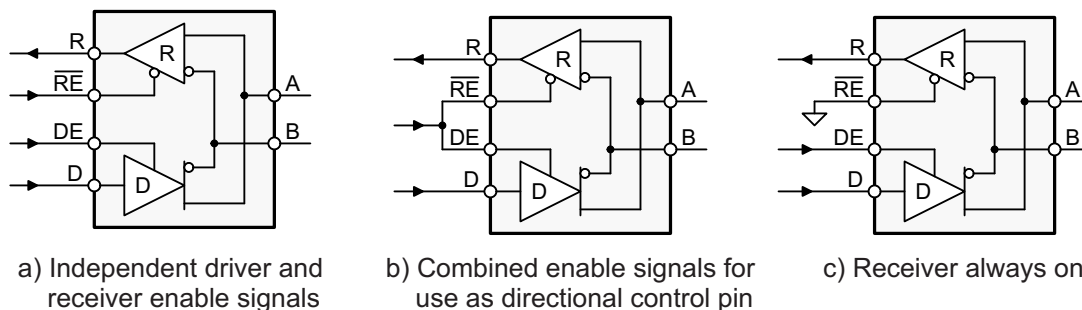
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

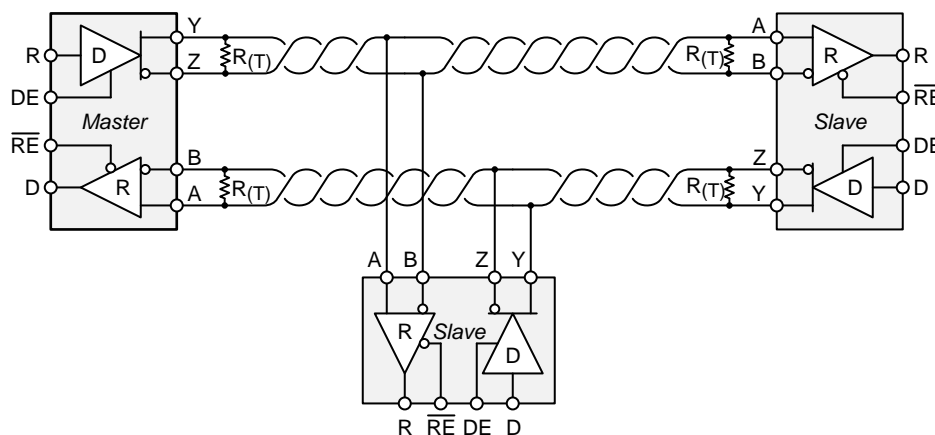
### 10.1 Application Information

The ISO15x and ISO35x family consists of RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. For half-duplex transmission there is only one pair which shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R(T)$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

### 10.2 Typical Application



**Figure 18. Half-Duplex Transceiver Configurations**



**Figure 19. Typical RS-485 Network With Full-Duplex Transceivers**

## Typical Application (continued)

### 10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

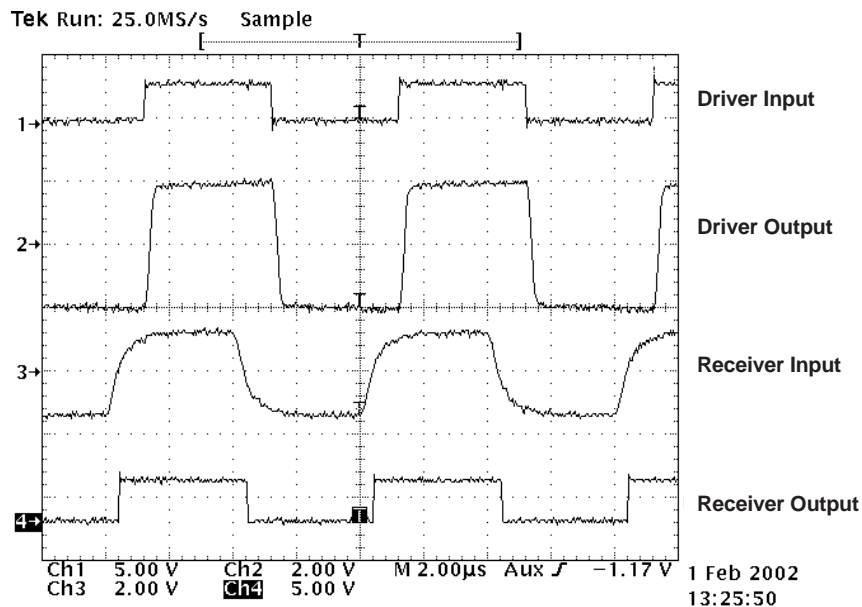
**Table 3. Design Parameters**

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

### 10.2.2 Detailed Design Procedure

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver. The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because these devices consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

### 10.2.3 Application Curve



**Figure 20. Typical Input and Output Waveforms**

## 11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet ([SLLSEA0](#)).

## 12 Layout

### 12.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, highfrequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 21](#)).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating the board.
- Use VCC and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC-pins of transceiver, UART, controller ICs on the board (see [Figure 21](#)).
- Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance (see [Figure 21](#)).
- Use 1-k $\Omega$  to 10-k $\Omega$  pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events (see [Figure 21](#)).
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up (see [Figure 21](#)).
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

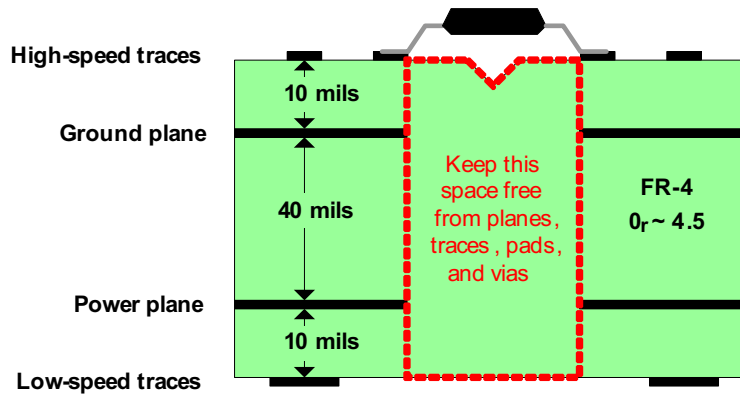
If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

**Layout Guidelines (continued)**

**NOTE**

For detailed layout recommendations, see Application Note [SLLA284](#), *Digital Isolator Design Guide*.

**12.2 Layout Example**



**Figure 21. Recommended Layer Stack**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide*, [SLLSEA0](#)
- *Transformer Driver for Isolated Power Supplies*, [SLLA284](#)

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO15	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ISO35	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ISO15M	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ISO35M	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.3 Trademarks

All trademarks are the property of their respective owners.

### 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

[SLLA353](#) -- *Isolation Glossary*.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO15DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	<a href="#">Samples</a>
ISO15DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	<a href="#">Samples</a>
ISO15DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15	<a href="#">Samples</a>
ISO15MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO15M	<a href="#">Samples</a>
ISO15MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO15M	<a href="#">Samples</a>
ISO35DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	<a href="#">Samples</a>
ISO35DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	<a href="#">Samples</a>
ISO35DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35	<a href="#">Samples</a>
ISO35MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO35M	<a href="#">Samples</a>
ISO35MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO35M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO15DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO15MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO15DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO15MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO35DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO35MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

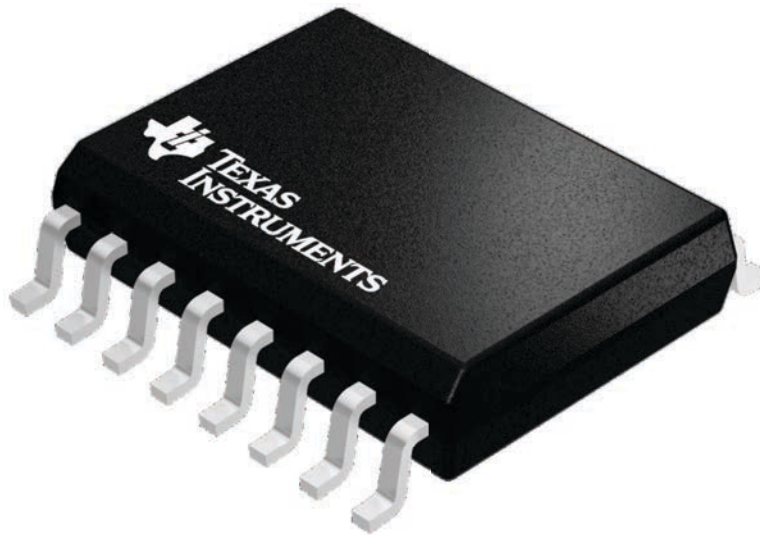
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

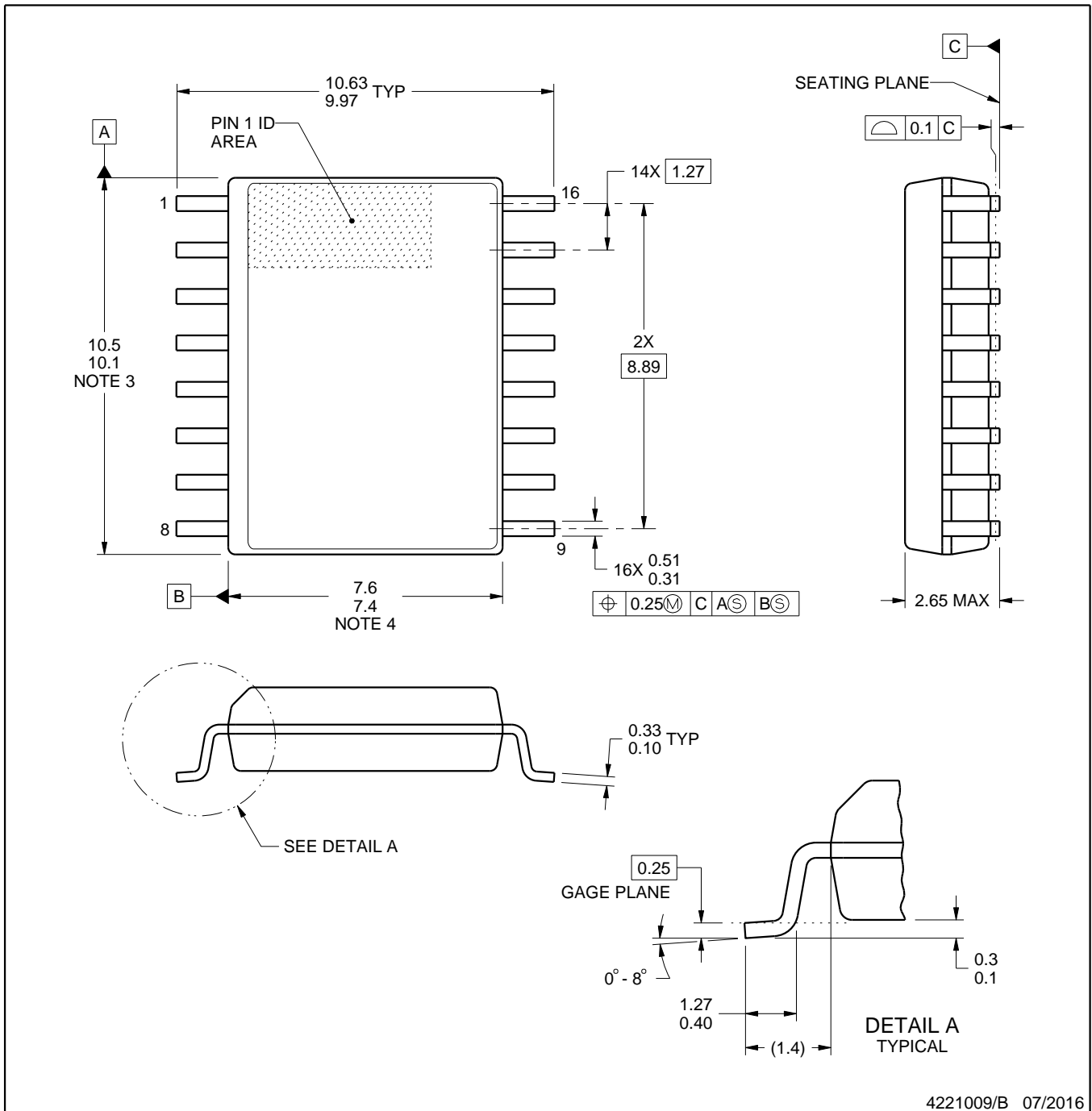


# DW0016B

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

### NOTES:

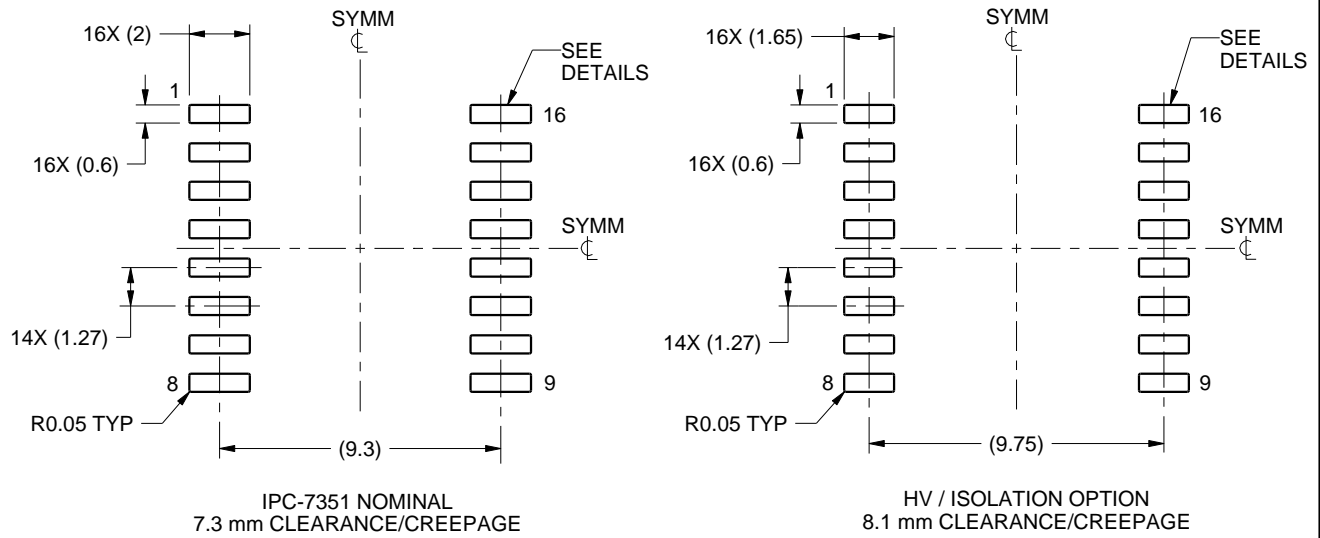
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

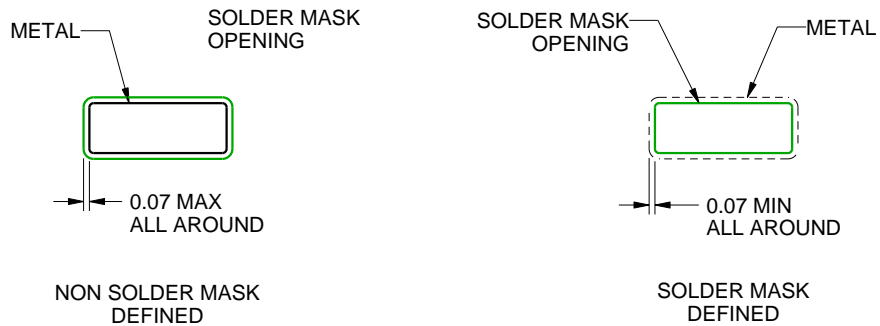
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

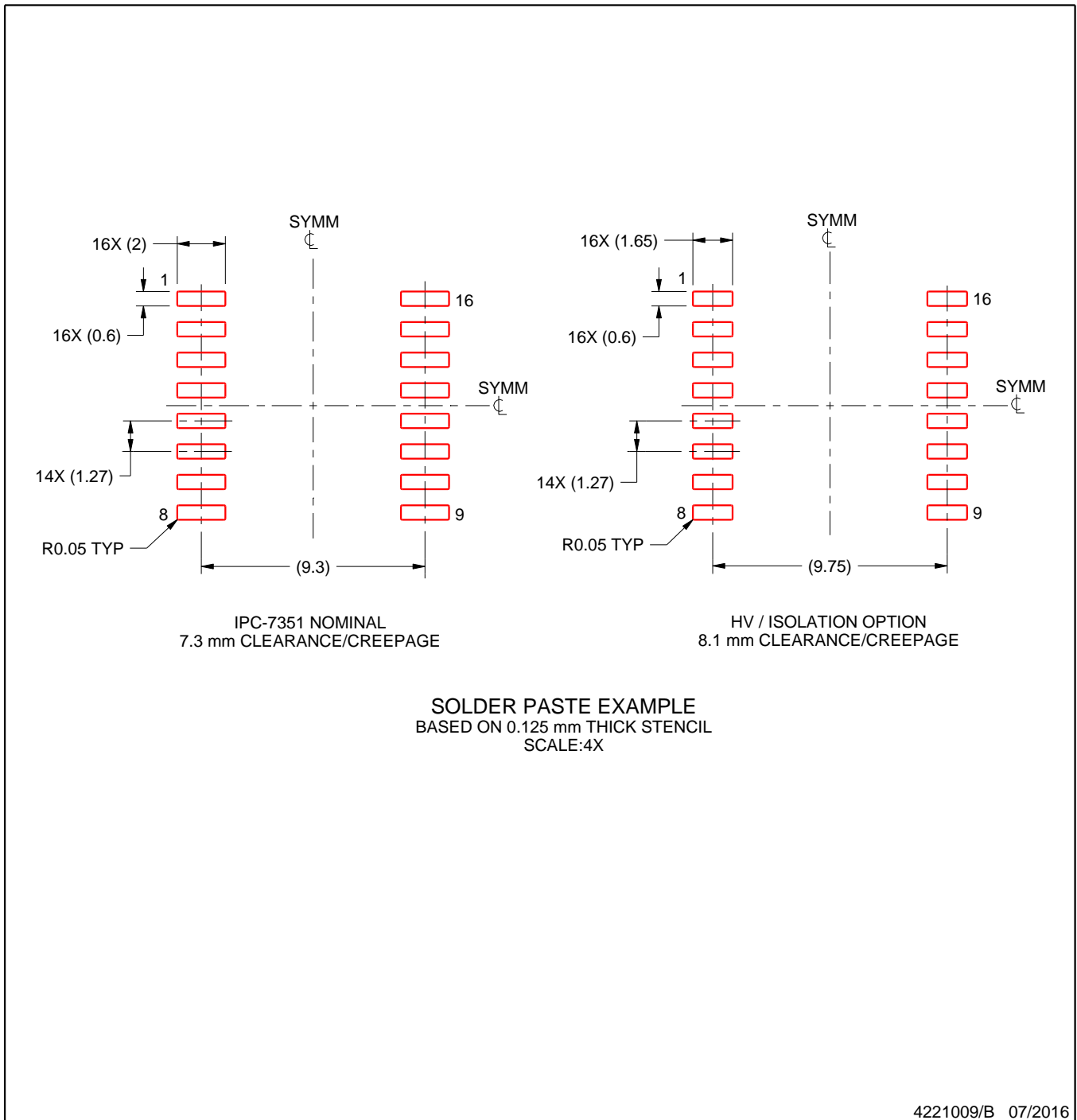
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated