iC-HTG
POWER CW LASER DIODE DRIVER

preliminary

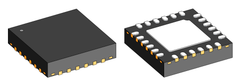
FEATURES

- CW operation with external driver transistor
- 3.3 to 24 V power supply
- Analog modulation frequency of up to 50 kHz
- Internal programmable logarithmic monitor resistor
- Operating point setup with a logarithmic resolution of 10 bits
- Current or Power control mode (ACC/APC) configurable
- A/D converters for analog signals monitoring
- Serial programming interface (SPI or I^2C compliant)
- Configuration RAM content integrity monitored.
- Optimized for both N-type and P-type laser diodes
- Low drop linear regulator for 3.3 V
- Low current standby mode
- Temperature monitor
- Temperature range of -40 to 85 °C

APPLICATIONS

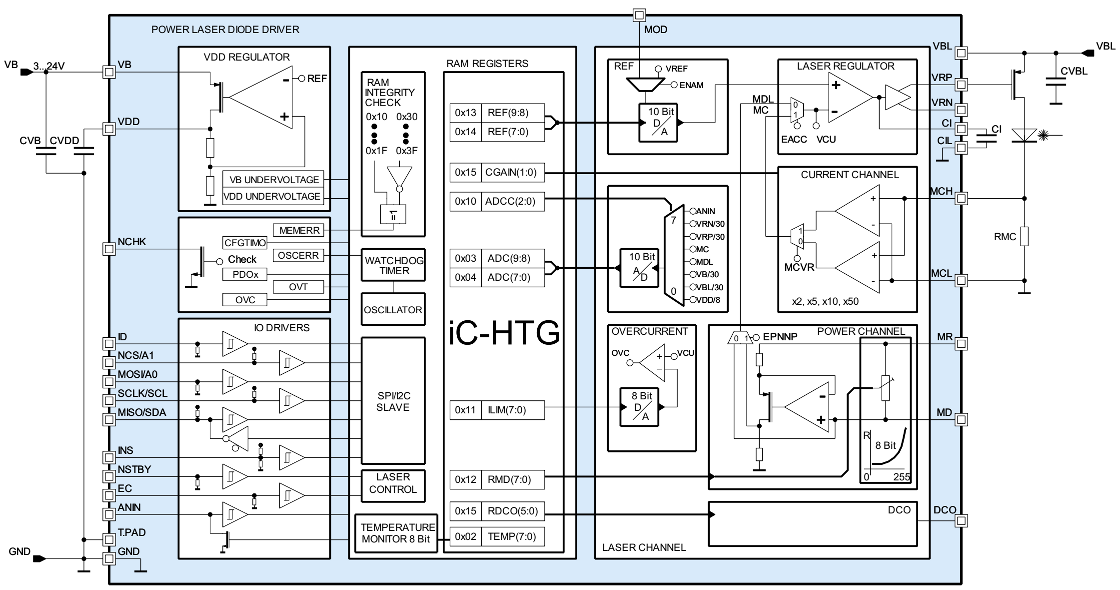
- Commercial LED/Laser diode modules
- Safety related CW laser diode drivers
- Structured-light 3D illumination
- Laser diode stack control
- Optical amplification
- Optical pumping

PACKAGES



QFN24 4 mm x 4 mm

BLOCK DIAGRAM



DESCRIPTION

The CW power laser diode driver iC-HTG can operate an external laser or LED diode with an external power transistor and has automatic current (ACC) and power (APC) control functionality. All parameters, including the internal reference voltages, are set via serial communication (I^2C or SPI). A 10-bit resolution D/A converter with logarithmic characteristic is used to set the operating point of the laser or LED. This allows an operating point resolution better than 1%. In APC mode, the monitor diode photocurrent is used to track the optically emitted power of the laser diode. The voltage present over a resistor through which the photocurrent flows is used for feedback in the control loop. An 8-bit internal programmable logarithmic monitor resistor (PLR) or an external monitor resistor can be selected to close the control loop. The PLR ranges from 100 Ω to 500 kΩ with a step width of less than 5%. In ACC mode, the laser diode current can be measured by means of a low impedance shunt resistor. The output power can be analog modulated with a frequency of up to 50 kHz. iC-HTG allows the laser channel to be disabled when an overcurrent threshold has been exceeded. The overcurrent threshold is programmable using an 8-bit linear D/A converter. The temperature monitor measures the internal chip temperature. iC-HTG disables the laser channel when overtemperature is detected. A variety of voltages can be measured with a 10-bit A/D converter. The following voltages can be measured:

- V(VB)
- V(VBL)
- V(VDD)
- V(ANIN)
- V(MC)
- V(MDL)
- V(VRP)
- V(VRN)

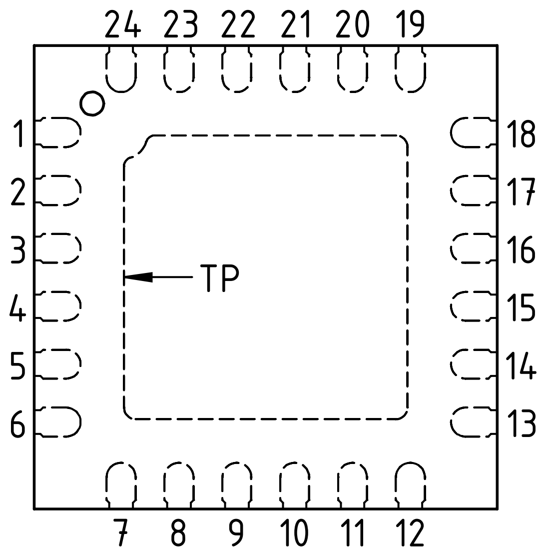
The current output pin DCO can be used to adjust an external DC/DC converter. Controlling the DC/DC output voltage may optimize the power dissipation of the whole system to extend battery life, for example. In standby mode, iC-HTG has a very low current consumption (typ. < 10 µA) while retaining its configuration. The device features for **safe operation** are:

- Configuration RAM content integrity monitored
- Tri-state configuration pins
- Write protection in operating mode
- Safe power-up state

CONTENTS

PACKAGING INFORMATION QFN24 4 mm x 4 mm to JEDEC

PIN CONFIGURATION QFN24 4 mm x 4 mm (topview)



PIN FUNCTIONS

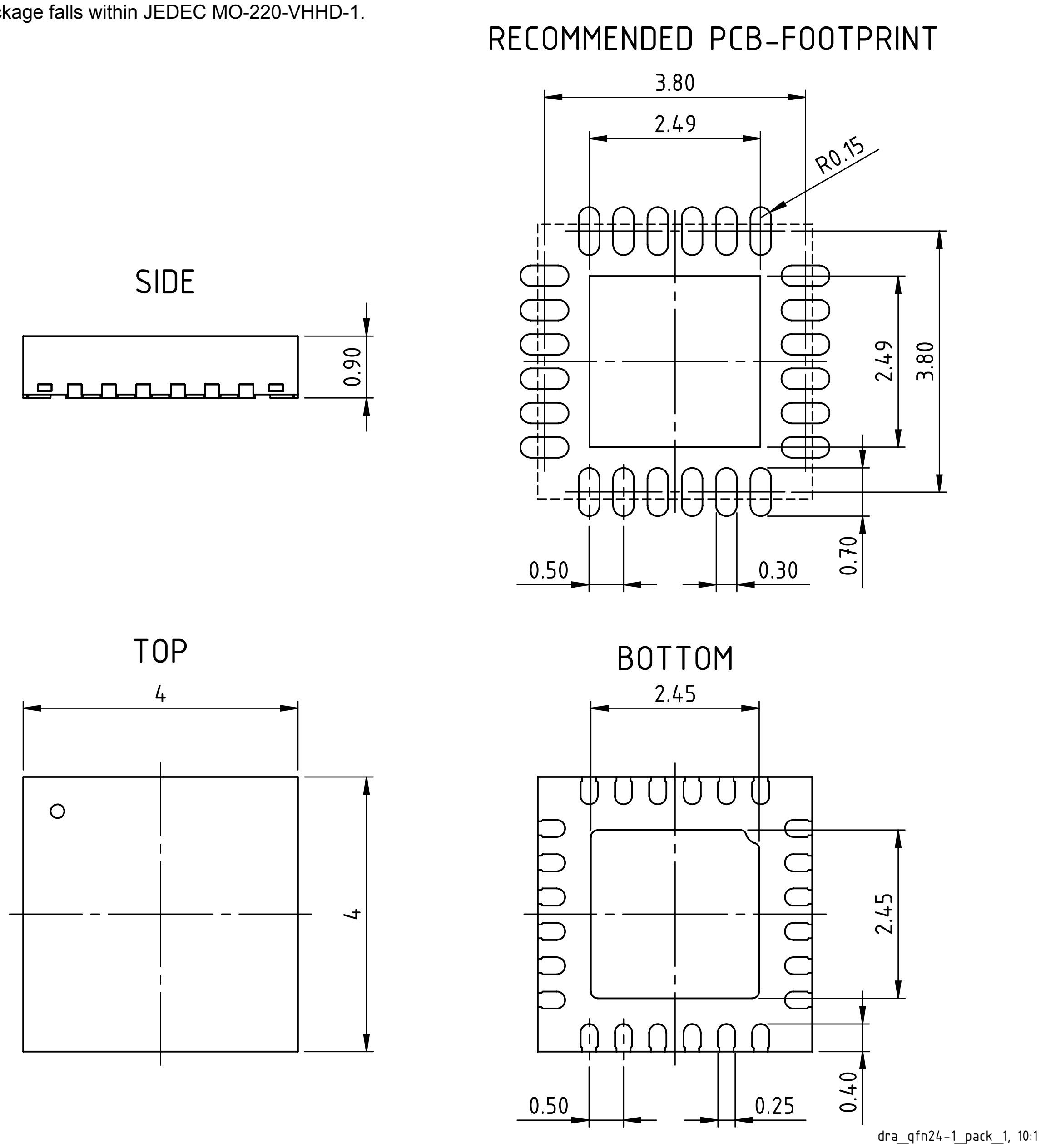
No.	Name	Function
1	NCHK	Check output, active low
2	NSTBY	Standby input, active low
3	NCS/A1	Chip Select, active low / I^{2}C Address bit 1
4	ID	I^{2}C address bit 2
5	EC	Enable Channel input
6	MOSI/A0	SPI Master Out Slave In / I^{2}C Address Bit 0
7	SCLK/SCL	SPI Clock / I^{2}C Clock
8	MISO/SDA	SPI Master In Slave OUT / I^{2}C Data
9	ANIN	Analog input for ADC
10	MCH	Current monitor high side
11	MCL	Current monitor low side
12	MOD	Analog modulation
13	CI	Integration Capacitor high side
14	CIL	Integration Capacitor low side
15	VRN	N transistor regulation
16	VRP	P transistor regulation
17	VBL	Channel supply
18	MD	Monitor diode
19	MR	Monitor resistor
20	GND	Ground
21	DCO	DC/DC converter trimmer
22	INS	I^{2}C or SPI selection input
23	VDD	3.3 V output supply
24	VB	Power supply
	BP(TP)	Backside Paddle (GND) [1)]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes).

1) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS QFN24-4x4

All dimensions given in mm.
This package falls within JEDEC MO-220-VHHD-1.



ABSOLUTE MAXIMUM RATINGS

These ratings do not imply permissible operating conditions; functional operation is not guaranteed. Exceeding these ratings may damage the device.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VB	Voltage at VB, VBL		-0.3	30	V
G002	I(VB)	Current in VB, VBL		-20	50	mA
G003	VDD	Voltage at VDD		-0.3	5.5	V
G004	I(VDD)	Current in VDD		-20	1	mA
G005	V()	Voltage at DCO, ANIN, SCLK/SCL, MISO/SDA, MOSI/A0, NCS/A1, DCO, INS, NCHK, CI, MOD		-0.3	5.5	V
G006	V()	Voltage at VRP, VRN, MCH, MCL, NSTBY			30	V
G007	I()	Current in DCO, ANIN, SCLK/SCL, MISO/SDA, MOSI/A0, NCS/A1, DCO, INS, NCHK, CI, VRP, VRN, MCH, MCL, NSTBY		-20	20	mA
G008	V()	Voltage at CIL		-0.3	0.5	V
G009	I(CIL)	Current in CIL	DC current	-900	1	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Operating Junction Temperature		-40	85	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VB = 3 . . . 24 V (referenced to GND)

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Mounted on PCB		25		K/W
T03	RthjTP	Thermal Resistance Chip/Thermal Pad			4		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 3 . . . 24 V (relative to GND), Tj = -40 . . . 125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General Functionality and parameters beyond the operating conditions (with reference to independent voltage supplies, for instance) are to be verified within the individual application using FMEA methods.							
001	VB	Permissible Supply Voltage	Relative to GND	3		24	V
002	I(VB)	Standby Current at VB	V(NSTBY) ≤ 0.4 V, VB = 3. . . 11 V VB = 11. . . 24 V			 10 30	 µA µA
003	I(VBL)	Standby Current at VBL	V(NSTBY) ≤ 0.4 V, VBL = 3. . . 11 V VBL = 11. . . 24 V			 5 10	 µA µA
004	I(VB)	Supply Current at VB	No load, EC, NSTBY = hi			5	mA
005	I(VBL)	Supply Current at VBL	No load, EC, NSTBY = hi			25	mA
006	V(VB)on	Turn-on threshold at VB, VBL	Increasing VB, VBL	1		2.9	V
007	V(VB)off	Turn-off threshold at VB, VBL	Decreasing VB, VBL	0.8		2.6	V
008	V(VB)Hys	Power-on hysteresis at VB, VBL		20		250	mV
009	V(VDD)on	Turn-on threshold	Increasing VDD	1.3		2.4	V
010	V(VDD)off	Turn-off threshold	Decreasing VDD	1.2		2.3	V
011	V(VDD)Hys	Power-on hysteresis		20		250	mV
012	V(VB)INITR	RAM memory reset during Stand-By	NSTBY = lo	0.85		1.4	V
013	RCIL()	Resistor between GND and CIL				20	Ω
014	Vc()lo	Clamp Voltage lo at VB, VBL, VDD, NCHK, NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, INS, NSTBY, EC, DCO, CI, MD, MR, MCH, MCL, VRP, VRN, MOD	I() = -10 mA	-1.6		-0.3	V
Transistor Driver VRx, CIx, MCx, MR, MD							
101	C(CI)	Required capacitor at CI	CW Analog Modulation	1000	 80		pF pF
102	I(CI)	Charge Current at CI	V(CI) = 0 V, CI regulated	-30		-5	µA
103	V(MCx)	Permisible Voltage at MCH, MCL	EC = hi, NSTBY = hi MCVR = lo MCVR = hi	 0 VBL-5		 5 VBL	 V V
104	Tci	Permisible Voltage at MR, MD	EC = hi, NSTBY = hi EPNNP = lo EPNNP = hi	 0 VDD-1.2		 1.2 VDD	 V V
105	I(VRx)max	Short Circuit Current at VRP, VRN	EC = hi, NSTBY = hi V(VRP) = 1.5 V . . . VBL V V(VRN) = 1.5 V . . . VBL V; VRNHR = hi V(VRN) = 0 V . . . VBL-1.5 V; VRNHR = lo	 -200		 200 200	 mA mA mA
106	V(VRP)	Voltage output range	|I(VRP)| < 1mA	1		VBL	V
107	V(VRN)	Voltage output range	|I(VRN)| < 1mA VRNHR = lo VRNHR = hi	 0 1		 VBL-1.5 VBL	 V V
108	Ten	Time to laser enabled	NSTBY lo → hi, no load at VDD, V(VDD) 0 to 90 %, CVDD = 1 µF			1.3	ms
Programmable Resistor							
201	Rmda	Resistor at MD and MR pin	RMD(7:0) = 0xFF, DISP = 0 RMD(7:0) = 0x00, DISP = 0	350 0.154	500 0.220	650 0.286	kΩ kΩ
202	Tk	Temperature coefficient			-500		ppm/K

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 3 . . . 24 V (relative to GND), Tj = -40 . . . 125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
203	ΔR	Resistor increment	$\Delta R = \frac{R(n+1)-R(n)}{R(n)}$	1	3.3	7	%
204	Ileak(MDA)	MD, MR leakage current	DISP = 1	-2		2	μA
D/A Converter							
301	RES(DAC)	D/A Converter Resolution				10	bit
302	ΔV	Voltage increments	$\Delta V = \frac{V(n+1)-V(n)}{V(n)}$	0.05	0.235	1	%
303	V(DAC)	D/A Converter	REF(9:0) = 0x000 lowest value REF(9:0) = 0x3FF highest value	0.09 1.00	0.10 1.10	0.12 1.25	V V
304	V(REF)	D/A Converter	V(MOD)=1.1V, Analog Modulation Enabled REF(9:0) = 0x000 lowest value REF(9:0) = 0x3FF highest value	 0.09 1.00	 0.10 1.10	 0.12 1.25	 V V
305	G()	Gain Factor	ACC mode CGAIN(1:0) = 00 CGAIN(1:0) = 01 CGAIN(1:0) = 10 CGAIN(1:0) = 11	 1.5 3 7 43	 2 5 10 50	 2.5 7 13 57	
Check Output NCHK							
401	Vs()lo	Saturation Voltage lo at NCHK	I(NCHK) = 1.0 mA			0.4	V
402	Isc()lo	Short Circuit Current lo at NCHK	V(NCHK) = 0.4 . . . 3.3 V	9		33	mA
403	Ilk()	Leakage Current at NCHK	NCHK = 1; V(NCHK) = 0 . . . 5.5 V	 -10		 10	 μA
Series Regulator Output VDD							
501	V(VDD)	Regulated output voltage	I(VDD) = -10 . . . 0 mA NSTBY = hi	3		3.5	V
502	V(VB,VDD)	Voltage Drop between VB and VDD	VB=3 V , I(VDD) = -10 . . . 0 mA NSTBY = hi		300	630	mV
503	C(VDD)	Capacitor at VDD	Ri(C) < 1 Ω	1		3.3	μF
504	Tvdd	Settling time VDD	NSTBY lo → hi, no load at VDD, V(VDD) 0 to 90 % CVDD = 1 μF			1	ms
505	Isc(VDD)	Short circuit current at VDD	VDD Connected to GND			-125	mA
Digital inputs/output NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, ID, NSTBY, EC, ANIN							
601	Vt()hi	Input Threshold Voltage hi at NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, ID, NSTBY, EC, ANIN	MISO/SDA as input with INS = hi			2	V
602	Vt()lo	Input Threshold Voltage lo at NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, ID, NSTBY, ANIN, EC, ANIN	MISO/SDA as input with INS = hi	0.7			V
603	Vt()hys	Hysteresis at NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, ID, NSTBY, ANIN, EC	Vt()hys = Vt()hi - Vt()lo	50			mV
604	Ipd()	Pull-Down Current at MOSI/A0, EC	V() = 0.4 V . . . VDD	1		50	μA
605	Ipd()	Dynamic Pull-Down Current at NSTBY	V() = 0.4 V . . . Vt()hi V() = Vt(hi) . . . VB	2 1		50 15	μA μA
606	Rpu()	Pull-Up Resistor at NCS/A1, SCLK/SCL		80	150	260	kΩ
607	Rpu()	Pull-Up Resistor at MISO/SDA	INS = lo INS = hi	8 53	20 100	50 174	kΩ kΩ
608	Er()	Safe enable threshold voltage at INS	Rising Falling	52 30	54 32	56 34	% VDD % VDD
609	Voc()	Open Circuit Voltage at INS		39	41	43	% VDD

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 3 . . . 24 V (relative to GND), Tj = -40 . . . 125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
610	Ri()	Internal Resistance at INS		170	250	330	kΩ
611	Isc()lo	Short Circuit current lo at MISO/SDA	INS = lo, V(MISO/SDA) = 5.5 V	-40		-4	mA
612	Vs()lo	Saturation Voltage lo at MISO/SDA	INS = lo, I(MISO/SDA) = 2 mA			0.4	V
613	Isc()lo	Short Circuit current lo at ANIN	ANIN as output, V(ANIN) = 5.5 V	-40		-4	mA
614	Vs()lo	Saturation Voltage lo at ANIN	ANIN as output, I(ANIN) = 2 mA			0.4	V
A/D Converter							
701	Ton	Converter initialization time	ENAD changes from 0 to 1			500	µs
702	Tconv	Conversion time				140	µs
703	RES(ADC)	A/D Converter Resolution				10	bit
704	RAC	Relative Accuracy		-1		+1	LSB
705	VZS()	Zero Scale Voltage	ADC(9:0) = 0x000		0		V
706	VFS()	Full Scale Voltage	ADC(9:0) = 0x3FF	1.0	1.1	1.2	V
707	VDDM()	VDD Measurement	VDD=3.3 V, ADCC(2:0)= 000	334	368	402	LSB
708	VBLM()	VBL Measurement	VBL=24 V, ADCC(2:0) = 001	654	720	786	LSB
709	VBM()	VB Measurement	VB=24 V, ADCC(2:0) = 010	654	720	786	LSB
710	MDLM()	MDL Measurement	|V(MD)-V(MR)|=0.5 V, ADCC(2:0) = 011	413	455	497	LSB
711	MCM()	V(MCH)-V(MCL)Measurement	V(MCH) < 3 V, V(MCH)-V(MCL)=0.25 V, CGAIN(1:0)=000 ADCC(2:0) = 100	400	441	482	LSB
712	VRNM()	VRN Measurement	VRN=VBL=VB= 12 V, ADCC(2:0) = 101	330	365	402	LSB
713	VRPM()	VRP Measurement	VRP = 24 V, ADCC(2:0) = 110	658	724	790	LSB
714	ANINM()	ANIN Measurement	ANIN = 0.5 V, ADCC(2:0) = 111	409	451	493	LSB
Overtemperature							
B01	Toff	Overtemperature Shutdown	Rising temperature	130		170	°C
B02	Ton	Overtemperature Release	Falling temperature	120		160	°C
B03	Thys	Hysteresis	Toff – Ton	3			°C
Temperature Monitor							
C01	Trange	Temperature Measurement Range		-40		125	°C
C02	Tresol	Temperature Measurement Resolution			1		°C
C03	TEMP	Temperature Value Ranges	Tj = 60 °C Tj = 0 °C	100 40		125 60	LSB LSB
DCO Output							
D01	Isc()hi	DCO Output Current	V(VDD) = 3...3.5 V, V(DCO) < 1.4 V, RDCO = 0x3F	-175	-130	-85	µA
D02	Ileak	Leakage Current at DCO	RDCO = 0x00 or NSTBY = lo, V(DCO) = 0 . . . 5.5 V	-1		1	µA
D03	I(DCO)LSB	I(DCO) Resolution	V(DCO) < 1.4 V	1.3	2	2.7	µA
Oscillator							
E01	F(osc)	Oscillator Frequency	NSTBY = hi	100	200	400	kHz
E02	T(CFGTIMO)	Configuration Mode Timeout	MODE(1:0) = 10	40	82	164	ms
E03	tWDT	Watchdog Timeout	NSTBY = hi	20		120	µs

OPERATING REQUIREMENTS: SPI and I²C Interface

Operating Conditions: VB = 3 . . . 24 V , Tj = -40 . . . 85 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI / I²C Interface Timing						
I001	tsCCL	Setup Time: NCS/A1 hi → lo before SCLK lo → hi	INS = lo	20		ns
I002	tsDCL	Setup Time: MOSI/A0 stable before SCLK/SCL lo → hi	INS = lo	20		ns
I003	thDCL	Hold Time: MOSI/A0 stable after SCLK/SCL lo → hi	INS = lo	5		ns
I004	tCLH	Signal Duration SCLK/SCL hi	INS = lo INS = hi	5 1250		ns ns
I005	tCLL	Signal Duration SCLK/SCL lo	INS = lo INS = hi	5 1250		ns ns
I006	thCLC	Hold Time: NCS/A1 lo after SCLK/SCL lo → hi	INS = lo	5		ns
I007	tCSH	Signal Duration NCS/A1 hi	INS = lo	20		ns
I008	tpCLD	Propagation Delay: MISO/SDA stable after SCLK/SCL hi → lo	V(VDD) > 3 V, Cload = 10 pF, no external pull-up	0	30	ns
I009	f(SCLK)	SPI clock frequency			10	MHz
I010	f(SCL)	I²C clock frequency			400	kHz

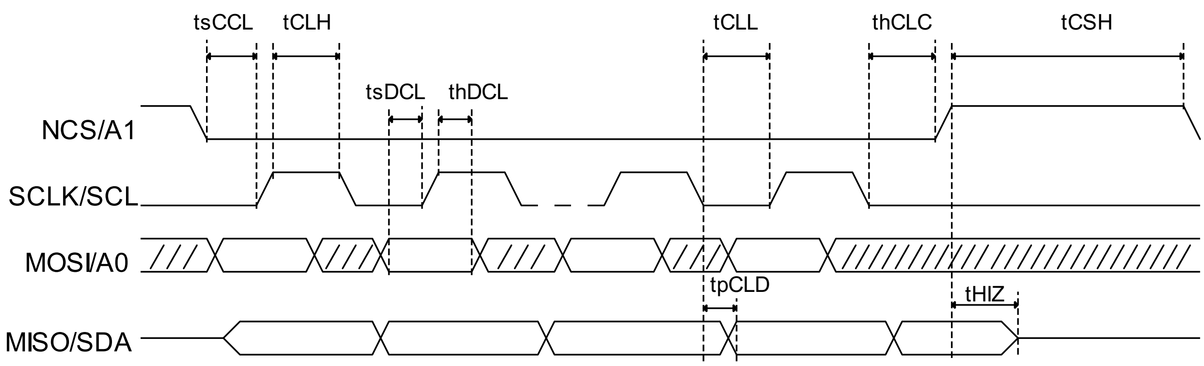


Figure 1: SPI / I²C interface timing

STANDBY

iC-HTG enters standby mode by setting pin NSTBY low. If in standby mode and no current is drained from pin VDD, the current consumption at VB is reduced to e.g. max. 10 µA (cf. *Electrical Characteristics No. 002*), and the chip retains its RAM configuration.

In order to exit standby mode, pin NSTBY must be set to hi (e.g. the supply voltage at VB). VDD is switched off in standby mode and can not be used to exit standby mode.

After wake-up (pin NSTBY's rising edge), the internal regulated supply voltage at VDD returns to its nominal value at a rate depending on the capacitor connected to the VDD pin (cf. *Electrical Characteristics No. 504*).

More information about the start-up procedure is available on page 29

OPERATION MODE

iC-HTG has two main modes: configuration mode and operation mode. The mode can be set with register MODE(1:0).

MODE(1:0)	Addr. 0x1C; bit 1:0 R/W 01
00	Not allowed, signaled as memory error
01	Chip set in operation mode (apply configuration, latch transparent)
10	Chip set in configuration mode (hold previous configuration)
11	Not allowed, signaled as memory error

Table 5: Select configuration or operation mode

The configuration of the internal parameters of iC-HTG must occur in configuration mode. Several parameters can be configured using a microcontroller via I^{2}C or SPI communication. In this mode, the configuration memory can be written and read back without changing the previous configuration state of iC-HTG. Once the configuration is verified and accepted as valid, iC-HTG can be switched to operation mode and the configuration will be activated. More information about configuration and operation modes, and the serial communication interface can be found on pages 28 and 17, respectively.

In operation mode, the driver can be enabled by setting pin EC to hi. Setting register bit DISC to '1' disables the driver. If either pin EC is low or or register bit DISC is high, the laser is disabled.

DISC	Addr. 0x10; bit 3 R/W 1
0	Channel can be enabled by pin EC
1	Channel cannot be enabled by pin EC

Table 6: Disable channel

The iC-HTG can be configured in two control modes: laser-light power-control (APC) and the laser current control (ACC). The control mode is selected by setting EACC register. More about control modes is on page 13

EACC	Addr. 0x10; bit 0 R/W 0
0	APC mode enabled (laser power control)
1	ACC mode enabled (laser current control)

Table 7: Select APC or ACC

Laser enabling and error handling
Setting register bit DISC to '0' enabled the laser channel.

The input pin INS needs to be high or low. With an open floating INS pin a corresponding internal error signal is generated (INSOPEN).

Internal INSOPEN error signal and Status errors shown in figure 2 disable the laser channel. Every change in the STATUS0 or STATUS1 registers is signaled at pin NCHK, unless the error event is masked by the corresponding error mask bit.

Register	Address	Bits	Default	Description
INITRAM	0x00	0	R/O	RAM initialized
PDOVDD	0x00	1	R/O	Power down event at VDD
MEMERR	0x00	2	R/O	RAM memory validation error
OVT	0x00	3	R/O	Overtemperature event
PDOVBL	0x00	4	R/O	Power down event at VBL
OVC	0x00	5	R/O	Overcurrent
OSCERR	0x00	6	R/O	Oscillator error (watchdog set)
CFGTIMO	0x00	7	R/O	Configuration mode timeout event
MAPC	0x01	0	R/O	Channel current state read back
MONC	0x01	1	R/O	Channel enabled at least once (latched)
EC	0x01	2	R/O	EC pin current state read back
NMCOK	0x01	3	R/O	Current feedback status

Table 8: Status registers overview

In order to enable the channel, the error events must be acknowledged. Acknowledging an error is accomplished by reading the corresponding STATUS register. After a power-on, PDOVDD and INITRAM errors will be set, therefore it is required to read the registers STATUS0 and STATUS1 after each power-on.

Exiting standby mode does not reset the RAM, but does set the PDOVDD status bit. Therefore STATUS0 must be read once after each standby to re-enable the laser channel.

In case of an overcurrent (OVC) or an overtemperature (OVT) event, the laser channel is disabled.

A memory error event (MEMERR) or a configuration timeout error event (CFGTIMO) also disables the laser channel. More information about the memory error is on page 28. The conditions to enable the laser channel are shown in Figure 2.

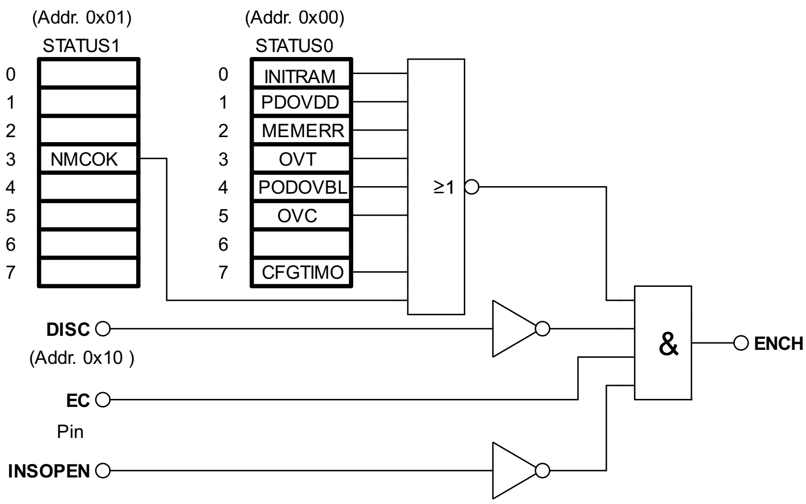


Figure 2: Laser control logic

CONTROL MODES AND LASER DIODE/LED TYPES

The iC-HTG has no integrated driver transistor. External power transistor (P-channel or N-channel) can be driven, connecting the gate of the transistor to pins VRP or VRN. Another possibility is to control a DC/DC converter directly, providing the best power efficiency. The on-chip regulator has an offset-cancelling feature, which can be controlled with register bit EOC (see table below).

EOC	Addr. 0x10; bit 4	R/W 1
0	Regulator offset compensation disabled	
1	Regulator offset compensation enabled	

Table 9: Enable offset compensation

The iC-HTG can be configured in two main control modes: laser power control (APC) and laser current control (ACC). The control mode is selected by setting EACC register bit.

EACC	Addr. 0x10; bit 0	R/W 0
0	APC mode enabled (laser power control)	
1	ACC mode enabled (laser current control)	

Table 10: Select APC or ACC

CI capacitor
For most applications, a CI capacitor of at least 220 pF is recommended in order to ensure the stability of the regulation. The exact amount of capacitance needed depends on many factors such as PCB layout, output transistor, laser diode, and current range. The CI capacitor can be used in APC and ACC.

ACC mode
In ACC mode, the laser current is controlled. ACC mode is selected by setting EACC register bit to '1'. In this mode, an external shunt resistor (RMC) is used to monitor the laser diode current. The voltage drop across this shunt resistor serves as feedback to the laser current control loop. To insert the current voltage drop in the control loop, both pins of the shunt resistor must be connected to the pins MCH and MCL. The voltage drop MCx = V(MCH)-V(MCL) needs to be positive. This voltage drop is internally amplified by a factor of 2, 5, 10 or 50. This factor can be selected using the register CGAIN(1:0). The resistor has to be chosen so that the value of the voltage drop multiplied by the amplification factor does not exceed the higher value of the reference generated with the 10-bit logarithmic D/A converter. This value is typically 1 V. More about this is on page 20

CGAIN(1:0)	Addr. 0x15; bit 7:6	R/W 00
00	Amplification set to x2	
01	Amplification set to x5	
10	Amplification set to x10	
11	Amplification set to x50	

Table 11: MCx voltage drop amplification

Depending on the output configuration and the position of RMC in the current path, the voltage between pins MCH and MCL will be in between 0 and 5 V or in the range from VBL - 5 V to VBL. The MCx voltage range can be set with the register bit MCVR.

MCVR	Addr. 0x13; bit 2	R/W 0
0	MCx Voltage Range is 0 to 5V	
1	MCx Voltage Range is VBL-5V to VBL	

Table 12: MCx voltage range

In ACC mode, the register EPNNP is ignored.

Some examples of connecting RMC using N-channel and P-channel transistor are shown in Figure 3.

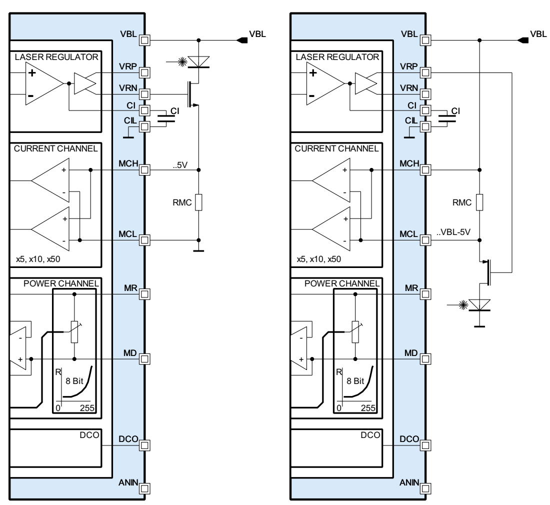


Figure 3: Operation in ACC mode with N-channel or P-channel output transistor. EACC=1, MCVR=0 and MCVR=1

By using the output transistor like in Figure 3, as a source follower, the system has increased stability, and the CI capacitor can be smaller. This is recommended for analog modulation with pin MOD. There are many other configurations possible depending on laser type, transistor, and voltage range. More information about this can be found on page 35.

ACC mode monitoring the optical power

In ACC mode, the optical power can be measured using a laser with an integrated photodiode (N-type or P-type). Connecting the photodiode to pin MD, a proportional voltage to the photocurrent can be measured with the 10-bit linear A/D converter. Two examples of driving in ACC mode using a laser with integrated photo diodes are shown in Figure 4. More examples of configuration for this application can be found on page 35. Depending on the type of laser, N or P, the register bit EPNNP has to be set to '0' or '1', respectively.

EPNNP	Addr. 0x13; bit 7	R/W 0
0	N-type laser	
1	P-type laser	

Table 13: Enable P-laser or N-laser type

The optical power can be measured when the photocurrent is induced in a resistor, producing a voltage drop as shown in Figure 4. The internal 8-bit programmable logarithmic resistor PLR (more information about the PLR on page 19) can be used. If an external resistor is desired, it must be connected to pins MD and MR, and the internal resistor PLR must be disconnected, by setting register bit DISP to '1'.

DISP	Addr. 0x10; bit 2	R/W 0
0	PLR enabled	
1	PLR disabled	

Table 14: Enable/disable PLR

To measure the optical power, the register ADCC(2:0) has to be set to 0b011. Thus, the internal voltage MDL $= |V_{MD} - V_{MR}|$ will be selected as an input for the 10-bit A/D converter.

ADCC(2:0)	Addr. 0x10; bit 7:5	R/W 000
000	ADC sourced by $V(VDD) \div 8$ (3V .. 5.5V)	
001	ADC sourced by $V(VBL) \div 30$ (3V .. 24V)	
010	ADC sourced by $V(VB) \div 30$ (3V .. 24V)	
011	ADC sourced by $V(MDL)$ (0V .. 1.1V)	
100	ADC sourced by $V(MC)$ (0V .. 1.1V)	
101	ADC sourced by $V(VRN) \div 30$ (0V .. 24V)	
110	ADC sourced by $V(VRP) \div 30$ (0V .. 24V)	
111	ADC sourced by $V(ANIN)$ (0V .. 1.1V)	

Table 15: ADC source selection

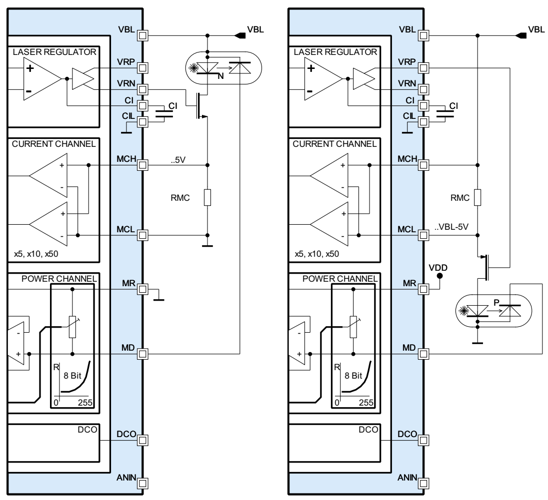


Figure 4: Example of ACC monitoring the optical power EACC=1. In the left setup MCRV=0 and EPNNP=0 while in the right setup, MCVR=1 and EPNNP=1

APC mode

In APC mode, the laser power is controlled. APC mode is selected by setting EACC register bit to '0'. In this mode, the monitor diode current is used as feedback in the laser power control loop. To introduce the monitor diode current in to the feedback control loop pins MR and MD are used. An internal, 8-bit programmable logarithmic monitor resistor (PLR) can be used in APC mode and is controlled by register RMD(7:0). It is also possible to use an external monitor resistor connected to pins MR and MD. If register bit DISP is '0', the PLR is present. If DISP is '1', the PLR is disabled and an external monitor resistor must be used. The PLR feature a wide logarithmic resistor range from 100 Ω to 500 kΩ, in steps of typically 3.3%. This covers a wide range of monitor currents. More information about the PLR can be found on page 19.

For fine-tuning the optical power, the reference voltage is set with a 10-bit logarithmic D/A converter, which is configurable using register REF(9:0).

REF(9:8) **REF(7:0)**	Addr. 0x13; bit 1:0 Addr. 0x14; bit 7:0	R/W 0x000 R/W 0x000
0x000	Regulator reference voltage set to minimum voltage	
...	Regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$, n from 0 to 1023	
0x3FF	Regulator reference voltage set to maximum voltage	

Table 16: Channel regulator voltage reference

This converter has a voltage range that goes typically from Vref0=0.1 V to Vrefmax=1.1 V, allowing an operation resolution of typically ΔVref=0.235%. More information on the logarithmic D/A converted can be found on page 20. For calculating the minimum value for the monitor feedback current (Imon), Vref(0x00, max value) (cf. *Electrical Characteristics No. 303*) and Rmda(RMDx = 0xFF, min value) (cf. *Electrical Characteristics No. 201*) are used.

$$Imon(min) = \frac{Vref(0x000,max)}{Rmda(RMDx=0xFF,min)} = \frac{0.11}{350000} = 0.31\,uA$$

To calculate the maximum value of Imon, Vref(0x3FF, min value) (cf. *Electrical Characteristics No. 303*) and Rmda(RMD(7:0) = 0x00, max value) (cf. *Electrical Characteristics No. 201*) are used. The following formula is used to calculate Rmda(RMD(7:0) = 0x00, max value):

$$Imon(max) = \frac{Vref(0x3FF,min)}{Rmda(RMD=0x00,max)} = \frac{1.00}{280} = 3.5\,mA$$

Any other Imon value can be calculated using the Rmd formula above. Due to its logarithmic characteristic, the steps between two consecutive values is kept typically within 3.3 % of the nominal value. This formula provide only an approximated value of the resistor. Because of the coupling factor between laser and photodiode, and the parametric variation of the PLR, each system hast to be calibrated separately.

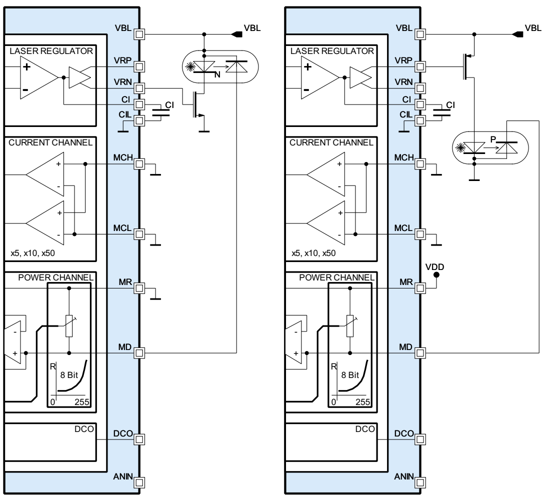


Figure 5: APC with N-channel and P-channel output transistor using N-type and P-type laser diodes. EACC=0, MCVR=0, EPNNP=0 for N-type lasers or EPNNP=1 for P-type lasers

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iC-HTG is optimized for driving P-type and N-type laser diodes. Figure 5 shows two examples of driving P-type and N-type laser diodes using APC mode. More examples of possible configurations can be found on page 35.

APC mode monitoring the laser current

In APC mode, there is the possibility to monitor the laser current using the 10-bit linear A/D converter and/or to use the overcurrent monitor function. More about overcurrent on page 16. To measure the optical power, a shunt resistor must be connected to pins MCH/MCL and the register ADCC(2:0) has to be set to 0b100.

ADCC(2:0)	Addr. 0x10; bit 7:5 R/W 000
000	ADC sourced by *V(VDD)* ÷ 8 (3V .. 5.5V)
001	ADC sourced by *V(VBL)* ÷ 30 (3V .. 24V)
010	ADC sourced by *V(VB)* ÷ 30 (3V .. 24V)
011	ADC sourced by *V(MDL)* (0V .. 1.1V)
100	ADC sourced by *V(MC)* (0V .. 1.1V)
101	ADC sourced by *V(VRN)* ÷ 30 (0V .. 24V)
110	ADC sourced by *V(VRP)* ÷ 30 (0V .. 24V)
111	ADC sourced by *V(ANIN)* (0V .. 1.1V)

Table 17: ADC source selection

Thus, the internal voltage MC=V(MCH)-V(MCL) will be selected as an input for the 10-bit A/D converter.

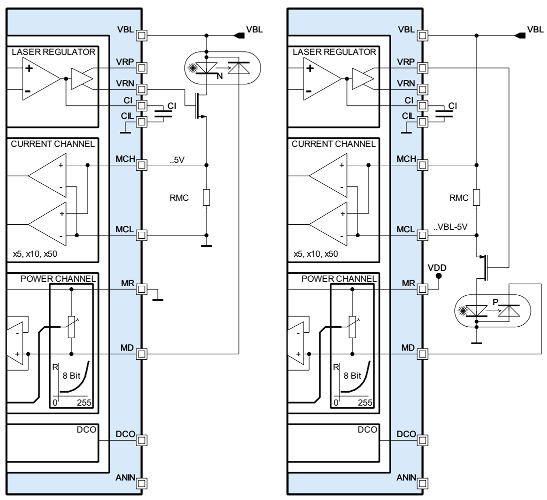

Figure 6: Example of APC monitoring the laser current. EACC=0. Left setup:MCRV=0, EPNNP=0. Right setup MCVR=1, EPNNP=1

More configuration examples can be found on page 35.

Other functions

For some special applications (for example with low VB/VBL) it is useful to drive VRN up to VBL. In this case, the register bit VRNHR has to be set to ’1’. The default and recommended value is setting the register bit VRNHR to '0'.

VRNHR	Addr. 0x13; bit 4	R/W 0
0	VRN set from 0V to VBL-1V	
1	VRN set from 1V to VBL	

Table 18: VRN voltage range

Some applications might need an extra amplification stage after VRN/VRP with inversion of the polarity of the control. For such application, the register bit NSW is to be set to '0' and the polarity of the controller inverted.

NSW	Addr. 0x13; bit 6	R/W 1
0	Inverted regulation mode (reference connected to regulator's negative input)	
1	Standard regulation mode (reference connected to regulator's positive input)	

Table 19: CI regulator reference Swap

OVERCURRENT MONITOR

A programmable overcurrent shutdown can be set to protect the laser by disabling the channel. If the voltage drop at the external shunt resistor V(MCH)-V(MCL) is higher than the programmed value the overcurrent signal, OVC, is set and the laser channel is disabled. The maximum voltage drop at the shunt resistor can be programmed using the register ILIM(7:0).

ILIM(7:0)	Addr. 0x11; bit 7:0	R/W 0x00
0x00	Overcurrent detection disconnected.	
0x01	Minimum value of V(MCH)-V(MCL) set to minimum value typ. (0.1V/CGAIN)	
...		
0xFF	Maximum value of V(MCH)-V(MCL) set to maximum value typ. (1.1V/CGAIN)	

Table 20: ILIM overcurrent register

An overcurrent event can be simulated using SOVC. If SOVC = 1, and the overcurrent detection is enabled (ILIM not set to 0x00), the corresponding overcurrent error bit OVC is set to 1, the error is signaled at NCHK, and the laser channel is disabled. The overcurrent error will remain forced until SOVC = 0.

SOVC	Addr. 0x16; bit 5	R/W 0
0	No overcurrent event is simulated.	
1	Overcurrent event simulated.	

Table 21: Simulate overcurrent

WATCHDOG TIMER

The internal 200 kHz oscillator is monitored with the Watchdog Timer (WDT).

If the oscillator remains longer than the maximum time of tWDT (cf. *Electrical Characteristics No. E03*) without activity, an oscillator error is triggered. An oscillator error sets OSCERR error bit to '1'. The automatic offset compensation of the laser control (see page 13) requires the oscillator.

The state of OSCERR is signaled at pin NCHK. The signaling of OSCERR state can be masked with bit MOSCERR. Setting MOSCERR to '1' masks the oscillator error and in this case OSCERR is not signaled at NCHK.

It is possible to simulate an error of the oscillator using SOSCERR bit. If SOSCERR = 1, the oscillator error is forced. When OSCERR is set to '1', the error is signaled through NCHK depending on the state of MOSCERR.

OSCERR	Addr. 0x00; bit 6	R
0	Oscillator functioning OK	
1	Watchdog timeout set on oscillator failure. Cleared on read	

Table 22: Oscillator watchdog

MOSCERR	Addr. 0x16; bit 0	R/W 0
0	Oscillator error (watchdog) will be signaled at NCHK	
1	Oscillator error (watchdog) will not be signaled at NCHK	

Table 23: Oscillator watchdog error mask

SOSCERR	Addr. 0x16; bit 7	R/W 0
0	No oscillator error simulated.	
1	Oscillator error simulated (watchdog timeout).	

Table 24: Simulate oscillator error

SERIAL COMMUNICATION INTERFACES

Communication modes

iC-HTG can be configured via a serial interface. It has two communication modes: SPI and I²C. Selection of the communication protocol is achieved using pin INS: INS = hi for I²C, INS = lo for SPI. If the pin INS is found to be open, NCHK will be pulled to 0.

SPI slave interface

The SPI slave interface is enabled by setting pin INS to lo and the interface uses pins NCS/A1, SCLK/SCL, MISO/SDA and MOSI/A0. The pin NCS/A1 is the chip select pin and must be set lo by the SPI master in order to start communication. The pins MISO/SDA and MOSI/A0 are the data communication lines and pin SCLK/SCL is the clock line generated by the SPI master (e.g. a microcontroller). The SPI protocol frames are shown in Figure 7.

A communication frame consists of one address byte and at least one data byte. The bits 7:6 of the address byte are the opcode used for selecting a read operation (set to "10") or a write (set to "01") operation. The remaining 6 bits are used for register addressing.

It is possible to transmit several bytes consecutively if the NCS signal is not reset and SCLK/SCL keeps clocking, as is shown in Figure 7. The address is internally incremented after each transmitted byte. Once the address reaches the last register (0x3F), it is reset back to 0x00.

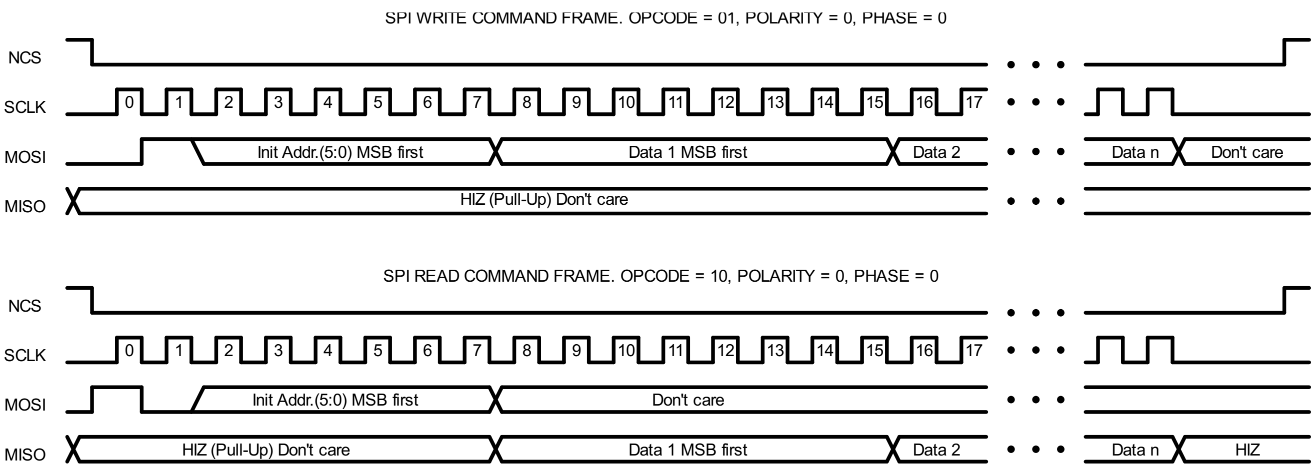

Figure 7: SPI commands

I²C slave interface

The I²C slave interface is enabled by setting pin INS to hi and the interface uses pins NCS/A1, SCLK/SCL, MISO/SDA, ID, and MOSI/A0. The protocol frames are shown in Figure 8.

Action	b7	b6	b5	b4	b3	b2	b1	b0
Write to slave	1	0	1	0	ID	A1	A0	0
Read from slave	1	0	1	0	ID	A1	A0	1

Table 25: I²C write/read byte

A communication frame consists of one slave address byte, one register address byte, and at least one data byte. The bits 7:1 of the slave address byte are build form the slave identification code (ID) and the address bit A1 and A0. The bit 0 is used to specify the data direction (RNW: 1 for read, 0 for write).

The four most significant bits are fixed by default to the value 0b1010. The pins MOSI/A0, NCS/A1, and ID are used to set the remaining slave ID bits (see Tables 25 and 26).

Action	ID	A1	A0	Slave ID	Command byte
Write to slave 0	lo	lo	lo	0x50	0xA0
Read from slave 0	lo	lo	lo	0x50	0xA1
Write to slave 1	lo	lo	hi	0x51	0xA2
Read from slave 1	lo	lo	hi	0x51	0xA3
Write to slave 2	lo	hi	lo	0x52	0xA4
Read from slave 2	lo	hi	lo	0x52	0xA5
Write to slave 3	lo	hi	hi	0x53	0xA6
Read from slave 3	lo	hi	hi	0x53	0xA7
Write to slave 4	hi	lo	lo	0x54	0xA8
Read from slave 4	hi	lo	lo	0x54	0xA9
Write to slave 5	hi	lo	hi	0x55	0xAA
Read from slave 5	hi	lo	hi	0x55	0xAB
Write to slave 6	hi	hi	lo	0x56	0xAC
Read from slave 6	hi	hi	lo	0x56	0xAD
Write to slave 7	hi	hi	hi	0x57	0xAE
Read from slave 7	hi	hi	hi	0x57	0xAF

Table 26: I^2C write/read command byte

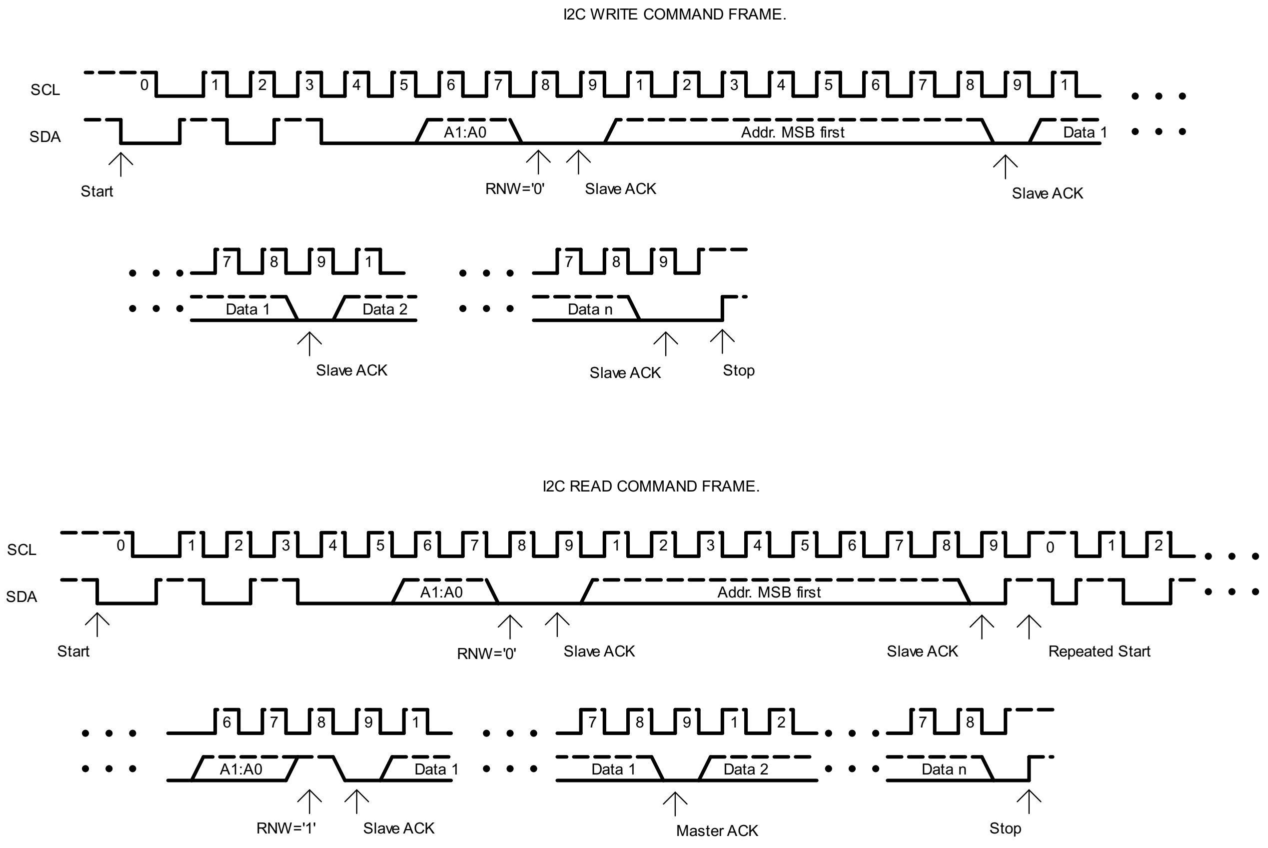

Figure 8: I^2C commands

8-BIT INTERNAL PROGRAMMABLE LOGARITHMIC MONITOR RESISTORS

An internal 8-bit Programmable Logarithmic monitor Resistor (PLR) is provided for the APC.

The PLR is used to control the optical power of the laser diode in APC mode or to measure a monitor photocurrent in ACC mode using the internal A/D converter. The resistor is connected to pins MR and MD using a Force Sense switch structure. This ensures a low thermal dependence, and a monotone dependence on the resistor with the register value RMD(7:0). Note that measuring of the internal resistor directly at external pins MD-MR is not possible (see Figure 9).

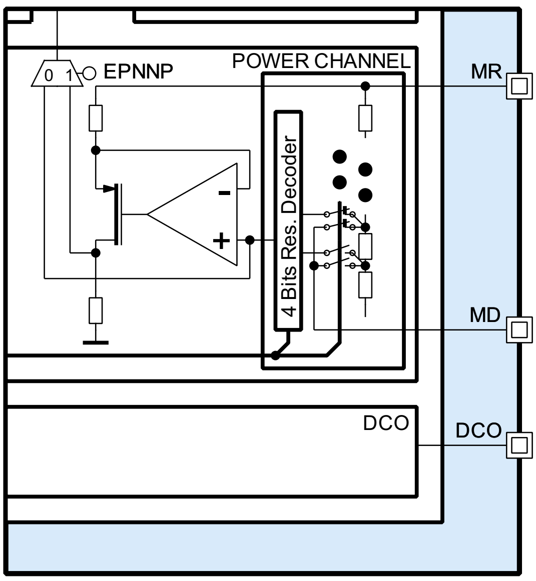

Figure 9: PLR internal node regulation

The internal resistor value can be selected from 256 values, ranging from typ. Rmd0=100 Ω to over 500 kΩ, following logarithmic increments with a typical step width of ΔRmd=3.3%. The resistors are configured with register RMD(7:0).

RMD(7:0)	Addr. 0x12; bit 7:0	R/W 0xFF
0x00	PLR set to the minimum resistance	
...	PLR set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$, n from 0 to 255	
0xFF	PLR resistor set to the maximum resistance	

Table 27: MR-MD resistance selection

The following formula calculates the register RMD(7:0) in order to set the desired resistor value:

$$Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}, : n \in [0, 255],$$

where Rmd_0 is the minimum resistor value (typically 100 Ω), $\Delta Rmd(\%)$ is the step between two consecutive resistor values (typically 3.3%) and n is the value of RMD(7:0) register in decimal.

Since the PLR has parametric variations and covers a wide range of resistors values, the given formula is only for simulation or information purposes. Each system has to be calibrated separately. The recommended procedure is to enable the channel with a high value of RMD(7:0) and a medium value on register REF(9:0). While measuring the optical power reduce the PLR value until the desired optical power is reached. Then using the register REF(9:0) you can make a more accurate selection of the optical power. For more information see 13.

The PLR is disabled by using the register bit DISP.

DISP	Addr. 0x10; bit 2	R/W 0
0	PLR enabled	
1	PLR disabled	

Table 28: Enable/disable PLR

In ACC mode the PLR is not used in the control circuit. Even though the PLR is not in the control circuit, it can be enabled (DISP = 0) in order to give feedback using the 10-bit A/D converter to control the light power if a monitor diode is connected.

Alternatively, an external monitor resistor can be used to measure the optical power, which requires DISP to be set to '1'.

10-BIT LOGARITHMIC D/A CONVERTER

The 10-bit logarithmic D/A converter is used for setting the regulator's voltage reference. The D/A converter is active in all operating modes. With a range from 0.1 to 1.1 V and the typical step width is ΔVref=0.235%. (Maximal ΔVref=1%) This ensures that with each LSB step there is a maximum variation of 1% of the optical power.

The D/A converter is configured using register REF(9:0). With REF(9:0) = 0x000, the D/A output value is set to 0.1 V, and for REF(9:0) = 0x3FF the D/A output is configured to 1.1 V.

REF(9:8)	Addr. 0x13; bit 1:0	R/W 0x000
REF(7:0)	Addr. 0x14; bit 7:0	R/W 0x000
0x000	Regulator reference voltage set to minimum voltage	
...	Regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$, n from 0 to 1023	
0x3FF	Regulator reference voltage set to maximum voltage	

Table 29: Channel regulator voltage reference

To calculate the D/A converter value for each REF(9:0) value, use the following equation:

$$V_{ref} = V_{ref0}(1 + \frac{\Delta V_{ref}(\%)}{100})^{n+1} : n \in [0, 1023],$$

where $Vref_0$ is the minimum value (typically 0.1 V), $\Delta Vref(\%)$ is the step value (typically 0.235 %) and n is the value of REF register in decimal.

Since the D/A has parametric variations, the given formula is only for simulation or information purposes. Each system has to be calibrated separately. The recommended procedure in APC mode is to enable the channel with a high value of RMD(7:0) and a medium value on register REF(9:0). While measuring the optical power, reduce the PLR value until the desired optical power is reached. Then using the register REF(9:0) you can make a more accurate selection of the optical power. For ACC mode is recommended to enable the laser with register value REF(9:0)=0xFF. While measuring the optical power, reduce the value of the register REF(9:0) until reaching the desired optical power. For more information see 13.

10-BIT LINEAR A/D CONVERTER

A 10-bit linear A/D converter is available for a variety of voltages that can be measured with different resolutions:

- V(VDD) up to 5.5 V with 8.6 mV resolution
- V(VBL) up to 30 V with 32.3 mV resolution
- V(VB) up to 30 V with 32.3 mV resolution
- V(MDL) internal voltage up to 1.1 V with 1.075 mV resolution
- V(MC) internal voltage up to 1.1 V with 1.075 mV resolution
- V(VRN) up to 30 V with 32.3 mV resolution
- V(VRP) up to 30 V with 32.3 mV resolution
- V(ANIN) up to 1.1 V with 1.075 mV resolution

As described in block diagram on Page 1, the voltages V(VDD), V(VBL), V(VB), V(VRN), V(VRP) and V(ANIN) are th PIN Voltage directly. V(MC) is proportional to the laser current value and is the voltage difference between pins MCH and MCL. (V(MC)=V(MCH)-V(MCL)). The voltage V(MDL) is proportional to the optical laser power (monitor current) and the value is the absolute value of the difference between the pins MD and MR (V(MDL)=|V(MD)-V(MR)|).

The register ADCC(2:0) select the signal measured with the 10-bit A/D converter.

ADCC(2:0)	Addr. 0x10; bit 7:5	R/W 000
000	ADC sourced by $V(VDD) \div 8$ (3V .. 5.5V)	
001	ADC sourced by $V(VBL) \div 30$ (3V .. 24V)	
010	ADC sourced by $V(VB) \div 30$ (3V .. 24V)	
011	ADC sourced by $V(MDL)$ (0V .. 1.1V)	
100	ADC sourced by $V(MC)$ (0V .. 1.1V)	
101	ADC sourced by $V(VRN) \div 30$ (0V .. 24V)	
110	ADC sourced by $V(VRP) \div 30$ (0V .. 24V)	
111	ADC sourced by $V(ANIN)$ (0V .. 1.1V)	

Table 30: ADC source selection

When enabled, the A/D converter continuously acquires the signal selected by ADCC register. The conversion time is 140 µs. Changing the source requires 500 µs settling time.

The converter does not provide an end of conversion (EOC) bit, the ADC(9:0) register always contains the value of the last valid conversion.

As the A/D converter has a resolution of 10 bits, the results are split into two, one byte wide, separate registers; ADCh contains ADC MSBs values while ADCl stores the LSBs. A consecutive read of both registers (lower and upper part) should be carried out in order to prevent an undesired change in the measured value between two read commands.

ADC(9:8) **ADC(7:0)**	Addr. 0x03; bit 1:0 Addr. 0x04; bit 7:0	R R
0x000 ... 0x3FF	ADC minimum value ADC maximum value	

Table 31: ADC

The voltage corresponding to the measured digital value can be directly obtained using the following formula:

$$V(VBL, VB, VRP, VRN) = 30 * \frac{VFS}{1024} * ADCx$$

$$V(VDD) = 8 * \frac{VFS}{1024} * ADCx$$

$$V(MDL, MC, ANIN) = \frac{VFS}{1024} * ADCx$$

VFS is the full scale voltage of the A/D converter (cf. *Electrical Characteristics No. 706*) typically 1.1 V. For a more precise measurement, the A/D converter can be calibrated by measuring a known VB voltage and calculating the VFS.

ANIN GENERAL PURPOSE IO PIN

The Pin ANIN is a general purpose IO-Pin. Figure 10 describe the functionality of pin ANIN.

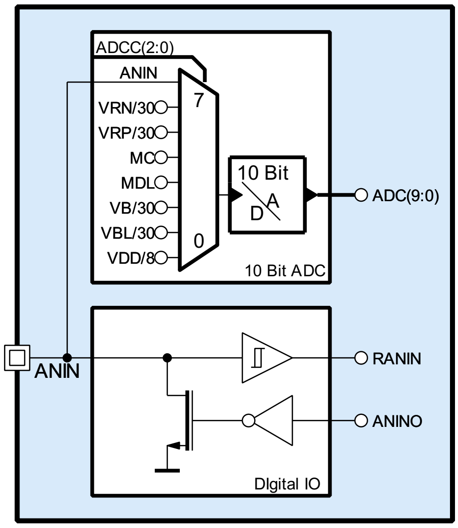

Figure 10: ANIN pin function description

With the pin ANIN an external analog Voltage from 0V to 1.1V can be digitalized using the 10 bit linear A/D converter. To this end, register bit ANINO has to be set to 1 and the register ADCC(2:0) has to be set to value 0x07. For the digitalisation of higher voltages a resistor divider is recommended. An example of measuring voltages up to 24V is shown in figure 13.

ANIN can be used as a digital open collector output. As digital output an external Pull-Up resistor needs to be used. The maximum allowed voltage at pin ANIN is 5V. With register bit ANINO the state of ANIN will be set.

ANINO	Addr. 0x1C; bit 2 R/W 1
0	ANIN pin pulled low (open collector)
1	ANIN pin set to high impedance

Table 32: ANIN output state

RANIN	Addr. 0x01; bit 4 R
0	ANIN pin is digital low at the precise reading moment.
1	ANIN pin is digital high at the precise reading moment.

Table 33: ANIN pin state

As digital TTL input the Pin ANIN is mapped to status Register Bit RANIN.

DC/DC CONVERTER OPTIMIZATION

iC-HTG provides a 6-bit configurable current source at pin DCO that can be used to trim the output voltage of a DC/DC converter. Current at DCO can be programmed with register RDCO(5:0). Possible application benefits with using DCO include:

- DC/DC step down operation: regulation at voltages lower than power supply
- DC/DC step up operation: regulation at voltages higher than power supply
- Efficiency enhancement

RDCO(5:0)	Addr. 0x15; bit 5:0 R/W 0x00
0x00	No current
...	
0x3F	130 µA Typ (see spec point D01)

Table 34: DCO current control

The proposed applications can be demonstrated with a standard DC/DC converter, e.g. TPS63060DSC from Texas Instruments. This converter allows an input voltage ranging from 2.5 V to 12 V and offers an output voltage from 2.5 V to 8 V. It is capable of delivering up to 2 A current, depending on the output voltage. Figure 11 shows a possible configuration.

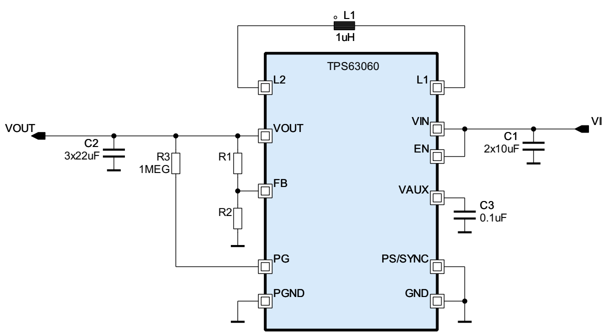

Figure 11: TPS63060 DC/DC converter from TI

DC/DC step down operation: regulation at voltages lower than power supply

The resistors R1 and R2 in the feedback path allow setting the desired output value Vout. The DC/DC converter drives Vout pin in order to yield 0.5 V at feedback pin FB. The DCO output signal from iC-HTG is connected to FB pin. The Vout is controlled with the internal register RDCO(5:0) from iC-HTG.

The DCO current into FB node controls the voltages of the divider R1 and R2, and Vout changes in order to maintain 0.5 V at the pin FB. When selecting R1 and R2, one needs to consider:

- Resistors values: $R1 = R2(\frac{Vout}{Vfb} - 1)$
- The current of the voltage divider should be high enough in comparison to the current from the pin DCO to offer acceptable resolution. The programmable current resolution of register RDCO(5:0) is 2 µA.
- The DCO current into the voltage divider lowers the voltage Vout. Vout is 8 V when no current is present at DCO.

Choosing R1 = 100 kΩ, the value of R2 can be calculated:

$$R2 = \frac{R1}{\frac{Vout}{Vfb} - 1} = \frac{100k}{\frac{8V}{0.5V} - 1} = 6.7\,\text{k}\Omega$$

With this configuration, the current through the voltage divider is 75 µA at 8 V . The resolution of each RDCO(5:0) step is then 200 mV.

The value in RDCO(5:0) register needed in order to have the desired output voltage can be calculated using the following formula:

$$RDCO = \frac{Idco}{2uA} = \frac{IR2 - IR1}{2uA} = \frac{\frac{0.5V}{6.7k} - \frac{Vout - 0.5V}{100k}}{2uA}$$

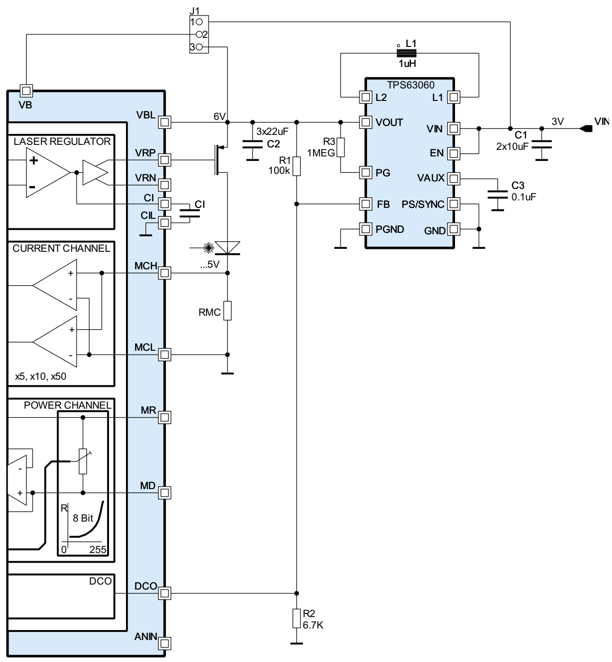

Figure 12: Regulation of VB / VBL Supply using DCO

The resulting value varies slightly depending on the tolerances of the selected resistors and the DCO current. iC-HTG incorporates an internal 10-bit A/D converter.

Selecting VBL or VB as input of this converter the supply voltage can be measured and the selected current at DCO can be changed in order to obtain the desired voltage at VBL/VB. Setting register ADCC(2:0) to 0b001 or 0b010, the supply voltages VBL or VB can be measured, respectively. The digitalized value is the supply value divided by 30.

DC/DC step up operation: regulation at voltages higher than power supply

A practical application of the present case is the control of blue lasers. This type of laser presents a forward voltage around 5 V, which demands a voltage of about 6 V for the anode of the laser diode (LDA). If the system is supplied with a 3 V LiPo battery, it is necessary to use a DC/DC in order to step up and drive the laser diode and driver with a sufficient voltage. Figure 12 shows this application. Jumper J1 can be set to 1-2 or 2-3 position.

Typically setting register RDCO(5:0) to 10 it delivers 20 µA and 6 V, which are obtained at Vout.

Extension of system working voltage range
iC-HTG may be supplied with a voltage within the threshold values of 3 V and 24 V. It is possible to control the DC/DC output in a voltage range of 2.5 to 24 V if the DC/DC converter controlled by the DCO output signal is included in the system, as it is shown in Figure 12.

In Figure 12 both the laser and iC-HTG are supplied with output voltage Vout from DC/DC converter. Typically, the register RDCO(5:0) is set to 23, which forces 48 µA to be output to the voltage divider. A system voltage of 3.3 V is obtained at Vout.

Efficiency enhancement
If iC-HTG and the laser diode are supplied with the same power supply, the efficiency of the driver can be improved depending on the supplied voltage, the saturation voltage, and the laser diode forward voltage. The power dissipation of the driver transistor can be reduced if VBL is set through the DC/DC converter configured to deliver a voltage lower than the power supply as shown in Figure 13.

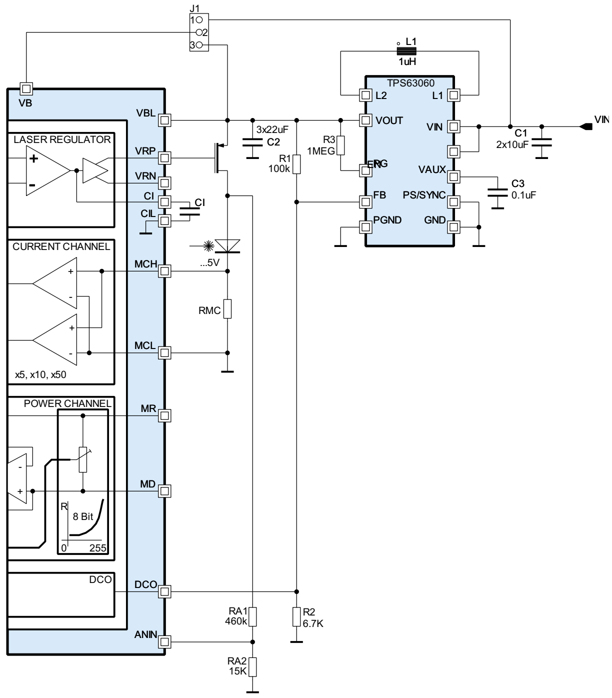

Figure 13: System efficiency enhancement

For this application the pin ANIN must be configured as an input by setting the register bit ANINO to 1. Using the resistors RA1 and RA2, the drain voltage at the drive transistor is reduced by a factor of approximately 30. For more information about ANIN see page 22.

ANINO	Addr. 0x1C; bit 2	R/W 1
0	ANIN pin pulled low (open collector)	
1	ANIN pin set to high impedance	

Table 35: ANIN output state

In this configuration, the voltage drop at the driver transistor can be measured and minimized by setting an appropriate supply at VBL. Some steps have to be done to optimize the power dissipation:

- A. Measure the voltage at pin VBL, setting the register ADCC(2:0) to 0b001. The measured voltage AD(VBL) is divided by a factor of 30.
- B. Measure the voltage at pin ANIN. AD(ANIN)
- C. The voltage drop at the driver transistor is (AD(VBL)-AD(ANIN))*30. By changing the DCO(6:0) register, the supply voltage at V(VBL) can be increased or decreased. ANIN should remain constant.
- D. Repeat steps A to C to achieve the desired voltage drop at the output transistor.

ANALOG MODULATION

iC-HTG allows analog modulation of the output current at a frequency of up to 50 kHz. An external modulation voltage source (sinusoidal, triangular, etc) must be provided and connected to pin MOD. The internal control loop forces the laser diode current to follow the modulation voltage signal. This feature is enabled by setting register bit ENAM high.

ENAM	Addr. 0x13; bit 3	R/W 0
0	Analog modulation disabled	
1	Analog modulation enabled	

Table 36: Enable analog modulation

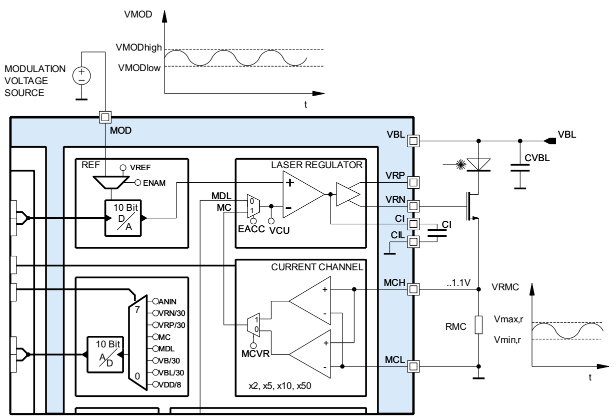

Figure 14: Recommended configuration for analog modulation using N-channel transistor. EACC=1, MCVR=0

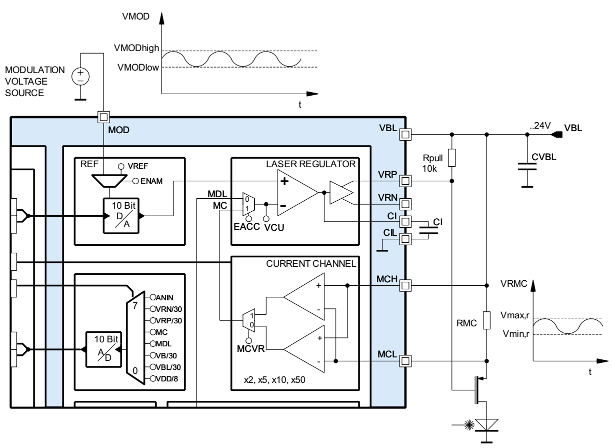

Figure 15: Recommended configuration for analog modulation using P-channel transistor. EACC=1, MCVR=1

The maximum allowed modulation frequency is 50 kHz, but general performance depends on the external capacitor connected at CI, the value of the RMC, the current gain selected (CGAIN(1:0)), and the total gate capacity of the external transistor.

To ensure a higher stability, the configuration shown in Figure 15 is recommended (See Figure 19 left from Examples of configuration on page 35). CGAIN(1:0) must be kept as low as possible, increasing the value of the RMC if necessary. For 50 kHz modulation figure 15 is recommended with values of CI from 100pF to 300pF.

Setting Current Modulation

The modulation current is set by 4 factors:

- The modulation voltage amplitude at MOD.
- The digital-to-analog converter setpoint REF(9:0)
- The external sense resistor RMC.
- Current Channel gain CGAIN(1:0).

With the analog modulation VREF is no more a DC voltage for the regulator but a voltage divider for the V(MOD) voltage to downscale AC and DC voltages for the regulator. The V(MOD) voltage contains a DC voltage part and a AC voltage part to define the required operation point with the parameter set.

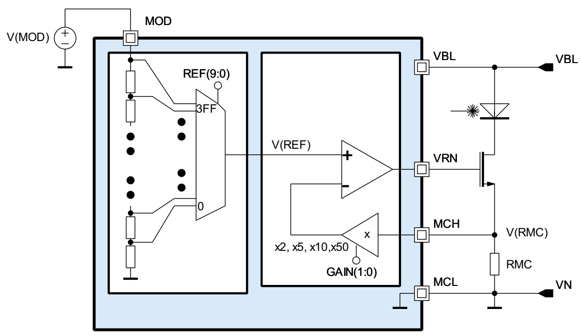

Figure 16: Signal path of the analog modulation

It is not recommended to use lower values that 100mV for V(VREF). For lower voltages the accuracy of the regulation and the frequency response are not guaranteed. Therefore, V(MOD) must be selected according to the REF(9:0) dividing factor to ensure V(VREF) higher or equal to 0.1 V.

For a first estimate of the values, the equation (1) and (2) can be used. In this equation REFx can be 1 to 1023 and CGAINx can take the values 2, 5, 10 and 50.

(1) $V(RMC) = \frac{VMOD}{1023} \cdot \frac{REFx}{CGAINx}$

(2) $I(RMC) = \frac{VMOD}{1023} \cdot \frac{REFx}{CGAINx} \cdot \frac{1}{RMC}$

With this equation the theoretical current value can be calculated. More accurate calculations can be made using the parameters 302 303 and 304 of the Electrical Characteristics and the equation (3) and (4)

(3) $V(RMC) = \frac{VMOD}{1.1} \cdot \frac{V(REF)}{G()}$

(4) $I(RMC) = \frac{VMOD}{1.1} \cdot \frac{V(REF)}{G()} \cdot \frac{1}{RMC}$

Due to the parameter variation is recommended to calibrate each circuit. The recommended procedure to set the current modulation values is:

1. Set the GAINx(1:0) value. (0x00 is recommended)
2. Set a reference value of voltage in V(MOD). For example a low voltage or a DC voltage (VMODdc) in a sinus signal as shown in figure 17
3. With fixed voltage at V(MOD) (for example VMODdc), use REF(9:0) to set the desired V(RMC) (In this case V(RMCdc) for current laser (I(RMCdc)). You can use the internal AD-Converter to sense the voltage at RMC.

   Note that using the equation the laser current I(RMCdc) is:

   (5) $I(RMCdc) = \frac{VMODdc}{1.1} \cdot \frac{V(REF)}{G()} \cdot \frac{1}{RMC}$
4. With this setup the relationship between the voltage at V(MOD) and the referenced current is given by (7):

(6) $I(RMChigh) = \frac{VMODhigh}{1.1} \cdot \frac{V(REF)}{G()} \cdot \frac{1}{RMC}$

(7) $\frac{I(RMChigh)}{I(RMCdc)} = \frac{VMODhigh}{VMODdc}$

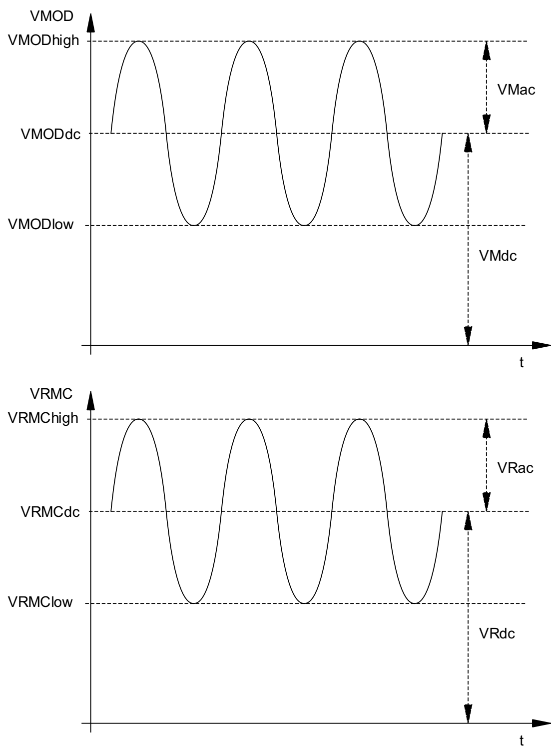

Figure 17: Example of modulation voltages

TEMPERATURE MONITOR AND PROTECTION

iC-HTG includes an 8-bit temperature monitor that allows to measure the internal chip temperature going from -40 to 125 °C. The resolution is 1 °C/LSB.

TEMP(7:0)	Addr. 0x02; bit 7:0 R
0x00	Minimum temperature
...	
0xFF	Maximum temperature

Table 37: Chip temperature

Absolute read values may differ from one chip to another. An individual initial calibration of the temperature monitor is recommended. The TEMP register must be read at a known temperature. Using the resolution value of 1 °C/LSB, the internal temperature can be calculated.

The temperature monitor can be used to compensate temperature effects on the laser diode. The microcontroller can use a laser diode characteristic formula or a look-up table combined with the temperature value measured using TEMP register. The reference voltage can be configured accordingly in order to compensate for temperature effects.

iC-HTG is protected against overtemperature. If the internal temperature exceeds a safety value, an overtemperature error bit (OVT) is set to 1. If OVT = 1, the laser channel is disabled, and the error event is signaled through NCHK pin. The error bit OVT is latched, and can only be cleared by reading the status register.

The overtemperature threshold value can not be configured.

OVT	Addr. 0x00; bit 3 R
0	No overtemperature event has occurred since last read
1	Overtemperature event has occurred. Cleared on read

Table 38: Overtemperature

It is possible to simulate an overtemperature event using the SOVT bit. Setting SOVT to 1, the overtemperature error flag OVT is set to 1. iC-HTG remains in the error state until SOVT is set back to 0.

SOVT	Addr. 0x16; bit 4 R/W 0
0	No overtemperature event is simulated.
1	Overtemperature event simulated.

Table 39: Simulate overtemperature

CONFIGURATION MODE AND MEMORY INTEGRITY MONITOR

iC-HTG supports the interfaces SPI or I^{2}C, which are selected by the INS pin. More information about the serial communication interface can be found on page 17

In the configuration mode the iC-HTG configuration can amended without affecting the configuration stored in the iC-HTG RAM. Only when switching back to the operation mode, the configuration is applied to the iC-HTG in an atomic operation (all at once).

Integrity monitoring is implemented by a duplication of the configuration registers into a validation page (see description below) where the registers are automatically copied with their inverted value. Every register bit is compared with its validation copy and, in case of inconsistency, a memory error is generated in such a case the laser channel is switched off.

Atomic appliance is achieved by latching the configuration registers. This permits a full configuration (different registers) to be made prior to apply it to the laser channel.

The configuration mode is selected by setting the register MODE(1:0) to 10.

MODE(1:0)	Addr. 0x1C; bit 1:0 R/W 01
00	Not allowed, signaled as memory error
01	Chip set in operation mode (apply configuration, latch transparent)
10	Chip set in configuration mode (hold previous configuration)
11	Not allowed, signaled as memory error

Table 40: Select configuration or operation mode

In **Configuration mode**, the *configuration memory* (addr. 0x10 to 0x1F) can be written and read back to check a correct communication without changing the present configured operation state of the iC-HTG. In this mode, the memory integrity check is disabled.

iC-HTG will monitor the time elapsed in configuration mode and automatically switch the laser off if it exceeds a configuration mode timeout. The time in configuration mode must be less than 40 ms to ensure that no configuration timeout occurs during configuration (cf. *Electrical Characteristics No. E02*).

When writing the configuration is completed, iC-HTG is switched to **operation mode** by writing "01" into the MODE register (addr. 0x1C). In **operation mode** the configuration is applied to the iC-HTG and the memory integrity check activated. In this mode configuration registers can only be read (except MODE(1:0) register, which is always accessible). Figure 18 shows the interface to the memory structure.

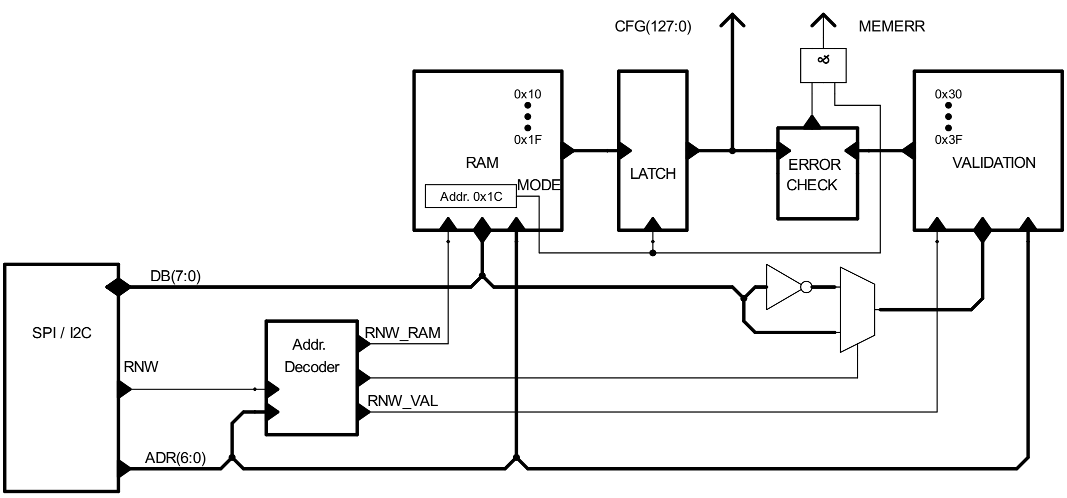

Figure 18: Interface, RAM integrity monitoring, and configuration latching

Register map description
The register map consists of 64 addresses subdivided in three different pages:

- Read-only page, addr. 0x00 to 0x0F: iC-HTG status, ADC readout, thermometer readout and chip revision.

- Configuration page (integrity monitored), read--write registers, addr. 0x10 to 0x1F.
- Validation page, read-write registers, addr. 0x30 to 0x3F.

Read-only registers with values or states
The Read-only registers are sub-divided into status registers (addr. 0x00 to 0x01) and measurement registers and the chip revision register CHIPREV. Status registers are normally latched to 1 on events and cleared on read (see individual register description). Measurement registers are dual-port and can be accessed simultaneously with the measurements in progress. ADC (addr. 0x03 to 0x04) is a 10-bit register split into two 8-bit registers and must be accessed in block mode (automatic address increment) to ensure data do not change during the read.

Configuration page (integrity monitored)
The configuration page (addr. 0x10 to 0x1F) contains the registers that control the driver. Every write operation to any of the registers of this page will be internally duplicated to the correspondent register at the validation page. After the write operation, the correspondent validation register contains the inverted value of the configuration register.

Validation page
The validation page (addr. 0x30 to 0x3F) can be read or written normally. Only when a write procedure is made to any of the configuration registers, the correspondent validation pair will be written with the inverted value of the configuration register as well.

Both the configuration and validation pages are initialized during power-up. This event is signaled at the STATUS0 register (bit 0, INITRAM). In standby mode (NSTBY = lo) the RAM is not reset if any write command has been executed and therefore configuration and validation pages keep the stored information and INITRAM remains unset. Entering standby mode after power-up without any write command, the RAM will be initialized again and the INITRAM bit will be set to 1 again. Any VDD power-down event signaled at the STATUS0 register outside the standby mode (NSTBY = hi) requires a RAM content check regardless of the state of the INITRAM bit to ensure data is not corrupted.

Possible start-up sequence:

1. iC-HTG starts in operation mode with default configuration. INITRAM and PDOVDD error bits are set in STATUS0, DISC (addr. 0x10, bit 3) is set to 1.
2. Write MODE(1:0) = "10" register (addr. 0x1C) to enable the configuration mode.
3. Configure the laser channel.
4. Read back to verify a correct data transfer.
5. Set the DISC bit to 0.
6. Read the status registers (addr. 0x00, 0x01) to detect possible errors and validate status. At any error: read again to ensure that the error is valid.
7. Write MODE(1:0) = "01" register (addr. 0x1C) to apply the configuration and enable the memory integrity check.
8. During operation: monitor the status registers, checking for errors. The NCHK pin signals any set status bit if not masked. This pin can be used to trigger an microcontroller interrupt line.

REGISTER OVERVIEW

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00 R	CFGTIMO	OSCERR	OVC	PDOVBL	OVT	MEMERR	PDOVDD	INITRAM
0x01 R	0	0	0	RANIN	NMCOK	EC	MONC	MAPC
0x02 R	TEMP(7:0)							
0x03 R							ADC(9:8)	
0x04 R	ADC(7:0)							
0x05 R								
0x06 R								
0x07 R	Not implemented							
...	Not implemented							
0x0F R	CHIPREV							
0x10	ADCC(2:0)			EOC	DISC	DISP	ENAD	EACC
0x11	ILIM(7:0)							
0x12	RMD(7:0)							
0x13	EPNNP	NSW	0	VRNHR	ENAM	MCVR	REF(9:8)	
0x14	REF(7:0)							
0x15	CGAIN(1:0)		RDCO(5:0)					
0x16	SOSCERR		SOVC	SOVT			MMONC	MOSCERR
0x17	Reserved							
0x18	Not implemented							
0x19	Not implemented							
0x1A	Not implemented							
0x1B	Not implemented							
0x1C	Not implemented					ANINO	MODE(1:0)	
0x1D	Not implemented							
0x1E	Reserved register. Set to zero							
0x1F	Reserved register(Factory test). Set to zero							
0x20	Not implemented							
...	Not implemented							
0x30	Validation content for 0x10, inverted							
0x31	Validation content for 0x11, inverted							
...	...							
0x3F	Validation content for 0x1F, inverted							

Table 41: Register layout

PARAMETERS

Register	Address	Bits	Description
INITRAM	0x00	0	RAM initialized.
PDOVDD	0x00	1	Power-down event at VDD
MEMERR	0x00	2	RAM memory validation error
OVT	0x00	3	Overtemperature event
PDOVBL	0x00	4	Power-down event at VBL
OVC	0x00	5	Overcurrent
OSCERR	0x00	6	Oscillator error (watchdog set)
CFGTIMO	0x00	7	Configuration mode timeout event
MAPC	0x01	0	Channel state
MONC	0x01	1	Channel enabled at least once (latched)
EC	0x01	2	EC pin digital state
NMCOK	0x01	3	MCL, MCH voltage status
RANIN	0x01	4	ANIN pin digital state

Table 42: Status overview

Register	Address	Bits	Description
TEMP	0x02	7:0	Chip temperature measurement
ADCh	0x03	1:0	ADC 9:8 readout
ADCl	0x04	7:0	ADC 7:0 readout
CHIPREV	0x0F	7:0	Chip revision identification

Table 43: Measurement overview

Status

INITRAM	Addr. 0x00; bit 0	R
0	RAM not initialized since last read	
1	RAM initialized. Cleared on read	

Table 44: RAM initialization

PDOVDD	Addr. 0x00; bit 1	R
0	VDD power down not occurred since last read	
1	VDD power down event has occurred. Cleared on read	

Table 45: VDD power down

MEMERR	Addr. 0x00; bit 2	R
0	RAM has not been changed since last validation	
1	RAM has changed and has not been validated	

Table 46: Memory validation

OVT	Addr. 0x00; bit 3	R
0	No overtemperature event has occurred since last read	
1	Overtemperature event has occurred. Cleared on read	

Table 47: Overtemperature

PDOVBL	Addr. 0x00; bit 4	R
0	VBL power down not occurred since last read	
1	VBL power down event has occurred. Cleared on read	

Table 48: VBL power down

OVC	Addr. 0x00; bit 5	R
0	No overcurrent event has occurred since last read	
1	Overcurrent event has occurred. Cleared on read	

Table 49: Overcurrent

OSCERR	Addr. 0x00; bit 6	R
0	Oscillator functioning OK	
1	Watchdog timeout set on oscillator failure. Cleared on read	

Table 50: Oscillator watchdog

CFGTIMO	Addr. 0x00; bit 7	R
0	iC-HTG not in *configuration mode* or *timeout* did not happened till now	
1	iC-HTG in *configuration mode* and *timeout* happened. Laser switched off.	

Table 51: Configuration timeout

MAPC	Addr. 0x01; bit 0	R
0	Channel is off at the precise reading moment	
1	Channel is on at the precise reading moment	

Table 52: Channel state

MONC	Addr. 0x01; bit 1	R
0	Channel has not been switched on since last read	
1	Channel has been switched on at least once. Cleared on read	

Table 53: Channel state history

EC	Addr. 0x01; bit 2	R
0	EC pin is high at the precise reading moment.	
1	EC pin is low at the precise reading moment.	

Table 54: EC pin state

NMCOK	Addr. 0x01; bit 3	R
0	MCH-MCL voltage is OK for the selected laser type.	
1	MCH-MCL voltage is not OK for the selected laser type.	

Table 55: MCH-MCL voltage status

RANIN	Addr. 0x01; bit 4	R
0	ANIN pin is digital low at the precise reading moment.	
1	ANIN pin is digital high at the precise reading moment.	

Table 56: ANIN pin state

TEMP(7:0)	Addr. 0x02; bit 7:0	R
0x00	Minimum temperature	
...		
0xFF	Maximum temperature	

Table 57: Chip temperature

CHIPREV	Addr. 0x0F; bit 7:0	R
18	iC-HTG Z	
19	iC-HTG Z1	
20	iC-HTG Y	
21	iC-HTG Y1	

Table 58: Chip revision

Channel configuration registers

EACC	Addr. 0x10; bit 0	R/W 0
0	APC mode enabled (laser power control)	
1	ACC mode enabled (laser current control)	

Table 59: Select APC or ACC

ENAD	Addr. 0x10; bit 1	R/W 0
0	AD Converter disabled	
1	AD Converter enabled, source selected with ADCC	

Table 60: Enable ADC

DISP	Addr. 0x10; bit 2	R/W 0
0	PLR enabled	
1	PLR disabled	

Table 61: Enable/disable PLR

DISC	Addr. 0x10; bit 3	R/W 1
0	Channel can be enabled by pin EC	
1	Channel cannot be enabled by pin EC	

Table 62: Disable channel

EOC	Addr. 0x10; bit 4	R/W 1
0	Regulator offset compensation disabled	
1	Regulator offset compensation enabled	

Table 63: Enable offset compensation

ADCC(2:0)	Addr. 0x10; bit 7:5	R/W 000
000	ADC sourced by $V(VDD) \div 8$ (3V .. 5.5V)	
001	ADC sourced by $V(VBL) \div 30$ (3V .. 24V)	
010	ADC sourced by $V(VB) \div 30$ (3V .. 24V)	
011	ADC sourced by $V(MDL)$ (0V .. 1.1V)	
100	ADC sourced by $V(MC)$ (0V .. 1.1V)	
101	ADC sourced by $V(VRN) \div 30$ (0V .. 24V)	
110	ADC sourced by $V(VRP) \div 30$ (0V .. 24V)	
111	ADC sourced by $V(ANIN)$ (0V .. 1.1V)	

Table 64: ADC source selection

ILIM(7:0)	Addr. 0x11; bit 7:0	R/W 0x00
0x00	Overcurrent detection disconnected.	
0x01	Minimum value of V(MCH)-V(MCL) set to minimum value typ. (0.1V/CGAIN)	
...		
0xFF	Maximum value of V(MCH)-V(MCL) set to maximum value typ. (1.1V/CGAIN)	

Table 65: ILIM overcurrent register

RMD(7:0)	Addr. 0x12; bit 7:0	R/W 0xFF
0x00	PLR set to the minimum resistance	
...	PLR set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$, n from 0 to 255	
0xFF	PLR resistor set to the maximum resistance	

Table 66: MR-MD resistance selection

REF(9:8) REF(7:0)	Addr. 0x13; bit 1:0 Addr. 0x14; bit 7:0	R/W 0x000 R/W 0x000
0x000	Regulator reference voltage set to minimum voltage	
...	Regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$, n from 0 to 1023	
0x3FF	Regulator reference voltage set to maximum voltage	

Table 67: Channel regulator voltage reference

MCVR	Addr. 0x13; bit 2	R/W 0
0	MCx Voltage Range is 0 to 5V	
1	MCx Voltage Range is VBL-5V to VBL	

Table 68: MCx voltage range

ENAM	Addr. 0x13; bit 3	R/W 0
0	Analog modulation disabled	
1	Analog modulation enabled	

Table 69: Enable analog modulation

NSW	Addr. 0x13; bit 6	R/W 1
0	Inverted regulation mode (reference connected to regulator's negative input)	
1	Standard regulation mode (reference connected to regulator's positive input)	

Table 70: CI regulator reference Swap

EPNNP	Addr. 0x13; bit 7	R/W 0
0	N-type laser	
1	P-type laser	

Table 71: Enable P-laser or N-laser type

RDCO(5:0)	Addr. 0x15; bit 5:0	R/W 0x00
0x00	No current	
...		
0x3F	130 µA Typ (see spec point D01)	

Table 72: DCO current control

CGAIN(1:0)	Addr. 0x15; bit 7:6	R/W 00
00	Amplification set to x2	
01	Amplification set to x5	
10	Amplification set to x10	
11	Amplification set to x50	

Table 73: MCx voltage drop amplification

MOSCERR	Addr. 0x16; bit 0	R/W 0
0	Oscillator error (watchdog) will be signaled at NCHK	
1	Oscillator error (watchdog) will not be signaled at NCHK	

Table 74: Oscillator watchdog error mask

MMONC	Addr. 0x16; bit 1	R/W 1
0	Enable Channel will be signaled at NCHK	
1	Enable Channel will not be signaled at NCHK	

Table 75: Enable Channel (ENCH) monitor mask

SOVT	Addr. 0x16; bit 4	R/W 0
0	No overtemperature event is simulated.	
1	Overtemperature event simulated.	

Table 76: Simulate overtemperature

SOVC	Addr. 0x16; bit 5	R/W 0
0	No overcurrent event is simulated.	
1	Overcurrent event simulated.	

Table 77: Simulate overcurrent

SOSCERR	Addr. 0x16; bit 7	R/W 0
0	No oscillator error simulated.	
1	Oscillator error simulated (watchdog timeout).	

Table 78: Simulate oscillator error

MODE(1:0)	Addr. 0x1C; bit 1:0	R/W 01
00	Not allowed, signaled as memory error	
01	Chip set in operation mode (apply configuration, latch transparent)	
10	Chip set in configuration mode (hold previous configuration)	
11	Not allowed, signaled as memory error	

Table 79: Select configuration or operation mode

ANINO	Addr. 0x1C; bit 2	R/W 1
0	ANIN pin pulled low (open collector)	
1	ANIN pin set to high impedance	

Table 80: ANIN output state

EXAMPLES OF CONFIGURATION

ACC mode

Examples of ACC mode using P-channel transistor. Figures 19 and 20

Examples of ACC Mode using N-channel transistor. Figures 21 and 22

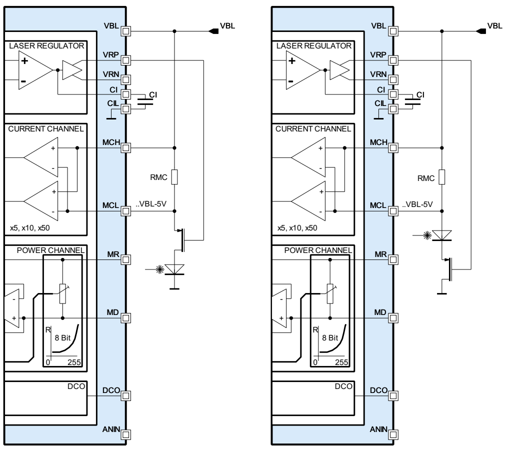

Figure 19: Working in ACC mode with P-channel output transistor as follower. (**Recommended**)

EACC	MCVR	EPNNP
1	1	-

Table 81: Register for Figure 19

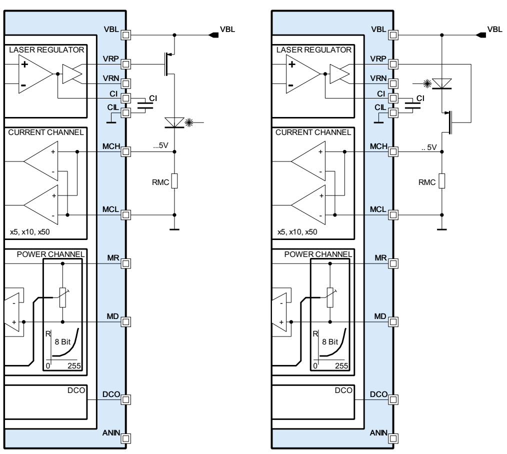

Figure 20: Working in ACC mode with P-channel output transistor

EACC	MCVR	EPNNP
1	0	-

Table 82: Register for Figure 20

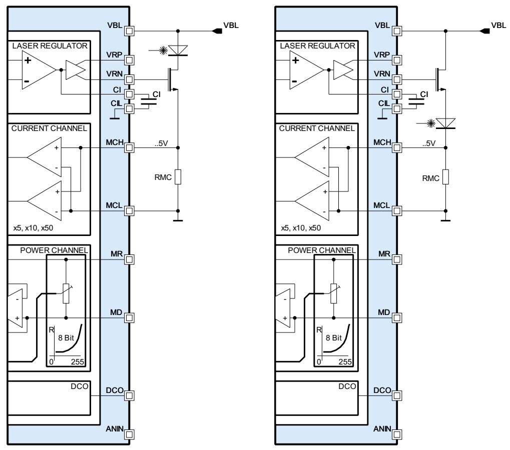

Figure 21: Working in ACC mode with N-channel output transistor as follower. (**Recommended**)

EACC	MCVR	EPNNP
1	0	-

Table 83: Register for Figure 21

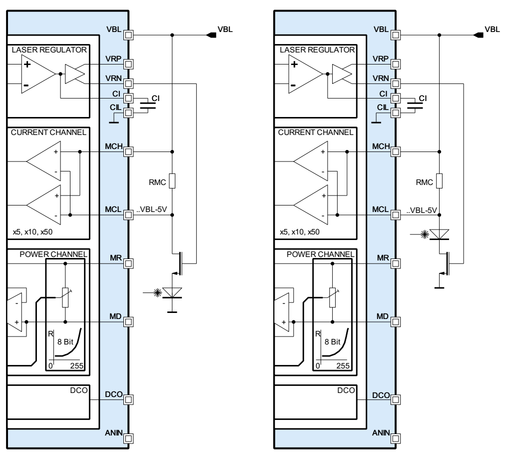

Figure 22: Working in ACC mode with N-channel output transistor.

EACC	MCVR	EPNNP
1	1	-

Table 84: Register for Figure 22

APC mode

Examples of APC mode using N-channel transistor. Figures 23 and 24.

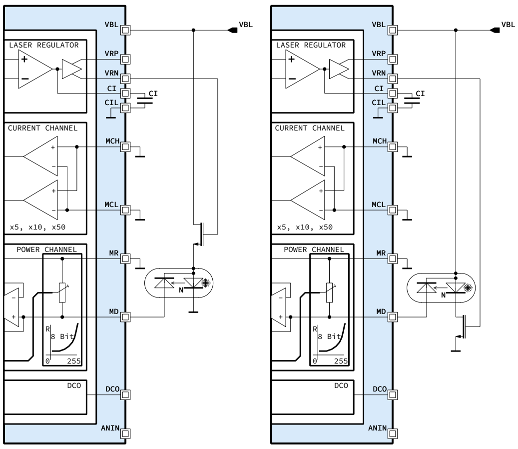

Figure 23: Working with N-channel output transistor and N-type laser diode.

EACC	MCVR	EPNNP
0	0	0

Table 85: Register for Figure 23

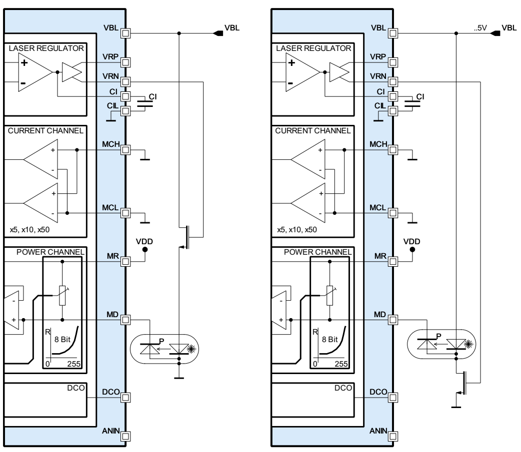

Figure 24: Working with N-channel output transistor and P-type laser diode.

EACC	MCVR	EPNNP
0	0	1

Table 86: Register for Figure 24

Examples of APC mode using P-channel transistor. Figures 25 and 26.

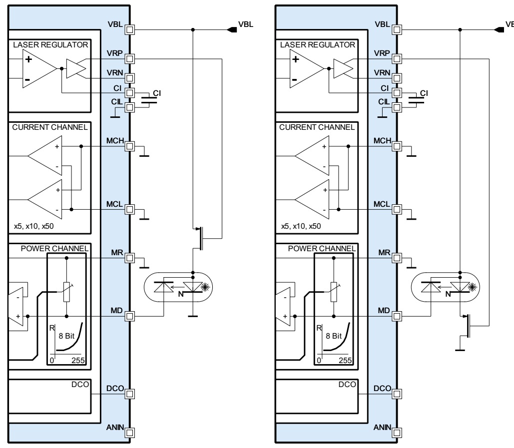

Figure 25: Working with P-channel output transistor and N-type laser diode.

EACC	MCVR	EPNNP
0	0	0

Table 87: Register for Figure 25

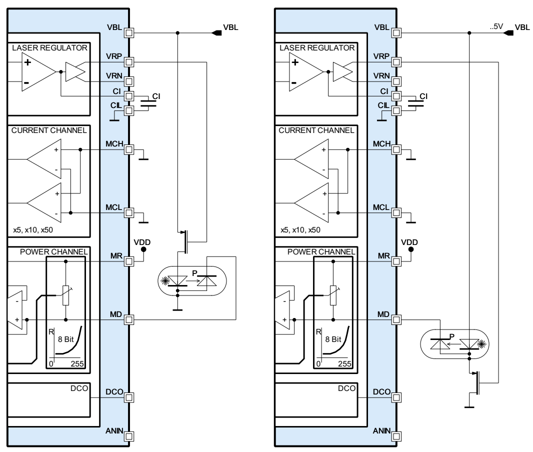

Figure 26: Working with P-channel output transistor and P-type laser diode.

EACC	MCVR	EPNNP
0	0	1

Table 88: Register for Figure 26

Note that in Figures 24 right and 26 right the VBL voltage is limited to 5 V.

APC mode with current monitor or ACC mode with optical power monitor

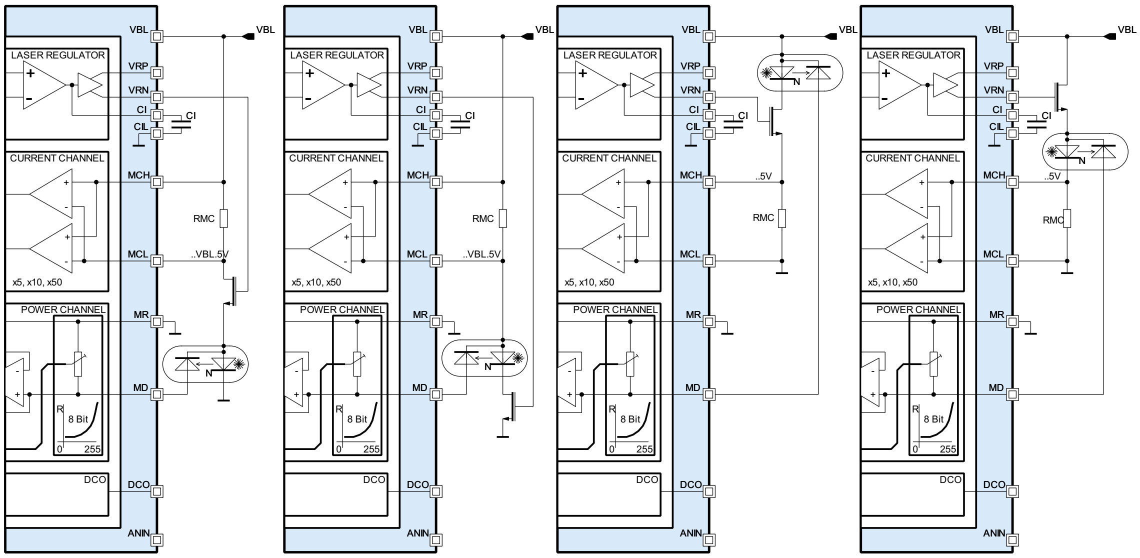

Figure 27: iC-HTG with N-channel output transistor and N-type laser diode.

Register	Figure 27.a	Figure 27.b	Figure 27.c	Figure 27.d	EACC	ADCC
MCVR	1	1	0	0	1	011
EPNNP	0	0	0	0	0	100

Table 89: Configuration register for Figure 27

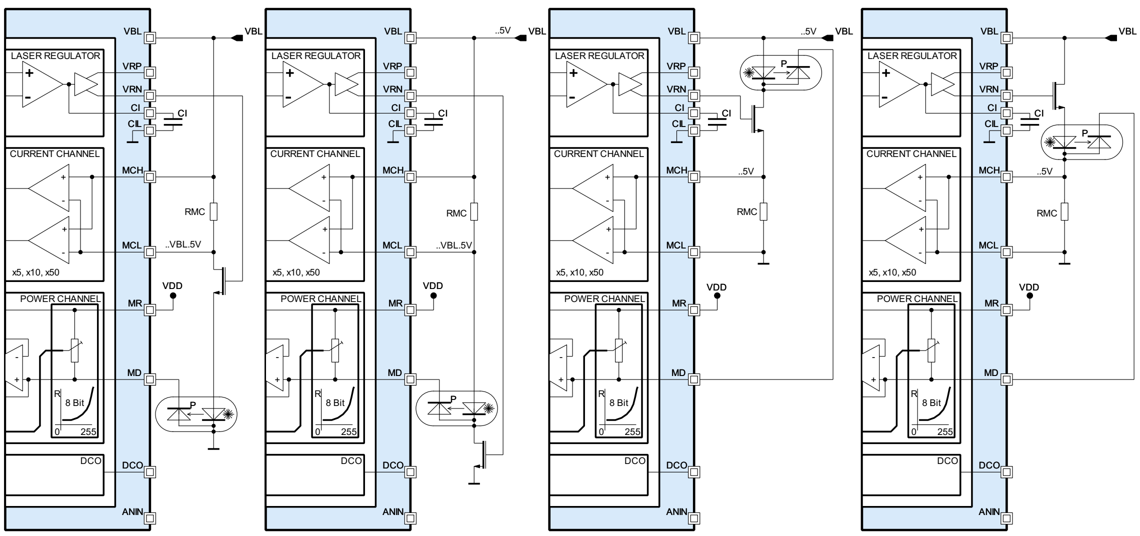

Figure 28: iC-HTG with N-channel output transistor and P-type laser diode

Register	Figure 28.a	Figure 28.b	Figure 28.c	Figure 28.d	EACC	ADCC
MCVR	1	1	0	0	1	011
EPNNP	1	1	1	1	0	100

Table 90: Configuration register for Figure 28

Note that in Figures 28.b and 28.c the VBL voltage is limited to 5 V.

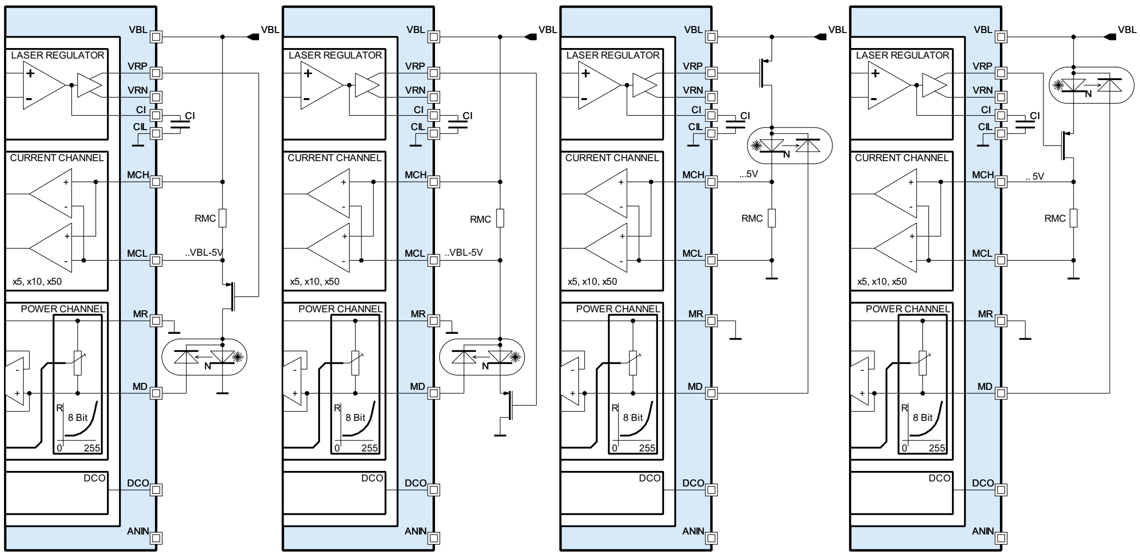

Figure 29: iC-HTG with P-channel output transistor and N-type laser diode.

Register	Figure 29.a	Figure 29.b	Figure 29.c	Figure 29.d	EACC	ADCC
MCVR	1	1	0	0	1	011
EPNNP	0	0	0	0	0	100

Table 91: Configuration register for Figure 29

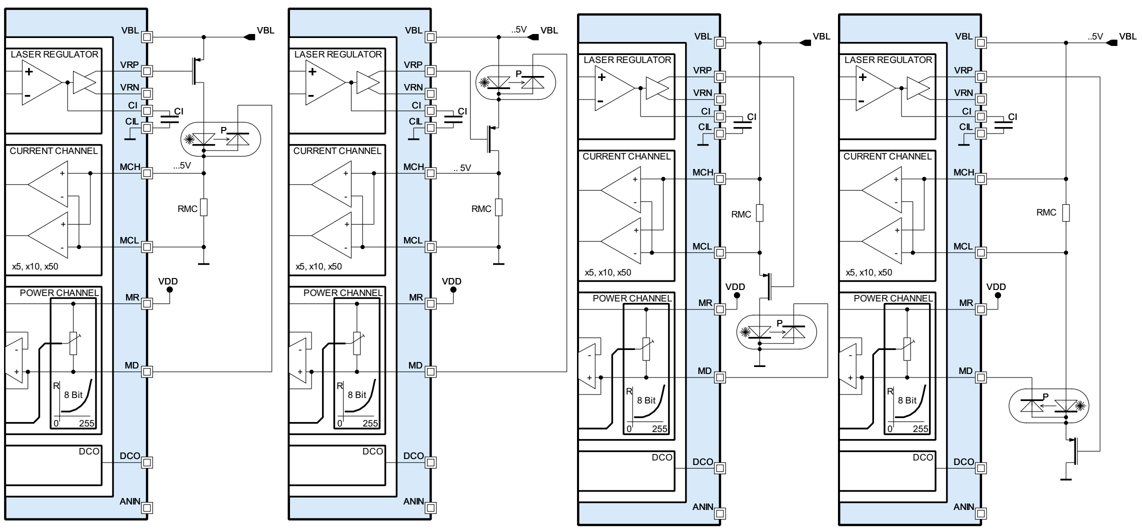

Figure 30: iC-HTG with P-channel output transistor and P-type laser diode

Register	Figure 30.a	Figure 30.b	Figure 30.c	Figure 30.d	EACC	ADCC
MCVR	0	0	1	1	1	011
EPNNP	1	1	1	1	0	100

Table 92: Configuration register for Figure 30

Note that in Figures 30.b and 30.d the VBL voltage is limited to 5 V.

DESIGN REVIEW: Notes On Chip Functions

iC-HTG Z, Z1		
No.	Function, Parameter/Code	Description and Application Notes
1	NEBUF	For iC-HTG chip releases Z and Z1 it is **NOT** recommended to use NEBUF = 0. Otherwise, proper operation of the control loop can not be guaranteed for all conditions. The parameter NEBUF does not exist anymore with iC-HTG chip release Y or higher. For iC-HTG chip releases see Table 58.

Table 93: Notes on chip functions regarding iC-HTG chip release Z and Z1.

REVISION HISTORY

Rel.	**Rel. Date***	**Chapter**	**Modification**	**Page**
A1	2017-11-24		Initial release	

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-HTG	QFN24 4 mm x 4 mm	iC-HTG QFN24-4x4
Evaluation Board	100 mm x 80 mm eval board	iC-HTG EVAL HTG1D

Please send your purchase orders to our order handling team:

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