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NTE74LS139
Integrated Circuit
TTL – Dual 2–Line–to–4–Line Decoder/Demultiplexer

Description:

The NTE74LS139 is a dual 2–line–to–4–line decoder/multiplexer in a 16–Lead plastic DIP type package designed to be used in high–performance memory decoding or stat–routing applications requiring very short propagation delay times. In high–performance memory systems this device can be used to minimize the effects of system decoding. When employed with high–speed memories utilizing a fast enable circuit the delay times of the decoder and the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky–clamped system decoder is negligible.

The circuit comprises two individual two–line to four–line decoders in a single package. The active–low enable input can be used as a data line in demultiplexing applications.

The NTE74LS139 features fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high–performance Schottky diodes to suppress line–ringing and to simplify system design.

Features:

- Designed Specifically for High–Speed:
  Memory Decoders
  Data Transmission Systems
- Two Fully Independent 2–to–4–Line Decoders/Demultiplexers
- Schottky Clamped for High Performance

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–1	mA
Low–Level Output Current	I_{OL}	–	–	20	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = 18mA	–	–	–1.2	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = –1mA	2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA	–	–	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	50	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.5V	–	–	–2	mA
Short–Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	–40	–	–100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Output Enabled and Open	–	75	90	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time and duration of short–circuit should not exceed one second.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Levels of Logic	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From Binary Input to Any Output)	t_{PLH}	2	R_L = 280Ω, C_L = 15pF	–	5	7.5	ns
	t_{PHL}	2		–	6.5	10	ns
Propagation Delay Time (From Select Input to Any Output)	t_{PLH}	3		–	7	12	ns
	t_{PHL}	3		–	8	12	ns
Propagation Delay Time (From Enable Input to Any Output)	t_{PLH}	2		–	5	8	ns
	t_{PHL}	2		–	6.5	10	ns

Function Table:

Inputs			Outputs			
Enable $\overline{G}$	Select					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level

L = LOW Level

X = Don’t Care

Pin Connection Diagram