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NTE74LS122 Integrated Circuit TTL – Retriggerable Monostable Multivibrator with Clear

Description:

The NTE74LS122 is a retriggerable monostable multivibrator in a 14-Lead plastic DIP type package that features output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values. The device contains internal timing resistors that allow the circuit to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

Features:

- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations
- DC Triggered from Active-HIGH Transition or Active-LOW Transition Inputs
- DC Retriggerable from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Internal Timing Resistors

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High-Level Output Current	I_{OH}	–	–	–400	μA
Low-Level Output Current	I_{OL}	–	–	8	mA
Pulse Width	t_w	40	–	–	ns
External Timing Resistance	R_{ext}	5	–	260	$k\Omega$
External Capacitance	C_{ext}	No Restriction			
Wiring Capacitance at R_{ext}/C_{ext} Terminal		–	–	50	pF
Operating Temperature Range	T_A	0	–	+70	$^{\circ}C$

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
High Level Input Voltage	V_{IH}		2	–	–	V	
Low Level Input Voltage	V_{IL}		–	–	0.8	V	
Input Clamp Voltage	V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$	–	-0.65	-1.5	V	
High Level Output Voltage	V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2\text{V}, I_{OH} = -400\mu\text{A}$	2.7	3.5	–	V	
Low Level Output Voltage	V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}$	$I_{OL} = 4\text{mA}$	–	0.25	0.4	V
			$I_{OL} = 8\text{mA}$	–	0.35	0.5	V
Input Current	I_I	$V_{CC} = \text{MAX}, V_I = 7\text{V}$	–	–	0.1	mA	
High Level Input Current	I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$	–	–	20	μA	
Low Level Input Current	I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	–	–	-0.4	mA	
Short-Circuit Output Current	I_{OS}	$V_{CC} = \text{MAX}, \text{Note 4}$	-20	–	-100	mA	
Supply Current	I_{CC}	$V_{CC} = \text{MAX}, \text{Note 5}$	–	–	11	mA	

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$.

Note 4. Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Note 5. With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary GND, then 4.5V is applied to clock.

Switching Characteristics: ($V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From A Input to Q Output)	t_{PLH}	$C_{ext} = 0, R_{ext} = 5\text{k}\Omega, R_L = 2\text{k}\Omega, C_L = 15\text{pF}$	–	23	33	ns
(From B Input to Q Output)			–	23	44	ns
(From A Input to \bar{Q} Output)	t_{PHL}		–	32	44	ns
(From B Input to \bar{Q} Output)			–	34	56	ns
Propagation Delay Time (From Clear Input to Q Output)	t_{PLH}		–	20	27	ns
(From Clear Input to \bar{Q} Output)	t_{PHL}		–	28	45	ns
Pulse Width (From A or B Input to Q Output)	$t_{wQ}(\text{min})$		–	116	200	ns
Pulse Width (From A or B Input to Q Output)	t_{wQ}		$C_{ext} = 1000\text{pF}, R_{ext} = 10\text{k}\Omega, R_L = 2\text{k}\Omega, C_L = 15\text{pF}$	4.0	4.5	5.0

Typical Application Data:

The output pulse t_W is a function of the external components, C_{ext} and R_{int} . For values of $C_{ext} \geq 1000\text{pF}$, the output pulse at $V_{CC} = 5\text{V}$ and $V_{RC} = 5\text{V}$ is given by:

$$t_W = K R_{ext} C_{ext} \text{ where } K \text{ is nominally } 0.45$$

If C_{ext} is in pF and R_{ext} is in k Ω then t_W is in nanoseconds.

The C_{ext} terminal is an internal connection to GND, however for the best system performance C_{ext} should be hard-wired to GND.

Care should be taken to keep R_{ext} and C_{ext} as close to the monostable as possible with a minimum amount of inductance between the R_{ext}/C_{ext} junction and the R_{ext}/C_{ext} pin. Good groundplane and adequate bypassing should be designed into the system for optimum performance to insure that no false triggering occurs.

Typical Application Data (Cont'd):

A switching diode is not needed for electrolytic capacitance and should not be used.

As long as $C_{ext} \geq 1000\text{pF}$ and $5\text{K} \leq R_{ext} \leq 260\text{K}$, the change in K with respect to R_{ext} is negligible.

If $C_{ext} \leq 1000\text{pF}$, the pulse width t_W in nanoseconds is approximated by:



















$$t_W = 6 + 0.05 C_{ext} (\text{pF}) + 0.45 R_{ext} (\text{k}\Omega) C_{ext} + 11.6 R_{ext}$$

In order to trim the output pulse width, it is necessary to include a variable resistor between V_{CC} and the R_{ext} pin. R_{ext} remote should be kept as close to the monostable as possible.

Retriggering of the part must not occur before C_{ext} is discharged or trigger pulse will not have any effect. The discharge time of C_{ext} in nanoseconds is guaranteed to be less than $0.22 C_{ext}$ (pF) and is typically $0.05 C_{ext}$ (pF).

For the smallest possible deviation in output pulse widths from various devices, it is suggested that C_{ext} be kept $\geq 1000\text{pF}$.

Function Table:

Inputs					Outputs	
Clear	A1	A2	B1	B2	Q	\bar{Q}
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H		
H	L	X	H	↑		
H	X	L	↑	h		
H	X	L	H	↑		
H	H	↓	H	H		
H	↓	↓	H	H		
H	↓	H	H	H		
↑	L	X	H	H		
↑	X	L	H	H		

† These lines of the functional table assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

Pin Connection Diagram

