1.1 Scope.

This specification covers the detail requirements for a linear bipolar monolithic dual low drift, low offset voltage operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD708SQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-8.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	±22 V
Internal Power Dissipation[1]	500 mW
Differential Input Voltage	$\pm V_S$
Input Voltage	$\pm V_S$
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AD708S	−55°C to +125°C
Lead Temperature (Soldering 60 sec)	+300°C

NOTE
[1]Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Cerdip (Q)	75°C	6.7 mW/°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 22°C/W for Q-8
θ_{JA} = 110°C/W for Q-8

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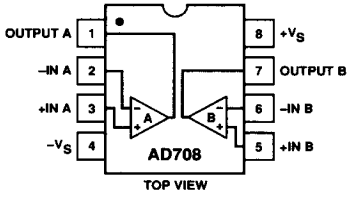
Table 1.

Test	Symbol	Device	Sub Group 1	Sub Group 2, 3	Test Condition[1]	Units
Gain Open Loop	A_{VS}	−1	4000	4000	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10\ V$	V/mV min
Output Voltage Swing	V_{OP}	−1	13.5		$R_L = \geq 10\ k\Omega$	±V min
			12.5	12.0	$R_L = 2\ k\Omega$	
			12.0		$R_L = 1\ k\Omega$	
Input Offset Voltage	V_{IO}	−1	50	65		±μV max
Input Offset Drift	$\Delta V_{IO}/\Delta T$	−1	0.4			±μV/°C max
Input Offset Voltage Match[2]	V_{OSM}	−1	50	75		±μV max
Input Offset Voltage Drift Match[2]	TCV_{OSM}	−1	0.4			±μV/°C max
Input Offset Current	I_{IO}	−1	1.0	1.5		±nA max
Input Bias Current	I_{IB}	−1	1.0	4.0		±nA max
Input Bias Current Match[2]	I_{IBM}	−1	1.0	2.0		±nA max
Common-Mode Rejection Ratio	CMRR	−1	130	130	$V_{CM} = \pm 13\ V$	dB min
Power Supply Rejection Ratio	PSRR	−1	120	120	$\pm 3 \leq V_S \leq \pm 18$	dB min
Common-Mode Rejection Ratio Match[2]	$CMRR_M$	−1	120	114	$V_{CM} = \pm 13\ V$	dB min
Power Supply Rejecton Ratio Match[2]	$PSRR_M$	−1	120	120	$\pm 3\ V \leq V_S \leq 18\ V$	dB min
Power Supply Current	I_Q	−1	5.5			mA max
Power Consumption	P_D	−1	165		No Load	mW max

NOTES
[1]$V_S = \pm 15$ V, unless otherwise noted.
[2]Matching is defined as the difference between parameters of the two amplifiers.

3.2.1 Functional Block Diagram and Terminal Assignments.

Cerdip (Q) Package



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).