

**MOTOROLA SEMICONDUCTOR TECHNICAL DATA**

T-33-05  
**2N3924**

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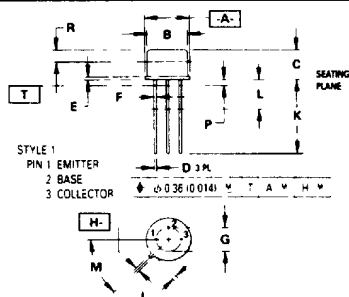
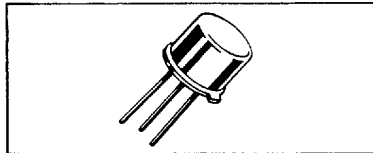
**The RF Line**

**NPN SILICON RF POWER TRANSISTOR**

... optimized Annular transistor for large-signal power-amplifier and driver applications to 300 MHz.

- Designed for 13.6 Volt Operation
- High Output Power — 4.0 W Min @ f = 175 MHz
- Multiple-Emitter Construction for Excellent High-Frequency Performance
- Guaranteed Safe Operating Area  
V<sub>CEO(sus)</sub> Measured at I<sub>C</sub> = 200 mA

**NPN SILICON  
RF POWER TRANSISTOR**



STYLE 1  
PIN 1 EMITTER  
2 BASE  
3 COLLECTOR

- NOTES
- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982
  - 2 CONTROLLING DIMENSION INCH
  - 3 DIMENSION J MEASURED FROM DIMENSION A MAXIMUM
  - 4 DIMENSION B SHALL NOT VARY MORE THAN 0.25 0.010 IN ZONE R THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING
  - 5 DIMENSION F APPLIES BETWEEN DIMENSION P AND L DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.41	0.53	0.016	0.021
E	0.23	1.04	0.009	0.041
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45 BSC		45 BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

**CASE 79-04  
TO-205AD  
(TO-39)**

**\*MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	18	Vdc
Collector-Base Voltage	V <sub>CB</sub>	36	Vdc
Emitter-Base Voltage	V <sub>EB</sub>	4.0	Vdc
Collector Current	I <sub>C</sub>	0.5	Adc
Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	7.0 40	Watts mW/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +200	°C

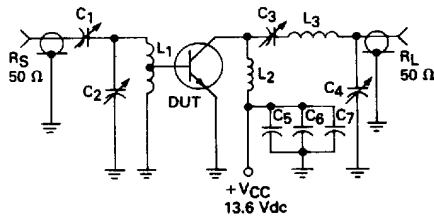
\*Indicates JEDEC Registered Data

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>						
Collector-Emitter Sustaining Voltage (Figure 2) (I <sub>C</sub> = 200 mAdc)	V <sub>CEO(sus)</sub>	18	—	—	Vdc	
Collector-Base Breakdown Voltage (I <sub>C</sub> = 0.25 mAdc, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	36	—	—	Vdc	
Emitter-Base Breakdown Voltage (I <sub>E</sub> = 1.0 mAdc, I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	4.0	—	—	Vdc	
Collector Cutoff Current (V <sub>CB</sub> = 15 Vdc, I <sub>E</sub> = 0) (V <sub>CB</sub> = 15 Vdc, I <sub>E</sub> = 0, T <sub>A</sub> = 150°C)	I <sub>CBO</sub>	—	—	0.1 5.0	mAdc	
<b>DYNAMIC CHARACTERISTICS</b>						
Current-Gain — Bandwidth Product (I <sub>C</sub> = 100 mAdc, V <sub>CE</sub> = 13.6 Vdc, f = 100 MHz)	f <sub>T</sub>	—	350	—	MHz	
Output Capacitance (V <sub>CB</sub> = 13.6 Vdc, I <sub>E</sub> = 0, f = 100 kHz)	C <sub>ob</sub>	—	12.5	20	pF	
<b>FUNCTIONAL TESTS</b>						
Power Input	Test Circuit Figure 1	P <sub>in</sub>	—	—	1.0	Watt
Common-Emitter Amplifier	V <sub>CE</sub> = 13.6 Vdc, R <sub>S</sub> = 50 ohms,	G <sub>pe</sub>	6.0	7.3	—	dB
Power Gain	R <sub>L</sub> = 50 ohms, f = 175 MHz					
Collector Efficiency	P <sub>out</sub> = 4.0 Watts	η	70	—	—	%

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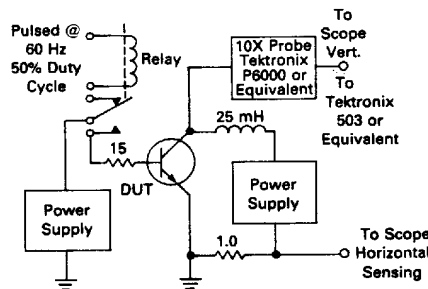
FIGURE 1 — 175 MHz TEST CIRCUIT



- C<sub>1</sub>, C<sub>2</sub>, C<sub>4</sub> ..... 5-50 pF (Air variable)
- C<sub>3</sub> ..... 7-100 pF (Air variable)
- C<sub>5</sub> ..... 470 pF (Disc ceramic)
- C<sub>6</sub> ..... 0.01 μF (Disc ceramic)
- C<sub>7</sub> ..... 0.001 μF (Disc ceramic)

- L<sub>1</sub> — 1½ turns #14 AWG tinned wire; ¼" ID Air wound; winding length ¾"; base tapped 1 turn from ground
- L<sub>2</sub> — RFC
- L<sub>3</sub> — 2 turns #14 AWG tinned wire; ¼" ID Air wound; winding length ¾"

FIGURE 2 — PULSE TEST CIRCUIT



CLASS C DESIGN DATA FOR  $V_{CE} = 13.6 \text{ Vdc}$ ,  $T_C = 25^\circ\text{C}$   
 (Emitter Grounded Directly to the Chassis — No Tuned-Emitter Techniques Used)

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FIGURE 3 — POWER OUTPUT versus FREQUENCY

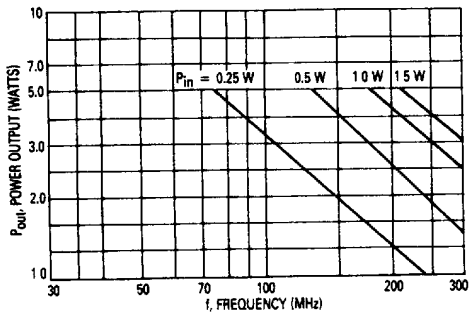


FIGURE 4 — POWER OUTPUT versus POWER INPUT

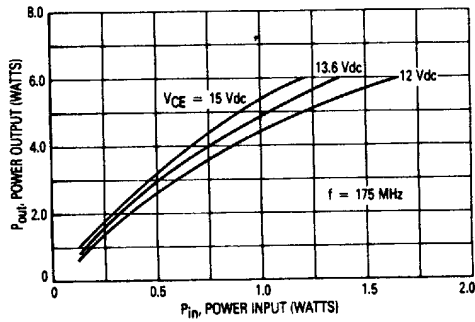


FIGURE 5 — PARALLEL EQUIVALENT INPUT RESISTANCE

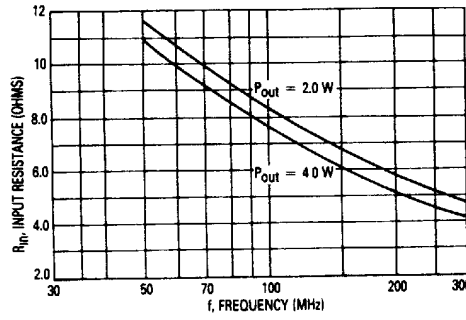


FIGURE 6 — PARALLEL EQUIVALENT INPUT CAPACITANCE

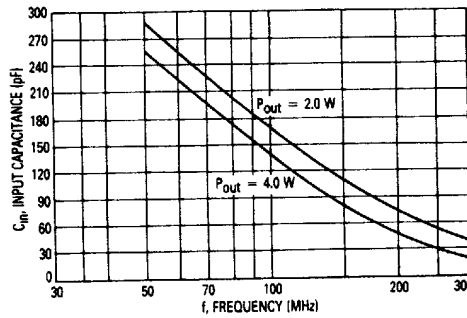


FIGURE 7 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE

