LP3981 Micropower, 300mA Ultra Low-Dropout CMOS Voltage Regulator

Check for Samples: LP3981

FEATURES

- **Small, Space Saving VSSOP-8**
- **Low Thermal Resistance in WSON-6 Package Gives Excellent Power Capability**
- **Logic Controlled Enable**
- **Stable with Ceramic and High Quality Tantalum Capacitors**
- **Fast Turn-On**
- **Thermal Shutdown and Short-Circuit Current Limit**

KEY SPECIFICATIONS

- **2.5 to 6.0V Input Range**
- **300mA Output**
- **60dB PSRR at 1kHz**
- **≤1µA Quiescent Current when Shut Down**
- **Fast Turn-On Time: 120 µs (Typ.) with C_{BYPASS} = 0.01uF**
- **132mV Typ Dropout with 300mA Load**
- **35µVrms Output Noise over 10Hz to 100kHz**
- **−40 to +125°C Junction Temperature Range for Operation**
- **2.5V, 2.7V, 2.8V, 2.83V, 3.0V, 3.03V, and 3.3V Outputs Standard**

APPLICATIONS

- **CDMA Cellular Handsets**
- **Wideband CDMA Cellular Handsets**
- **GSM Cellular Handsets**
- **Portable Information Appliances**
- **Tiny 3.3V ± 5% to 2.5V, 300mA Converter**

DESCRIPTION

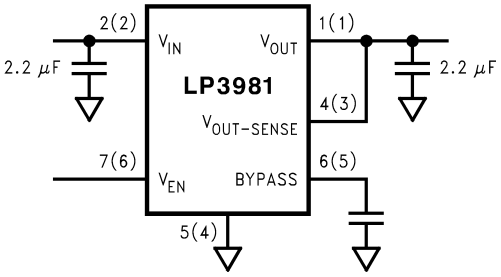
The LP3981's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies. This high power supply rejection is maintained down to lower input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 300 mA, from a 2.5V to 6V input, consuming less than 1µA in disable mode.

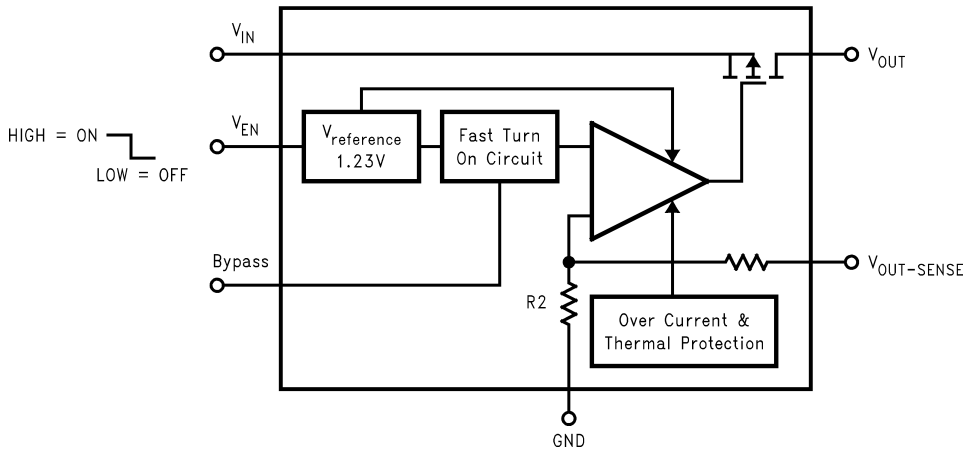
The LP3981 is available in VSSOP-8 package. For LP3981 in WSON-6 package, contact TI sales offices. Performance is specified for −40°C to +125°C temperature range. The device available in the following output voltages; 2.5V, 2.7V, 2.8V, 2.83V, 3.0V, 3.03V and 3.3V as standard. Other output options can be made available, please contact your local TI sales office.

Typical Application Circuit



Note: Pin Numbers in parenthesis indicate WSON-6 package.

Block Diagram



PIN DESCRIPTIONS

Name	VSSOP-8	WSON-6	Function
V_{EN}	7	6	Enable Input Logic, Enable High.
GND	5	4	Common Ground. Connect to PAD.
V_{OUT}	1	1	Output Voltage of the LDO.
V_{IN}	2	2	Input Voltage of the LDO.
Bypass	6	5	Optional bypass capacitor for noise reduction.
$V_{OUT-SENSE}$	4	3	Output. Voltage Sense Pin. Should be connected to V_{OUT} for proper operation.
N.C.	3, 8		
GND		PAD	Common Ground. Connect to pin 4.

Connection Diagrams

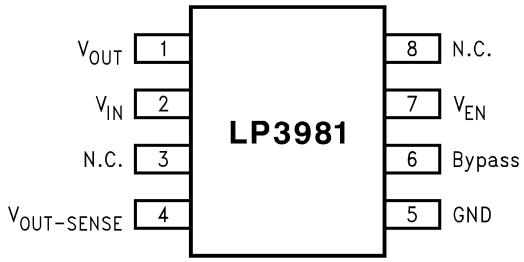


Figure 1. Top View
VSSOP-8 Package
See Package Number DGK

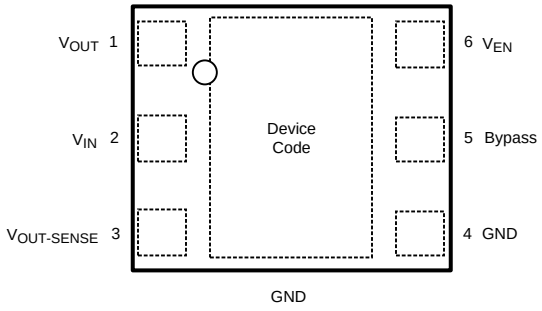


Figure 2. Top View
WSON-6 Package
See Package Number NGC0006D

ORDERING INFORMATION(1)(2)

WSON-6				
Output Voltage	**Grade**	**LP3981 Supplied as 1000 Units Tape and Reel**	**LP3981 Supplied as 4500 Units Tape and Reel**	**Package Marking**
2.5V	STD	LP3981ILD-2.5	LP3981ILDX-2.5	LO1UB
2.7V		LP3981ILD-2.7	LP3981ILDX-2.7	LO1VB
2.8V		LP3981ILD-2.8	LP3981ILDX-2.8	LO1ZB
2.83V		LP3981ILD-2.83	LP3981ILDX-2.83	L01SB
3.0V		LP3981ILD-3.0	LP3981ILDX-3.0	L017B
3.03V		LP3981ILD-3.03	LP3981ILDX-3.03	LO1YB
3.3V		LP3981ILD-3.3	LP3981ILDX-3.3	LO1XB
VSSOP-8 Package				
Output Voltage	**Grade**	**LP3981 Supplied as 1000 Units Tape and Reel**	**LP3981 Supplied as 3500 Units Tape and Reel**	**Package Marking**
2.5V	STD	LP3981IMM-2.5	LP3981IMMX-2.5	LFKB
2.7V		LP3981IMM-2.7	LP3981IMMX-2.7	LFLB
2.8V		LP3981IMM-2.8	LP3981IMMX-2.8	LFTB
2.83V		LP3981IMM-2.83	LP3981IMMX-2.83	LDUB
3.0V		LP3981IMM-3.0	LP3981IMMX-3.0	LF3B
3.03V		LP3981IMM-3.03	LP3981IMMX-3.03	LFPB
3.3V		LP3981IMM-3.3	LP3981IMMX-3.3	LFNB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

V_{IN}, V_{EN}	−0.3 to 6.5V
V_{OUT}, $V_{OUT-SENSE}$	−0.3 to V_{IN} + 0.3, Max 6.5V
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Lead Temp.	
Pad Temp.	
Power Dissipation (4) θ_{JA} (VSSOP-8) θ_{JA} (WSON-6)	 210°C/W 50°C/W
Maximum Power Dissipation at 25°C VSSOP-8 WSON-6	 595mW 2.5W
ESD Rating(5) Human Body Model Machine Model	 2kV 200V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) The figures given for Absolute Maximum Power dissipation for the device are calculated using the following equations: $P_D = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$ where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the WSON package θ_{JA}=50°C/W, $T_{J(MAX)}$=150°C and using T_A=25°C the maximum power dissipation is found to be 2.5W. The derating factor ($-1/\theta_{JA}$) = −20mW/°C, thus below 25°C the power dissipation figure can be increased by 20 mW per degree, and similarity decreased by this factor for temperatures above 25°C
(5) The human body model is 100pF discharged through 1.5kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Ratings(1)(2)

V_{IN}	2.7 to 6V
V_{EN}	0 to V_{IN}
Junction Temperature	−40°C to +125°C
Maximum Power Dissipation (3) VSSOP-8 WSON-6	 476mW 2.0W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) As for the Maximum Power dissipation, the maximum power in operation is dependant on the ambient temperature. This can be calculated in the same way using T_J=125°C, giving 2W as the maximum power dissipation for the WSON package in operation. The same derating factor applies.

Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.2V, V_{IN} = V_{OUT} + 0.5V, C_{IN} = 2.2 µF, C_{BP} = 0.033 µF, I_{OUT} = 1mA, C_{OUT} = 2.2 µF. Typical values and imits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C.(1)(2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance			−2 **−3**	2 **3**	% of $V_{OUT(nom)}$
	Line Regulation Error	V_{IN} = V_{OUT} + 0.5V to 6.0V, T_A < +85°C	0.005	−0.1	0.1	%/V
		V_{IN} = V_{OUT} + 0.5V to 6.0V, T_J ≤125°C		**−0.2**	**0.2**	%/V
	Load Regulation Error (3)	I_{OUT} = 1 mA to 300 mA	0.0003		**0.005**	%/mA
PSRR	Power Supply Rejection Ratio (4)	V_{IN} = $V_{OUT(nom)}$ + 1V, f = 1 kHz, I_{OUT} = 50 mA (Figure 4)	50			dB
		V_{IN} = $V_{OUT(nom)}$ + 1V, f = 10 kHz, I_{OUT} = 50 mA (Figure 4)	55			
I_Q	Quiescent Current	V_{EN} = 1.2V, I_{OUT} = 1 mA	70		**120**	µA
		V_{EN} = 1.2V, I_{OUT} = 1 to 300 mA, V_{OUT} = 2.5V(5)	170		**210**	
		V_{EN} = 0.4V	0.003		**1.5**	
	Dropout Voltage (6)	I_{OUT} = 1 mA	0.5		**5**	mV
		I_{OUT} = 200 mA	88		**133**	
		I_{OUT} = 300 mA	132		**200**	
I_{SC}	Short Circuit Current Limit	Output Grounded (Steady State)	600			mA
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{BP} = 0.033µF	35			µVrms
TSD	Thermal Shutdown Temperature		160			°C
	Thermal Shutdown Hysteresis		20			°C
$I_{OUT(PK)}$	Peak Output Current	V_{OUT} ≥ V_{OUT} (nom) - 5%	455	300		
I_{EN}	Maximum Input Current at V_{EN}	V_{EN} = 0 and V_{IN}	0.001			µA
V_{IL}	Logic Low Input threshold	V_{IN} = 2.7 to 6.0V			**0.4**	V
V_{IH}	Logic High Input threshold	V_{IN} = 2.7 to 6.0V		**1.4**		V
T_{ON}	Turn-On Time (4) (7)	C_{BYPASS} = 0.033 µF	240		**350**	µs

(1) Min and Max Limits are specified by design, test, or statistical analysis. Typical (Typ.) numbers are not verified, but do represent the most likely norm.
(2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
(3) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(4) Specified by design. Not production tested.
(5) For V_{OUT} > 2.5C, Increase $I_{Q(MAX)}$ by 2.5µA for every 0.1V increase in $V_{OUT(NOM)}$.i.e. $I_{Q(MAX)}$ = 210 + (($V_{OUT(NOM)}$ - 2.5) * 25)µA
(6) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.
(7) Turn-on time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.

Electrical Characteristics Output Capacitor, Recommended Specification

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
C_{OUT}	Output Capacitor	Capacitance		2.2	22	µF
		ESR		5	500	mΩ

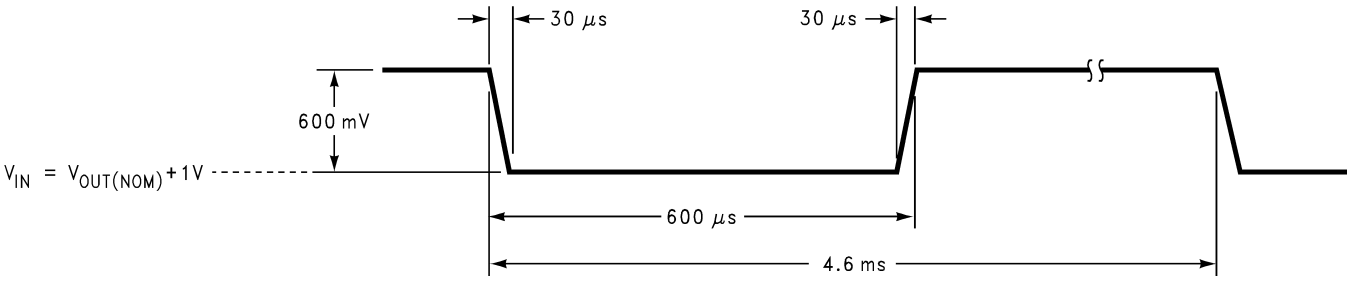


Figure 3. Line Transient Response Input Perturbation

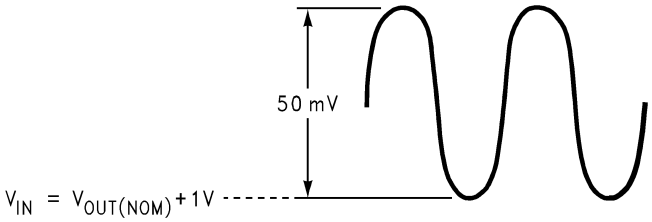
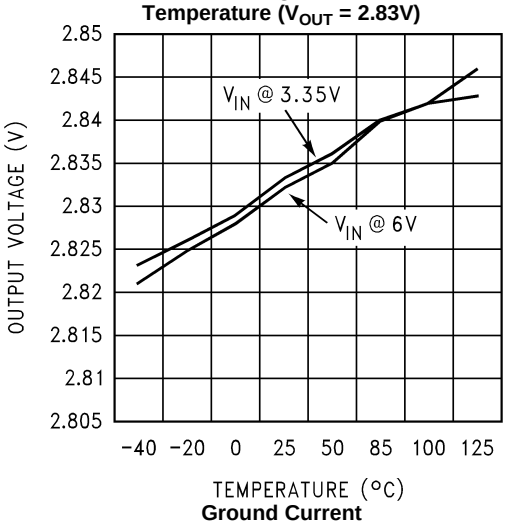


Figure 4. PSRR Input Perturbation

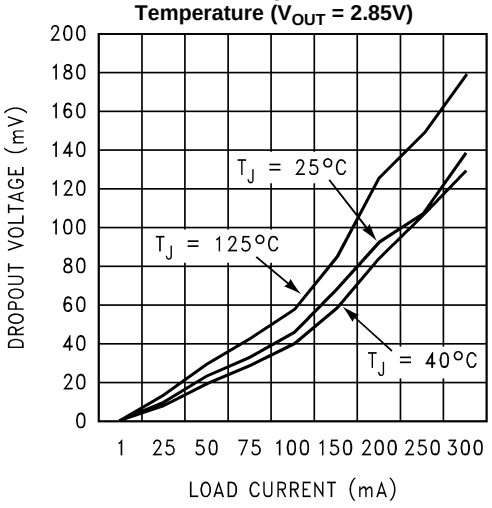
Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2\ \mu F$ Ceramic, $C_{BP} = 0.033\ \mu F$, $V_{IN} = V_{OUT} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}.

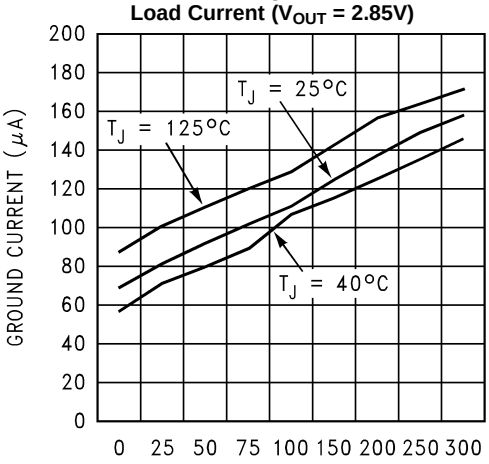
Output Voltage vs. Temperature (V_{OUT} = 2.83V)



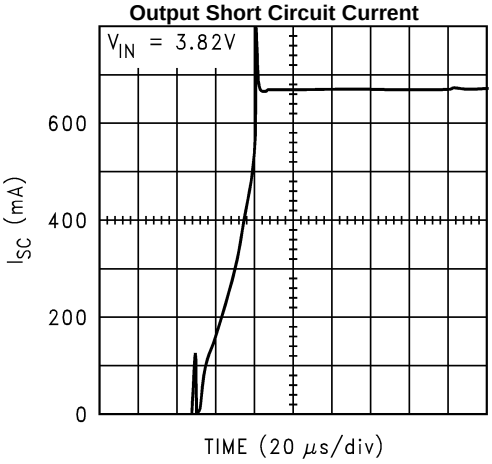
Dropout Voltage vs. Temperature (V_{OUT} = 2.85V)



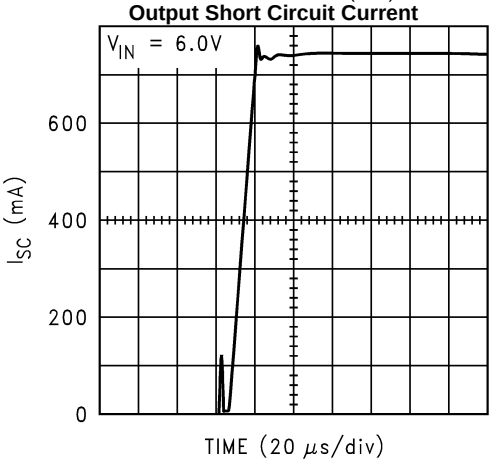
Ground Current vs. Load Current (V_{OUT} = 2.85V)



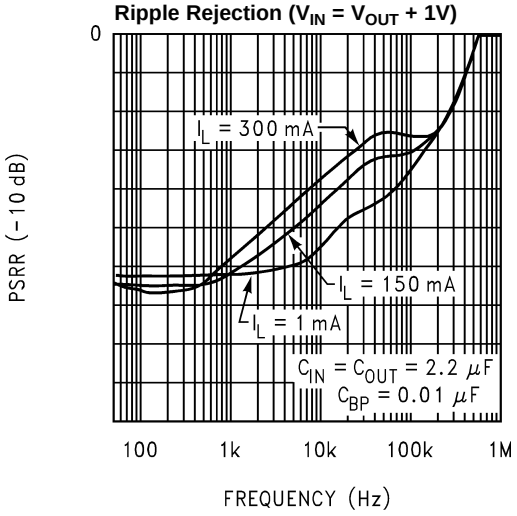
Output Short Circuit Current



Output Short Circuit Current



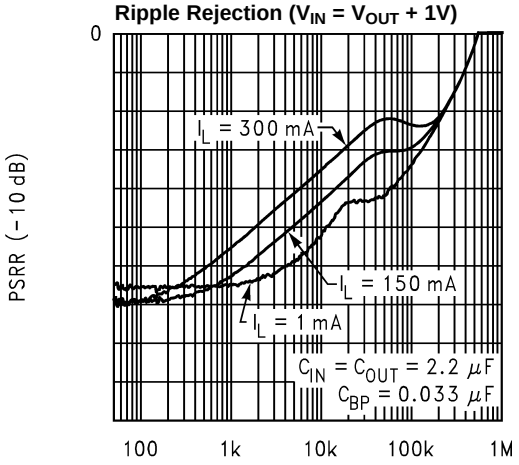
Ripple Rejection ($V_{IN} = V_{OUT}$ + 1V)



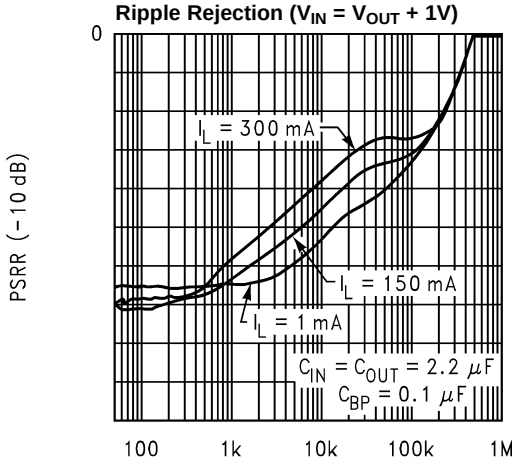
Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2\ \mu F$ Ceramic, $C_{BP} = 0.033\ \mu F$, $V_{IN} = V_{OUT} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}.

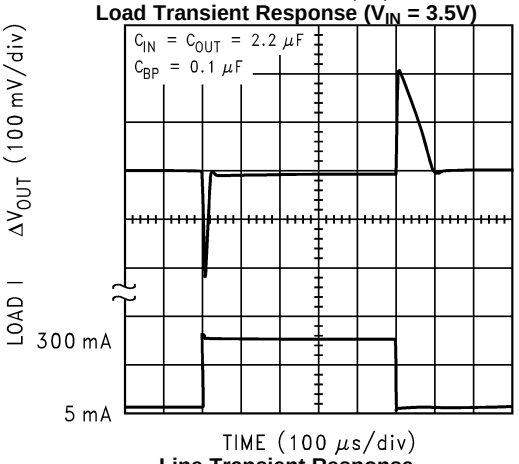
Ripple Rejection ($V_{IN} = V_{OUT} + 1V$)



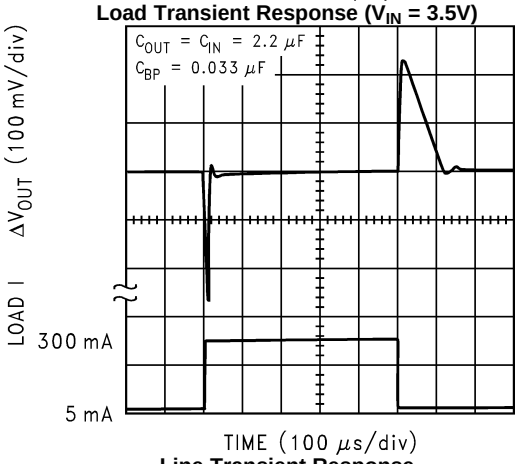
Ripple Rejection ($V_{IN} = V_{OUT} + 1V$)



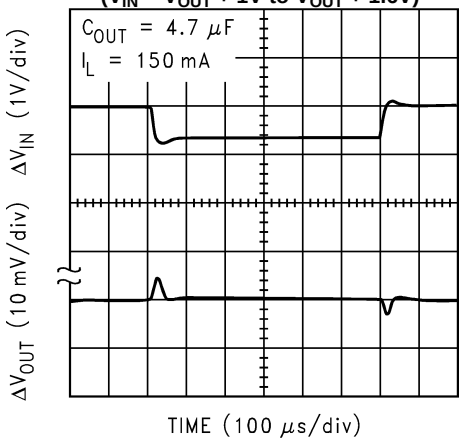
Load Transient Response ($V_{IN} = 3.5V$)



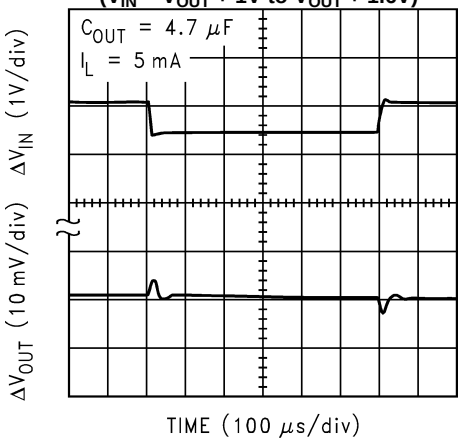
Load Transient Response ($V_{IN} = 3.5V$)



Line Transient Response ($V_{IN} = V_{OUT} + 1V$ to $V_{OUT} + 1.6V$)



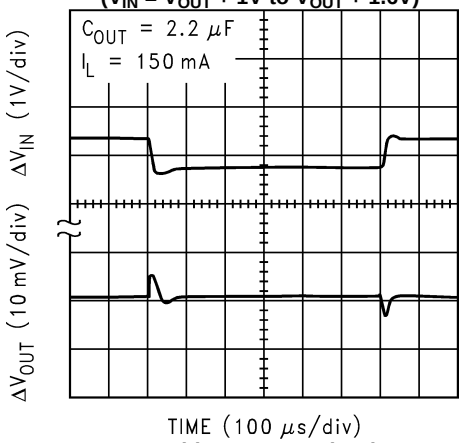
Line Transient Response ($V_{IN} = V_{OUT} + 1V$ to $V_{OUT} + 1.6V$)



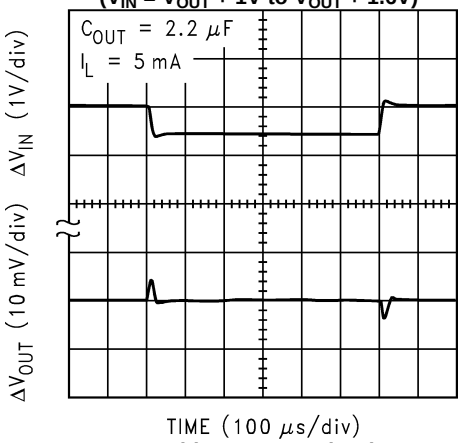
Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2$ µF Ceramic, $C_{BP} = 0.033$ µF, $V_{IN} = V_{OUT} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}.

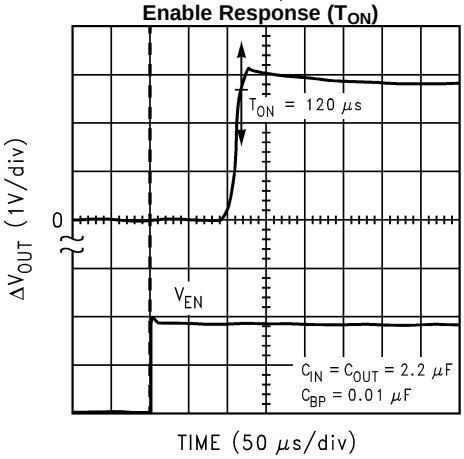
Line Transient Response
($V_{IN} = V_{OUT}$ + 1V to V_{OUT} + 1.6V)



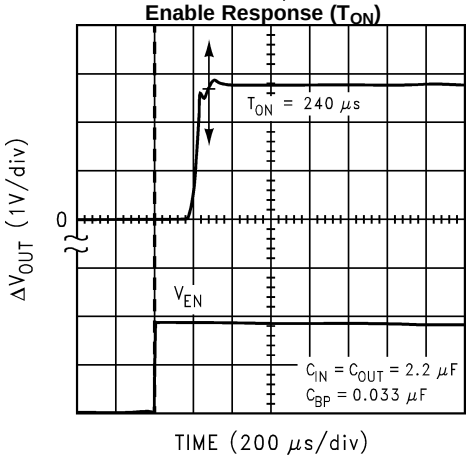
Line Transient Response
($V_{IN} = V_{OUT}$ + 1V to V_{OUT} + 1.6V)



Enable Response (T_{ON})



Enable Response (T_{ON})



APPLICATION HINTS

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependant on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in the notes for Absolute Maximum Ratings and Operating Ratings, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \quad (1)$$

With a θ_{JA} = 50°C/W, the device in the WSON package returns a value of 2.0W with a maximum junction temperature of 125°C and an ambient temperature of 25°C. The device in a VSSOP package returns a figure of 0.476W, (θ_{JA} = 210°C/W).

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal considerations, the voltage drop across the device, and the continuous current capability of the device. The device can deliver 300mA but care must be taken when choosing the continuous current output for the device under the operating load conditions.

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3981 requires external capacitors for regulator stability. The LP3981 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 2.2µF is required between the LP3981 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 2.2µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3981 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 2.2 to 22 µF range with 5mΩ to 500mΩ ESR range is suitable in the LP3981 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see CAPACITOR CHARACTERISTICS).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5 mΩ to 500 mΩ).

NO-LOAD STABILITY

The LP3981 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

NOISE BYPASS CAPACITOR

Connecting a 0.033µF capacitor between the C_{BP} pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the bad gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. Hight-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDO's, addition of a noise reduction capacitor does not effect the transient response of the device.

CAPACITOR CHARACTERISTICS

The LP3981 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1µF to 4.7µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3981.

The ceramic capacitor's capacitance can vary with temperature. Most large value ceramic capacitors (≅ 2.2µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

ON/OFF INPUT OPERATION

The LP3981 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST ON-TIME

The LP3981 utilizes a speed up circuitry to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turn on time.

REVISION HISTORY

Changes from Revision F (May 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3981ILD-2.5/NOPB	ACTIVE	WSON	NGC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LO1UB	Samples
LP3981ILD-2.8/NOPB	ACTIVE	WSON	NGC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L01ZB	Samples
LP3981ILD-3.0/NOPB	ACTIVE	WSON	NGC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-3-260C-168 HR		L017B	Samples
LP3981ILD-3.3/NOPB	ACTIVE	WSON	NGC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-3-260C-168 HR	-40 to 125	LO1XB	Samples
LP3981ILDX-2.5/NOPB	ACTIVE	WSON	NGC	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LO1UB	Samples
LP3981ILDX-2.7/NOPB	ACTIVE	WSON	NGC	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-3-260C-168 HR	-40 to 125	LO1VB	Samples
LP3981ILDX-2.8/NOPB	ACTIVE	WSON	NGC	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L01ZB	Samples
LP3981ILDX-2.83/NOPB	ACTIVE	WSON	NGC	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-3-260C-168 HR	-40 to 125	LO1SB	Samples
LP3981ILDX-3.03/NOPB	ACTIVE	WSON	NGC	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LO1YB	Samples
LP3981IMM-2.5	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	LFKB	
LP3981IMM-2.5/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFKB	Samples
LP3981IMM-2.7/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFLB	Samples
LP3981IMM-2.8/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFTB	Samples
LP3981IMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LF3B	Samples
LP3981IMM-3.03	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	LFPB	
LP3981IMM-3.03/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFPB	Samples
LP3981IMM-3.3	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	LFNB	
LP3981IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFNB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3981IMMX-2.5/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFKB	Samples
LP3981IMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFNB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

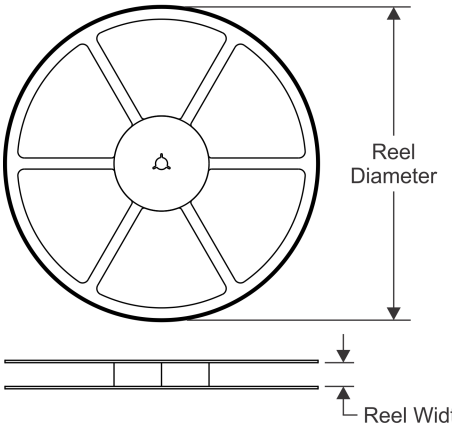
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

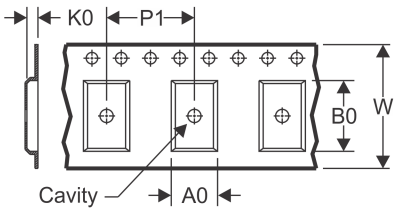
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

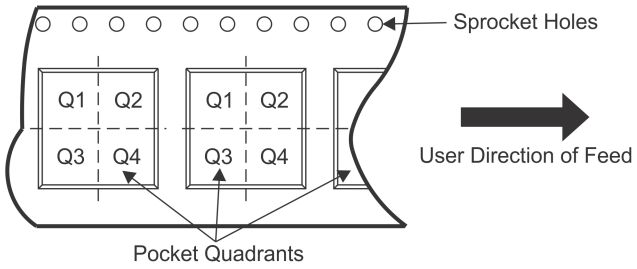


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

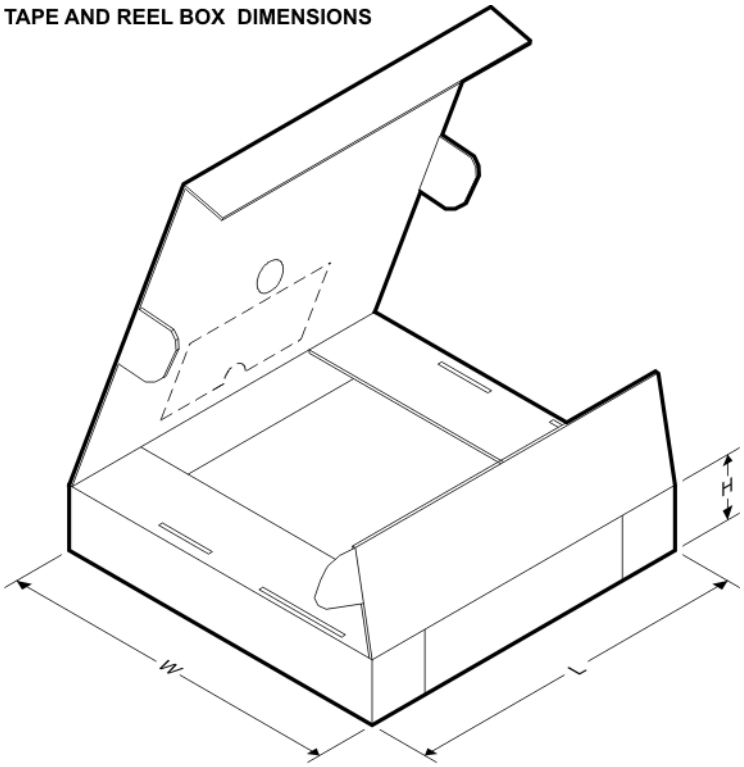


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3981ILD-2.5/NOPB	WSON	NGC	6	1000	178.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILD-2.8/NOPB	WSON	NGC	6	1000	178.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILD-3.0/NOPB	WSON	NGC	6	1000	180.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILD-3.3/NOPB	WSON	NGC	6	1000	180.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.5/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.7/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.8/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.83/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-3.03/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981IMM-2.5	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-2.5/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-2.7/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-2.8/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.03	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.03/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.3	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3981IMMX-2.5/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

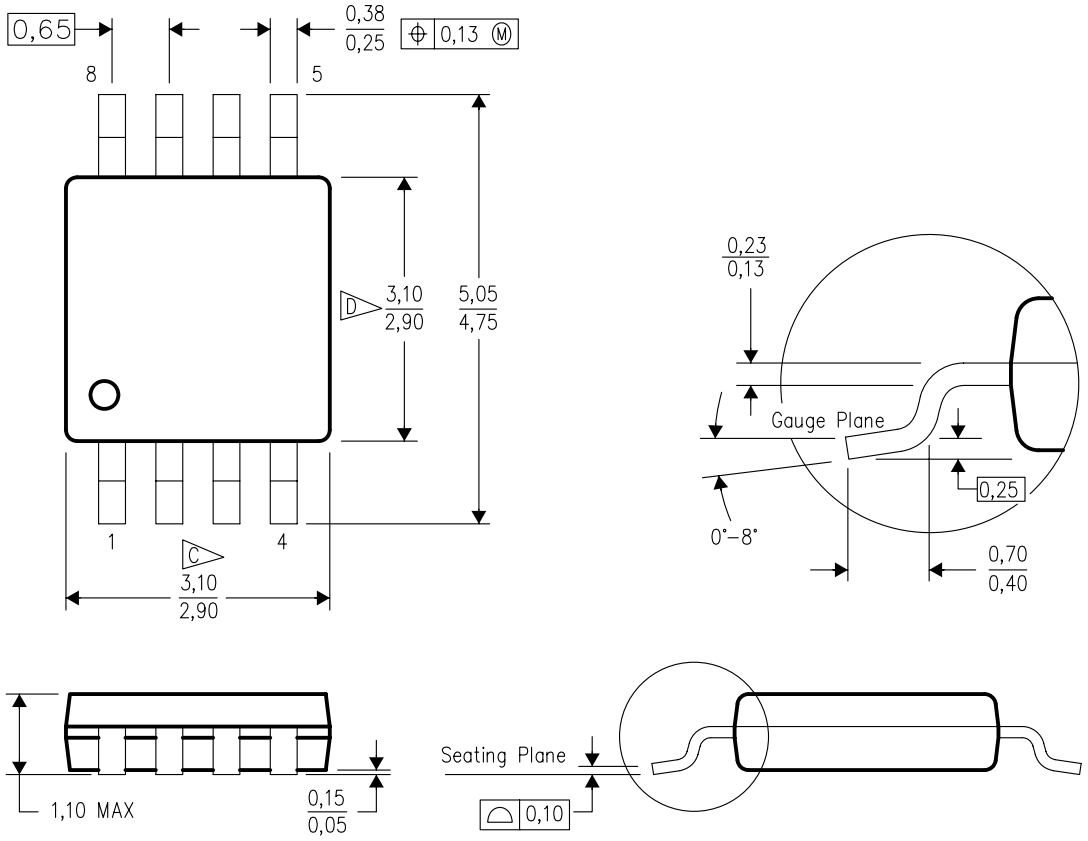


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3981ILD-2.5/NOPB	WSON	NGC	6	1000	213.0	191.0	55.0
LP3981ILD-2.8/NOPB	WSON	NGC	6	1000	213.0	191.0	55.0
LP3981ILD-3.0/NOPB	WSON	NGC	6	1000	195.0	200.0	45.0
LP3981ILD-3.3/NOPB	WSON	NGC	6	1000	195.0	200.0	45.0
LP3981ILDX-2.5/NOPB	WSON	NGC	6	4500	367.0	367.0	35.0
LP3981ILDX-2.7/NOPB	WSON	NGC	6	4500	370.0	355.0	55.0
LP3981ILDX-2.8/NOPB	WSON	NGC	6	4500	367.0	367.0	35.0
LP3981ILDX-2.83/NOPB	WSON	NGC	6	4500	370.0	355.0	55.0
LP3981ILDX-3.03/NOPB	WSON	NGC	6	4500	367.0	367.0	35.0
LP3981IMM-2.5	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMM-2.5/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMM-2.7/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMM-2.8/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMM-3.03	VSSOP	DGK	8	1000	210.0	185.0	35.0

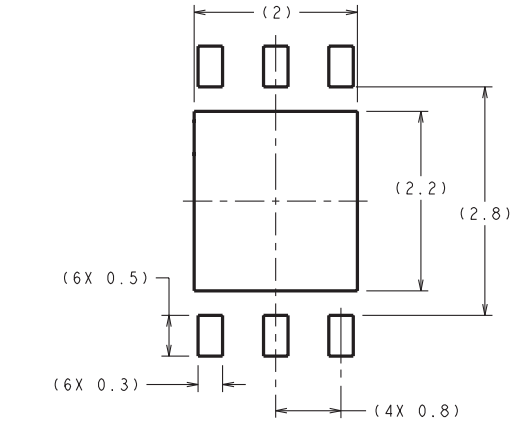
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3981IMM-3.03/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMM-3.3	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP3981IMMX-2.5/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3981IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



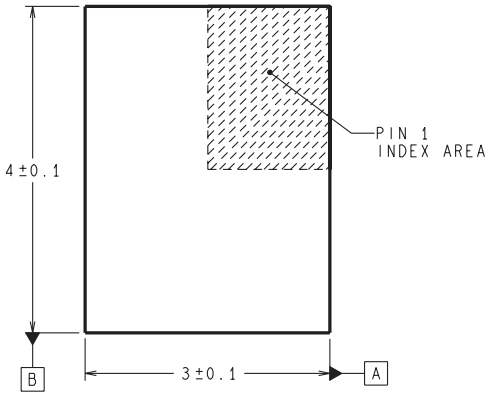
4073329/E 05/06

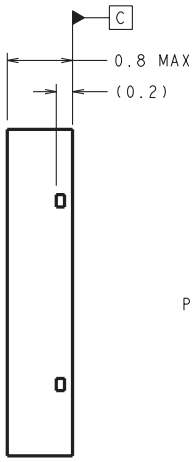
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

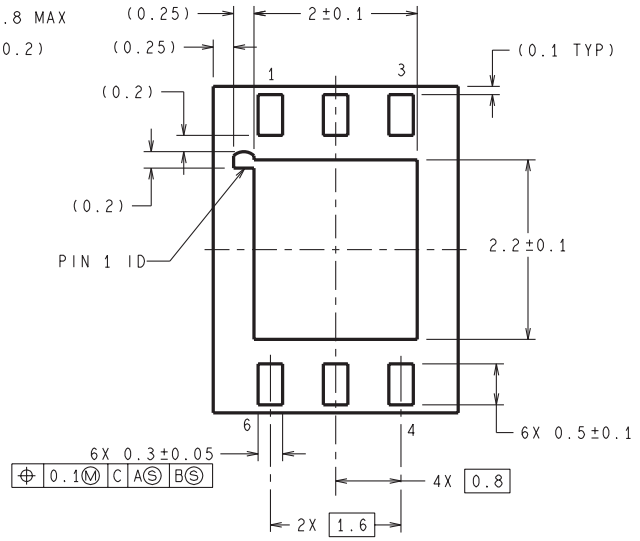


RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS







LDC06D (Rev B)

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