MOTOROLA
**SEMICONDUCTOR**
TECHNICAL DATA

# 2N3054
# 2N3054A

## MEDIUM-POWER NPN SILICON TRANSISTORS

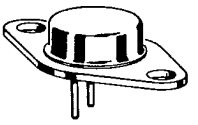
. . . designed for general purpose switching and amplifier applications.

- Excellent Safe Operating Area
- DC Current Gain Specified to 3.0 Amperes
- Complement to PNP Type 2N6049 or 2N4912

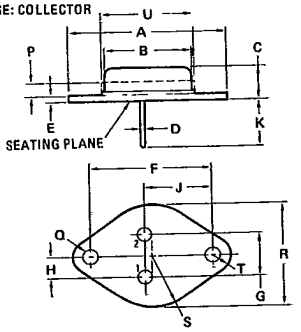
**4 AMPERE**

**POWER TRANSISTORS**
**NPN SILICON**

**55 VOLTS**
**25 WATTS – 2N3054**
**75 WATTS – 2N3054A**



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR




| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| B | 11.94 | 12.70 | 0.470 | 0.500 |
| C | 8.35 | 8.64 | 0.250 | 0.340 |
| D | 0.71 | 0.86 | 0.028 | 0.034 |
| E | 1.27 | 1.91 | 0.050 | 0.075 |
| F | 24.33 | 24.43 | 0.958 | 0.962 |
| G | 4.83 | 5.33 | 0.190 | 0.210 |
| H | 2.41 | 2.67 | 0.095 | 0.105 |
| J | 14.48 | 14.99 | 0.570 | 0.590 |
| K | 9.14 | – | 0.360 | – |
| P | – | 1.27 | – | 0.050 |
| Q | 3.61 | 3.86 | 0.142 | 0.152 |
| S | – | 8.89 | – | 0.350 |
| T | – | 3.68 | – | 0.145 |
| U | – | 15.75 | – | 0.620 |

All JEDEC Dimensions and and Notes Apply.

**CASE 80-02**
**TO-213AA**
**(TO-66)**

### *MAXIMUM RATINGS

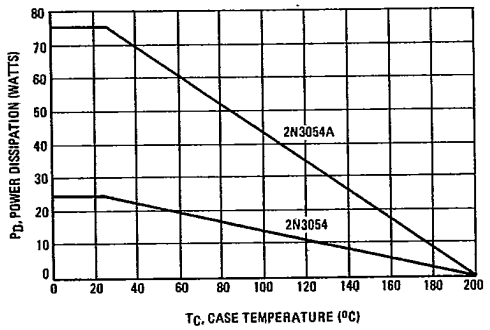
| Rating | Symbol | 2N3054A | 2N3054 | Unit |
|---|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | 55 | | Vdc |
| Collector-Emitter Voltage ($R_{BE}$ = 100 Ω) | $V_{CER}$ | 60 | | Vdc |
| Collector-Base Voltage | $V_{CB}$ | 90 | | Vdc |
| Emitter-Base Voltage | $V_{EB}$ | 7.0 | | Vdc |
| Collector Current — Continuous<br>Peak | $I_C$ | 4.0<br>10** | | Adc |
| Base Current | $I_B$ | 2.0 | | Adc |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 75<br>0.43 | 25<br>0.143 | Watts<br>W/°C |
| Operating and Storage Junction, Temperature Range | $T_J$, $T_{stg}$ | -65 to +200 | | °C |

*Indicates JEDEC Registered Data
**Addition to JEDEC Registered Data

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | 2N3054A | 2N3054 | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 2.33 | 7.0 | °C/W |

FIGURE 1 — POWER-TEMPERATURE DERATING




3

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25° unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| ***OFF CHARACTERISTICS** | | | | |
| Collector-Emitter Sustaining Voltage (1) ($I_C$ = 100 mAdc, $I_B$ = 0) | $V_{CEO(sus)}$ | 55 | — | Vdc |
| Collector-Emitter Sustaining Voltage (1) ($I_C$ = 100 mAdc, $R_{BE}$ = 100 Ω) | $V_{CER(sus)}$ | 60 | — | Vdc |
| Collector Cutoff Current ($V_{CE}$ = 30 Vdc, $I_B$ = 0) | $I_{CEO}$ | — | 500 | μAdc |
| Collector Cutoff Current ($V_{CE}$ = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) ($V_{CE}$ = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C$ = 150°C) | $I_{CEX}$ | —<br>— | 1.0<br>6.0 | mAdc |
| Emitter Cutoff Current ($V_{BE}$ = 7.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | — | 1.0 | mAdc |
| ***ON CHARACTERISTICS** (1) | | | | |
| DC Current Gain ($I_C$ = 0.5 Adc, $V_{CE}$ = 4.0 Vdc) ($I_C$ = 3.0 Adc, $V_{CE}$ = 4.0 Vdc) | $h_{FE}$ | 25<br>5.0 | 150<br>— | — |
| Collector-Emitter Saturation Voltage ($I_C$ = 500 mAdc, $I_B$ = 50 mAdc) ($I_C$ =3.0 Adc, $I_B$ = 1.0 Adc) | $V_{CE(sat)}$ | —<br>— | 1.0<br>6.0 | Vdc |
| Base-Emitter On Voltage ($I_C$ = 500 mAdc, $V_{CE}$ = 4.0 Vdc) | $V_{BE(on)}$ | — | 1.7 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Current-Gain—Bandwidth Product ($I_C$ = 200 mAdc, $V_{CE}$ = 10 Vdc) | $f_T$ | 3.0 | — | MHz |
| *Small-Signal Current Gain ($I_C$ = 100 mAdc, $V_{CE}$ = 4.0 Vdc, f = 1.0 kHz) | $h_{fe}$ | 25 | 180 | — |
| *Common-Emitter Cutoff Frequency ($I_C$ = 100 mAdc, $V_{CE}$ = 4.0 Vdc) | $f_{hfe}$ | 30 | — | kHz |

*Indicates JEDEC Registered Data
(1) Pulse test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%

3

**FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT**

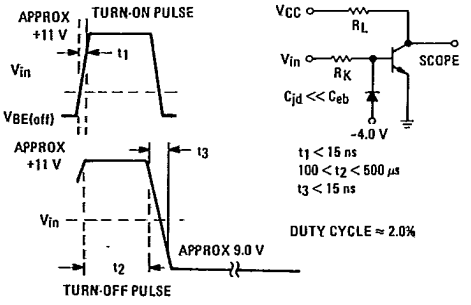



**FIGURE 3 – TURN-ON TIME**

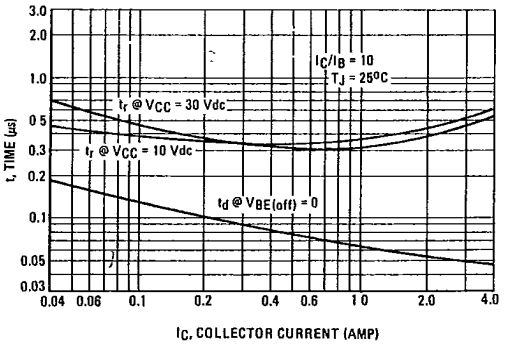


FIGURE 4 – THERMAL RESPONSE

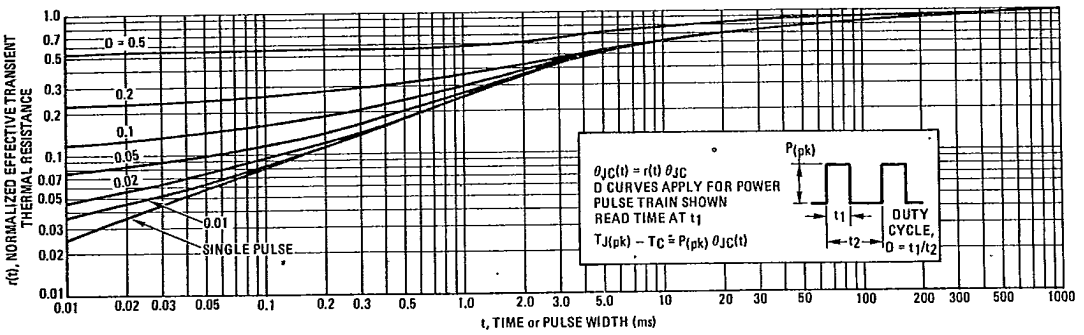
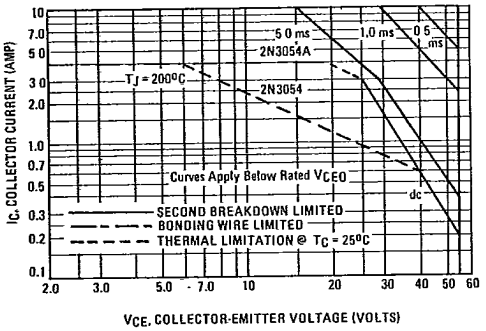



FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA




There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; $T_C$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

3

FIGURE 6 – TURN-OFF TIME

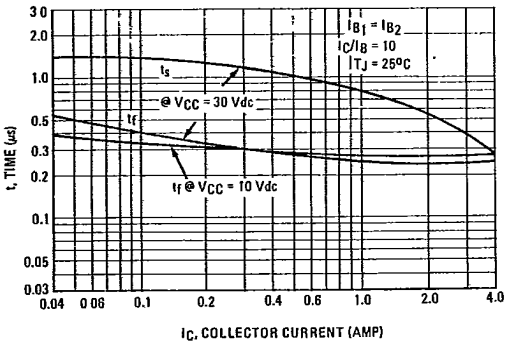



FIGURE 7 – CAPACITANCE

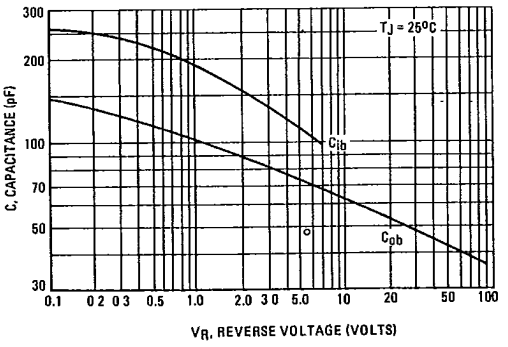


FIGURE 8 – DC CURRENT GAIN

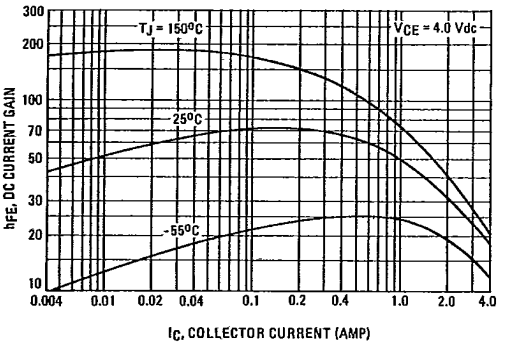



FIGURE 9 – COLLECTOR SATURATION REGION

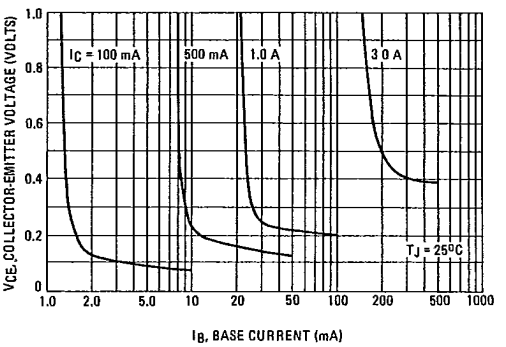



FIGURE 10 – TEMPERATURE COEFFICIENTS

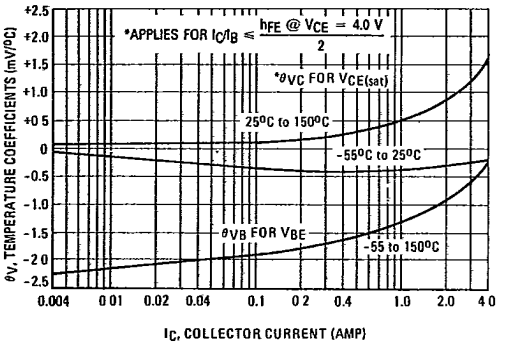
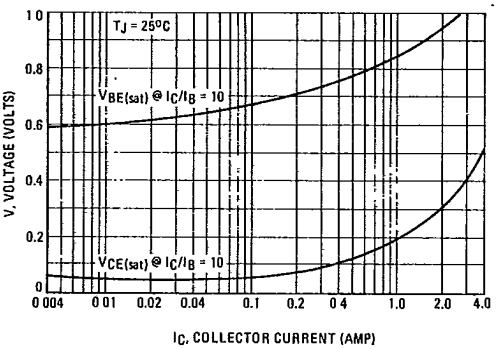



FIGURE 11 – "ON" VOLTAGES




3

FIGURE 12 – COLLECTOR CUT-OFF REGION

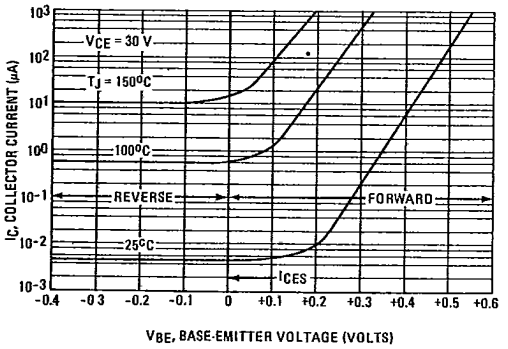



FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE