National Semiconductor

August 2, 2010

LMZ14202EXT

2A SIMPLE SWITCHER® Power Module with 42V Maximum Input Voltage for Military and Rugged Applications

Easy to use 7 pin package

Top View

Bottom View

30117786

TO-PMOD 7 Pin Package
10.16 x 13.77 x 4.57 mm (0.4 x 0.542 x 0.18 in)
θ_{JA} = 20°C/W, θ_{JC} = 1.9°C/W
RoHS Compliant

Electrical Specifications

- 12W maximum total output power
- Up to 2A output current
- Input voltage range 6V to 42V
- Output voltage range 0.8V to 6V
- Efficiency up to 90%

Key Features

- – 55°C to 125°C junction temperature range
- Integrated shielded inductor
- Simple PCB layout
- Flexible startup sequencing using external soft-start and precision enable
- Protection against inrush currents and faults such as input UVLO and output short circuit
- Single exposed pad and standard pinout for easy mounting and manufacturing
- Fast transient response for powering FPGAs and ASICs
- Low output voltage ripple
- Pin-to-pin compatible family:
  LMZ14203EXT/2EXT/1EXT (42V max 3A, 2A, 1A)
  LMZ14203/2/1 (42V max 3A, 2A, 1A)
  LMZ12003/2/1 (20V max 3A, 2A, 1A)
- Fully enabled for Webench® Power Designer

Applications

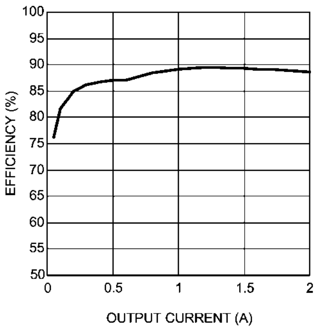
- Point of load conversions from 12V and 24V input rail
- Time critical projects
- Space constrained / high thermal requirement applications
- Negative output voltage applications (See AN-2027)

Performance Benefits

- Low radiated emissions / High radiated immunity
- Passes vibration standard
  MIL-STD-883 Method 2007.2 Condition A
  JESD22–B103B Condition 1
- Passes drop standard
  MIL-STD-883 Method 2002.3 Condition B
  JESD22–B110 Condition B

System Performance

Efficiency V_{IN} = 24V V_{OUT} = 5.0V



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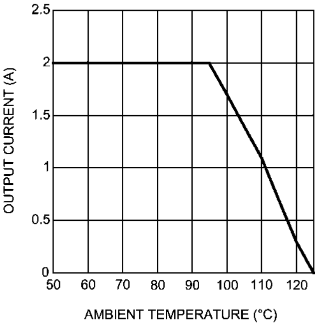
Thermal derating curve
V_{IN} = 24V, V_{OUT} = 5.0V,



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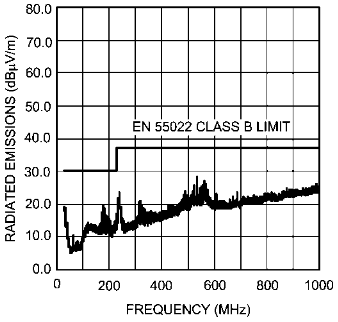
Radiated Emissions (EN 55022 Class B) from Evaluation Board



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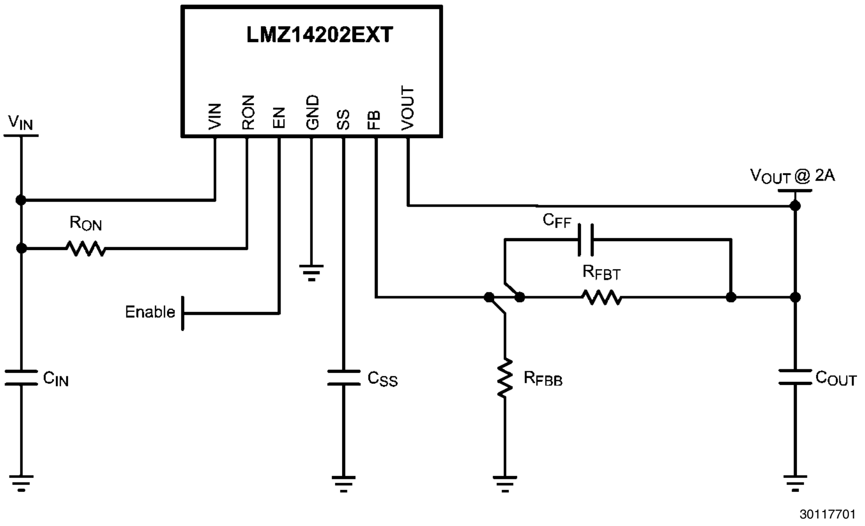
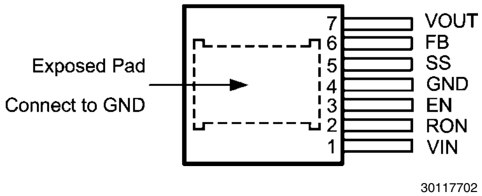
Simplified Application Schematic



Connection Diagram



Top View
7-Lead TO-PMOD

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LMZ14202EXTTZ	TO-PMOD-7	TZA07A	250 Units in Tape and Reel
LMZ14202EXTTZX	TO-PMOD-7	TZA07A	500 Units in Tape and Reel
LMZ14202EXTTZE	TO-PMOD-7	TZA07A	45 Units in a Rail

Pin Descriptions

Pin	Name	Description
1	VIN	Supply input — Nominal operating range is 6V to 42V . A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and exposed pad.
2	RON	On Time Resistor — An external resistor from V_{IN} to this pin sets the on-time of the application. Typical values range from 25k to 124k ohms.
3	EN	Enable — Input to the precision enable comparator. Rising threshold is 1.18V nominal; 90 mV hysteresis nominal. Maximum recommended input level is 6.5V.
4	GND	Ground — Reference point for all stated voltages. Must be externally connected to EP.
5	SS	Soft-Start — An internal 8 µA current source charges an external capacitor to produce the soft-start function. This node is discharged at 200 µA during disable, over-current, thermal shutdown and internal UVLO conditions.
6	FB	Feedback — Internally connected to the regulation, over-voltage, and short-circuit comparators. The regulation reference point is 0.8V at this input pin. Connected the feedback resistor divider between the output and ground to set the output voltage.

Pin	Name	Description
7	VOUT	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and exposed pad.
EP	EP	Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN, RON to GND	-0.3V to 43.5V
EN, FB, SS to GND	-0.3V to 7V
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility(*Note 2*)	± 2 kV

For soldering specifications:
see product folder at www.national.com and
www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings (*Note 1*)

V_{IN}	6V to 42V
EN	0V to 6.5V
Operation Junction Temperature	−55°C to 125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -55°C to +125°C. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24V, Vout = 3.3V

Symbol	Parameter	Conditions	Min (*Note 3*)	Typ (*Note 4*)	Max (*Note 3*)	Units
SYSTEM PARAMETERS						
Enable Control						
V_{EN}	EN threshold trip point	V_{EN} rising	**1.10**	1.18	**1.26**	V
$V_{EN\text{-}HYS}$	EN threshold hysteresis	V_{EN} falling		90		mV
Soft-Start						
I_{SS}	SS source current	V_{SS} = 0V	**4.9**	8	**11**	µA
$I_{SS\text{-}DIS}$	SS discharge current			-200		µA
Current Limit						
I_{CL}	Current limit threshold	d.c. average	**2.3**	2.6	**3.65**	A
ON/OFF Timer						
$t_{ON\text{-}MIN}$	ON timer minimum pulse width			150		ns
t_{OFF}	OFF timer pulse width			260		ns
Regulation and Over-Voltage Comparator						
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8V T_J = -55°C to 125°C I_O = 2A	**0.775**	0.795	**0.815**	V
		V_{SS} >+ 0.8V T_J = 25°C I_O = 10 mA	0.786	0.802	0.818	V
$V_{FB\text{-}OV}$	Feedback over-voltage protection threshold			0.92		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non Switching Input Current	V_{FB}= 0.86V		1		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0V		25		µA
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
$T_{SD\text{-}HYST}$	Thermal shutdown hysteresis	Falling		15		°C
θ_{JA}	Junction to Ambient	4 layer JEDEC Printed Circuit Board, 100 vias, No air flow		19.3		°C/W
		2 layer JEDEC Printed Circuit Board, No air flow		21.5		°C/W
θ_{JC}	Junction to Case	No air flow		1.9		°C/W
PERFORMANCE PARAMETERS						
ΔV_O	Output Voltage Ripple			8		mV_{PP}
$\Delta V_O/\Delta V_{IN}$	Line Regulation	V_{IN} = 12V to 42V, I_O= 2A		.01		%
$\Delta V_O/I_{OUT}$	Load Regulation	V_{IN} = 24V		1.5		mV/A

Symbol	Parameter	Conditions	Min (*Note 3*)	Typ (*Note 4*)	Max (*Note 3*)	Units
η	Efficiency	V_{IN} = 24V V_O = 3.3V I_O = 1A		86		%
η	Efficiency	V_{IN} = 24V V_O = 3.3V I_O = 2A		85		%

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.

Note 3: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 4: Typical numbers are at 25°C and represent the most likely parametric norm.

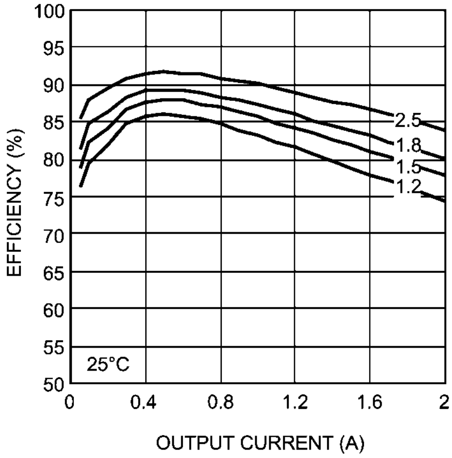
Note 5: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See AN-2024 and layout for information on device under test.

Note 6: Theta JA measured on a 1.705" x 3.0" four layer board, with one ounce copper, thirty five 12 mil thermal vias, no air flow, and 1W power dissipation. Refer to PCB layout diagrams

Typical Performance Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24V; Cin = 10uF X7R Ceramic; C_O = 100uF X7R Ceramic; Tambient = 25 C for efficiency curves and waveforms.

Efficiency 6V Input @ 25°C



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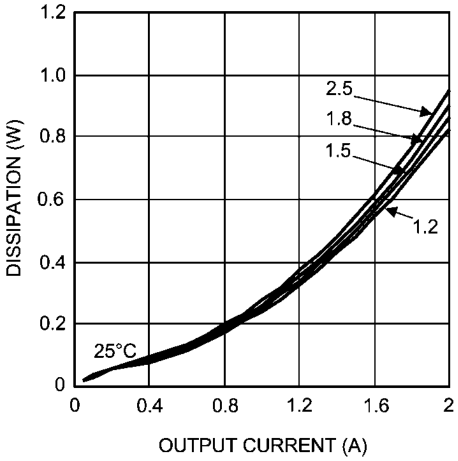
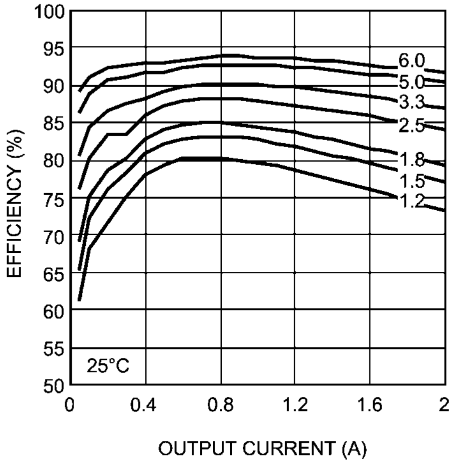
Dissipation 6V Input @ 25°C



30117732

Efficiency 12V Input @ 25°C



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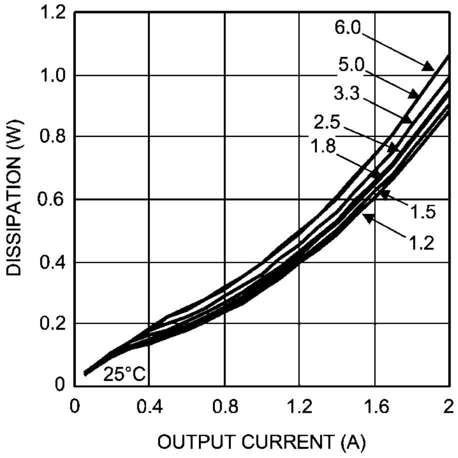
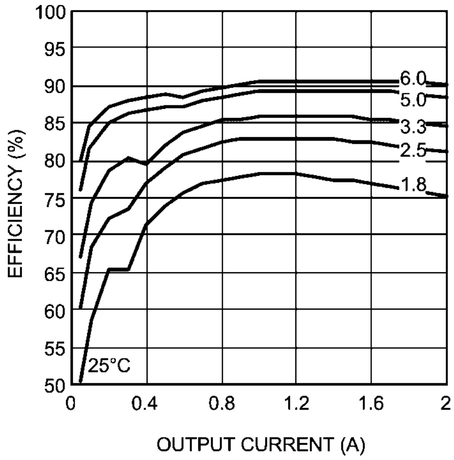
Dissipation 12V Input @ 25°C



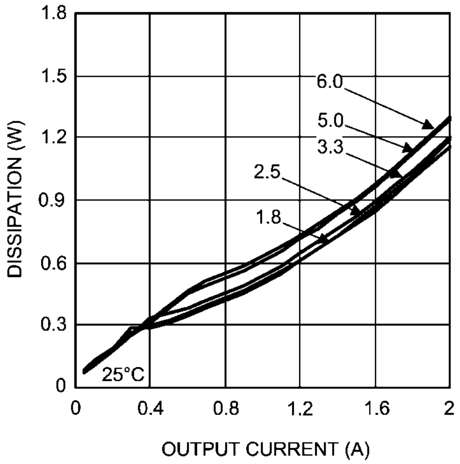
30117704

Efficiency 24V Input @ 25°C



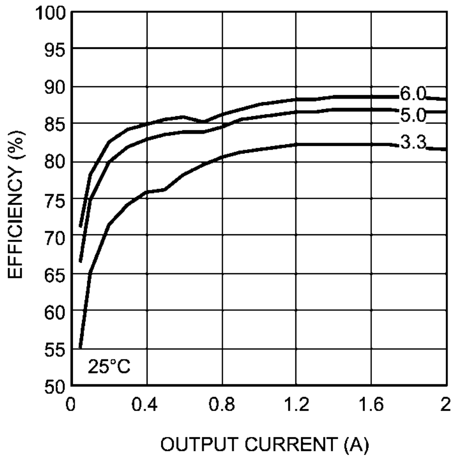
30117726

Dissipation 24V Input @ 25°C



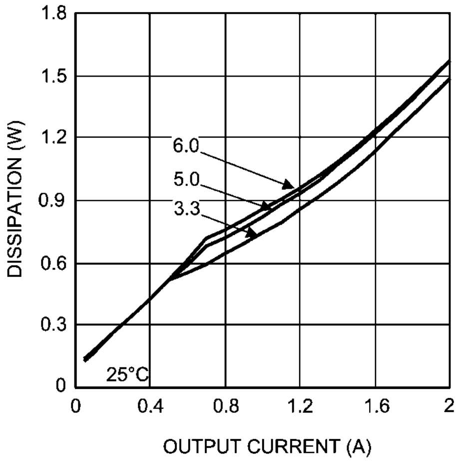
30117727

Efficiency 36V Input @ 25°C



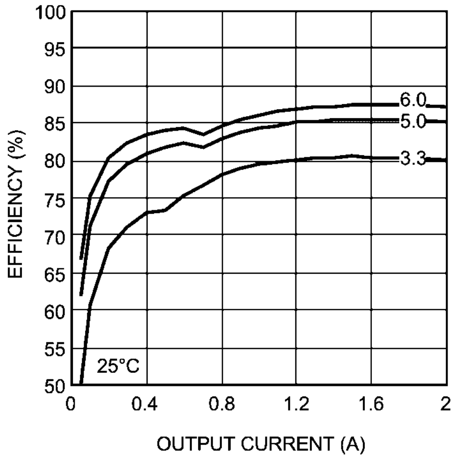
30117729

Dissipation 36V Input @ 25°C



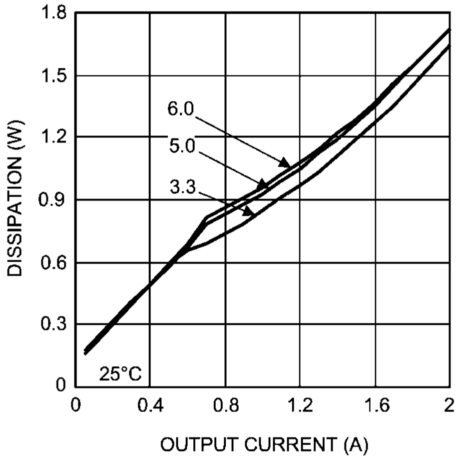
30117730

Efficiency 42V Input @ 25°C



30117750

Dissipation 42V Input @ 25°C



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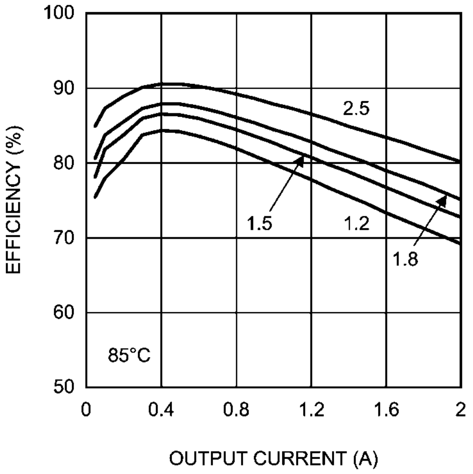
Efficiency 6V Input @ 85°C



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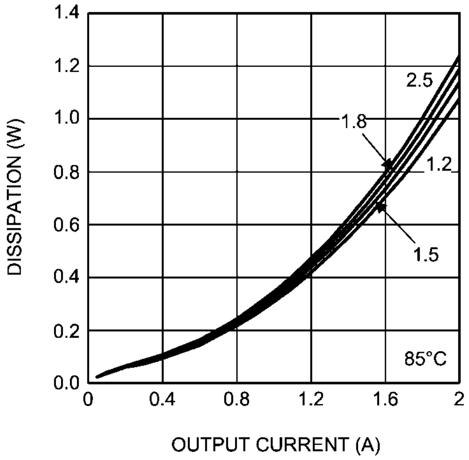
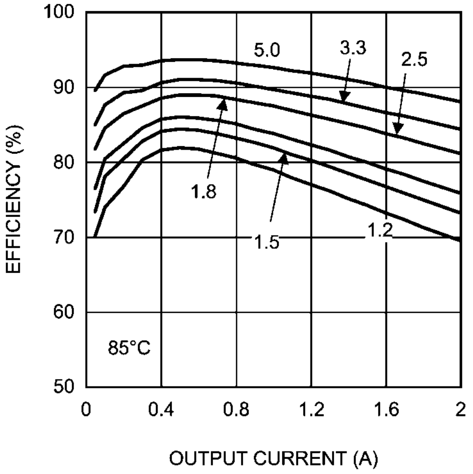
Dissipation 6V Input @ 85°C



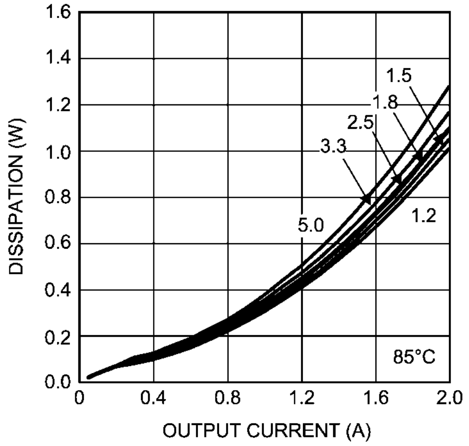
30117734

Efficiency 8V Input 85°C



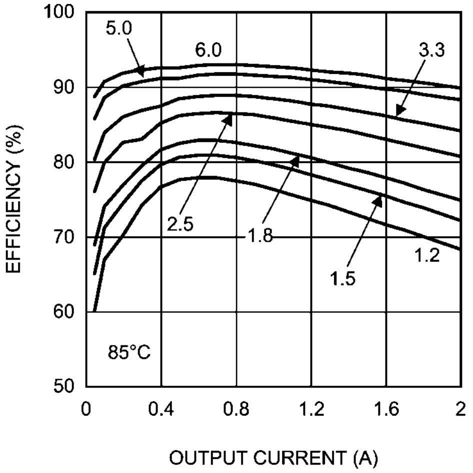
30117740

Dissipation 8V Input 85°C



30117741

Efficiency 12V Input@ 85°C



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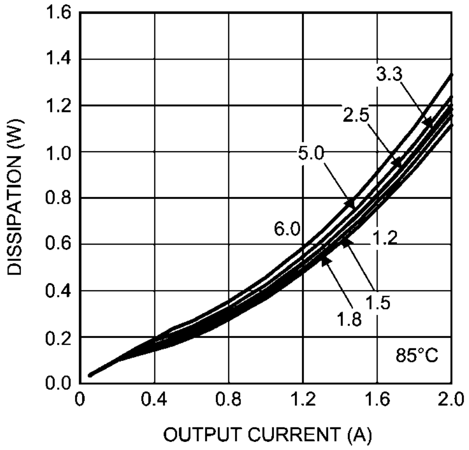
Dissipation 12V Input @ 85°C



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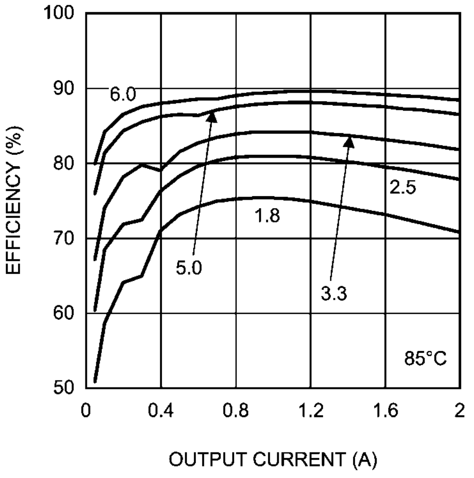

Efficiency 24V Input @ 85°C

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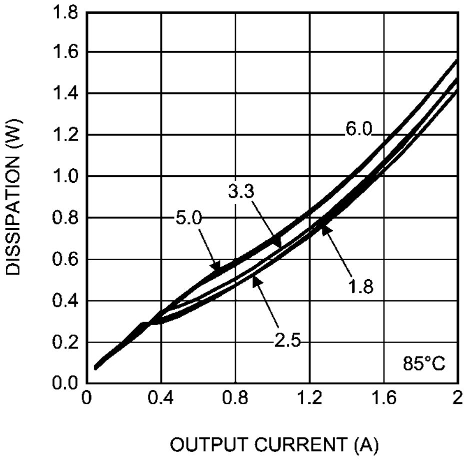

Dissipation 24V Input @ 85°C

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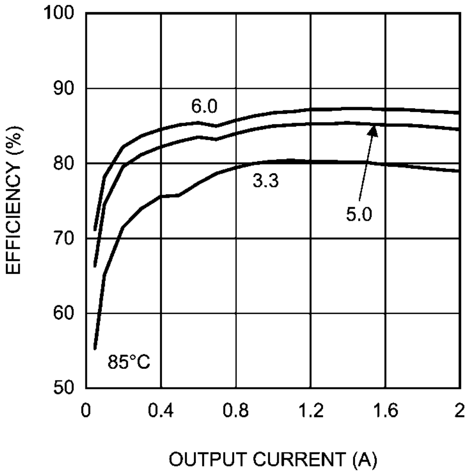

Efficiency 36V Input @ 85°C

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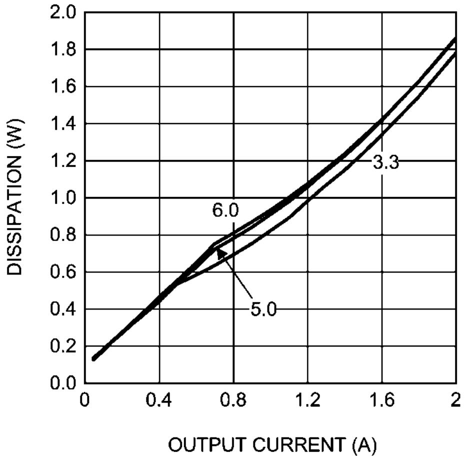

Dissipation 36V Input @ 85°C

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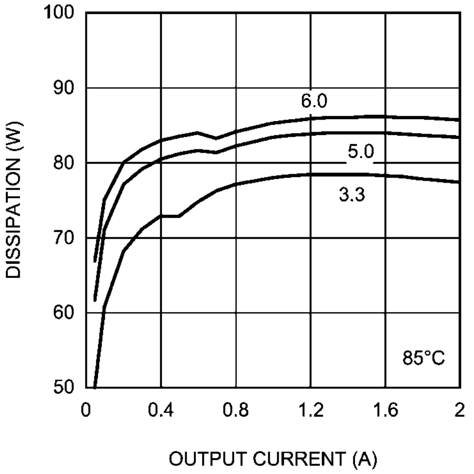

Efficiency 42V Input @ 85°C

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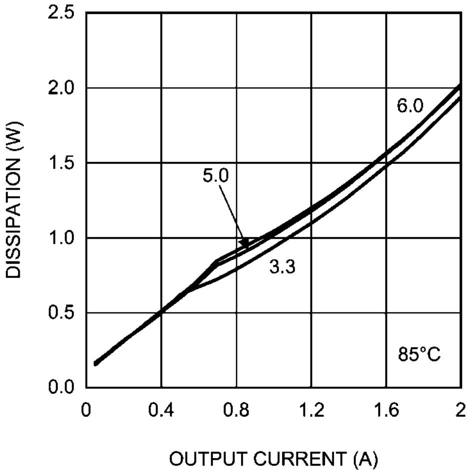
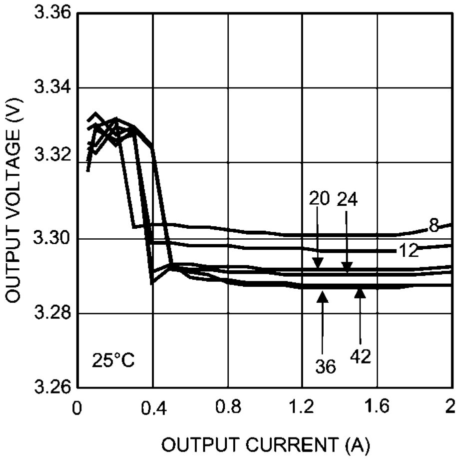


Dissipation 42V Input @ 85°C

30117753

Line and Load Regulation @ 25°C



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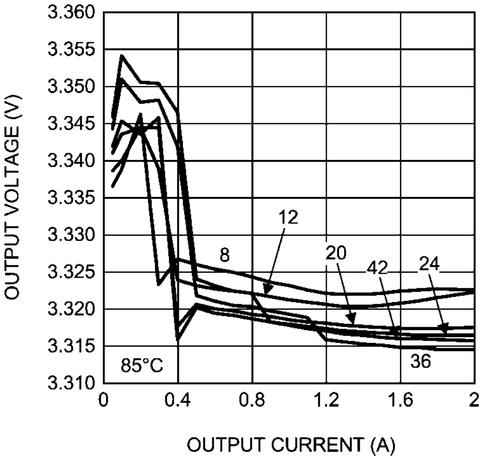
Line and Load Regulation @ 85°C



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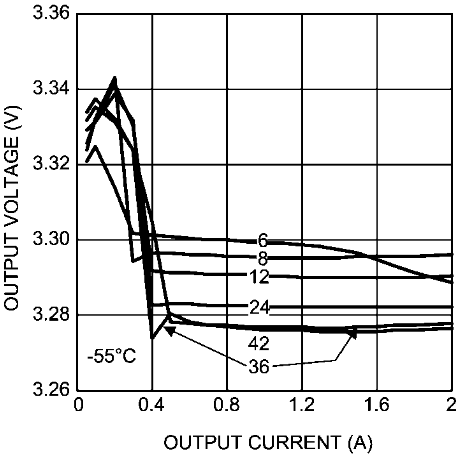
Line and Load Regulation @ –55°C



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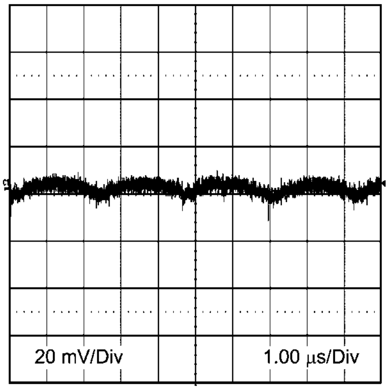
Output Ripple
$24V_{IN}$ $3.3V_O$ 2A, BW = 200 MHz



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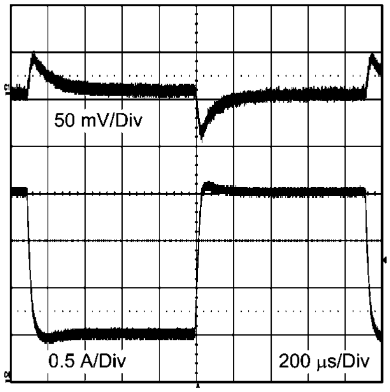
Transient Response
$24V_{IN}$ $3.3V_O$ 0.6A to 2A Step



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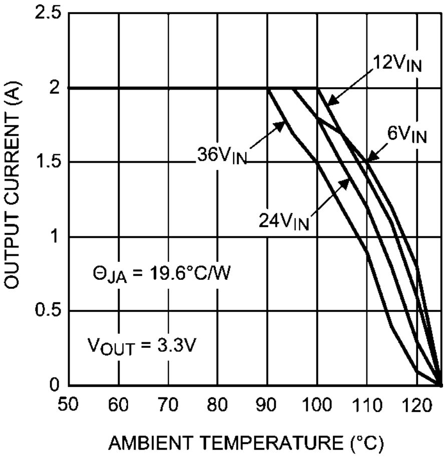
Thermal Derating V_{OUT} = 3.3V



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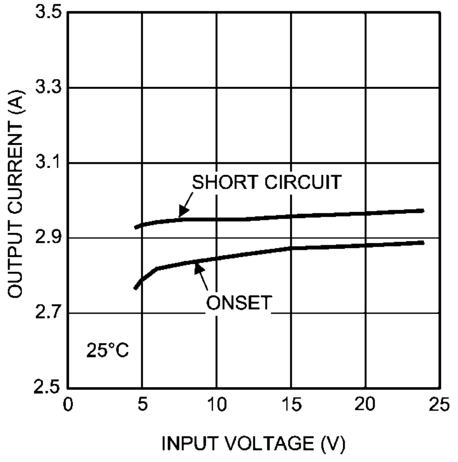
Current Limit 1.8V_{OUT} @ 25°C



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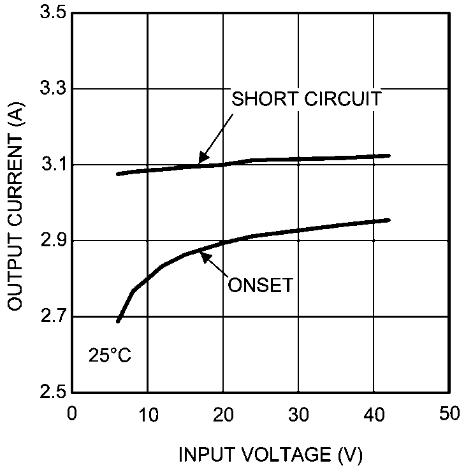
Current Limit 3.3V_{OUT} @ 25°C



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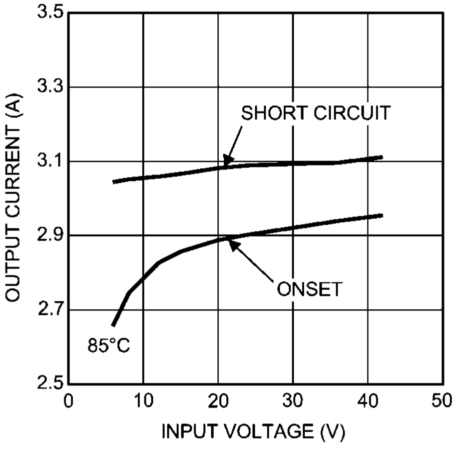
Current Limit 3.3V_{OUT} @ 85°C



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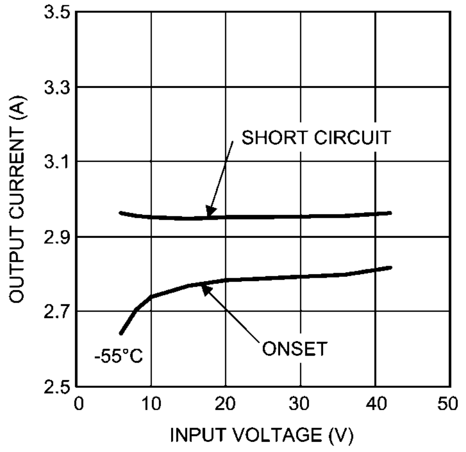
Current Limit 3.3V_{OUT} @ –55°C



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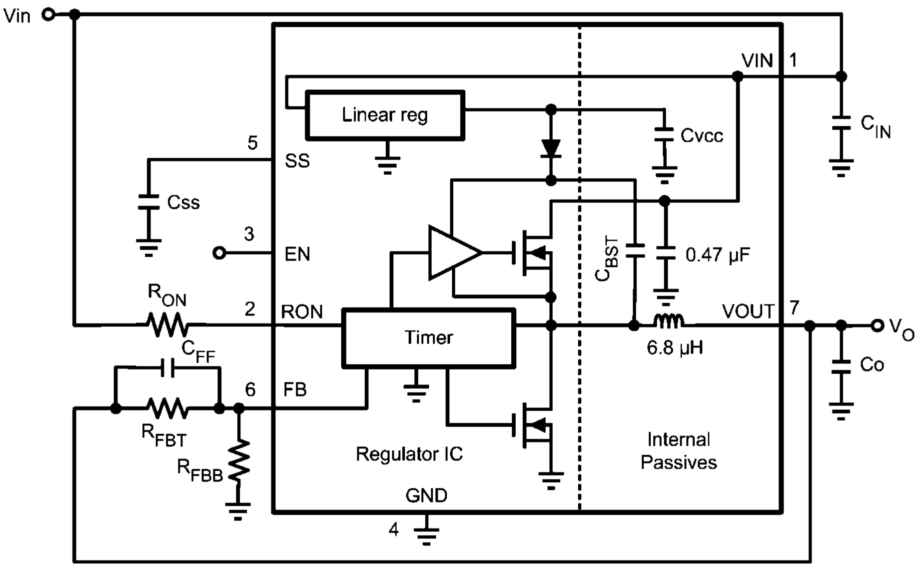
Application Block Diagram



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General Description

The LMZ14202EXT SIMPLE SWITCHER® power module is an easy-to-use step-down DC-DC solution capable of driving up to 2A load with exceptional power conversion efficiency, line and load regulation, and output accuracy. The LMZ14202EXT is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ14202EXT can accept an input voltage rail between 6V and 42V and deliver an adjustable and highly accurate output voltage as low as 0.8V. The LMZ14202EXT only requires three external resistors and four external capacitors to complete the power solution. The LMZ14202EXT is a reliable and robust design with the following protection features: thermal shutdown, input under-voltage lockout, output over-voltage protection, short-circuit protection, output current limit, and allows startup into a pre-biased output. A single resistor adjusts the switching frequency up to 1 MHz.

COT Control Circuit Overview

Constant On Time control is based on a comparator and an on-time one shot, with the output voltage feedback compared with an internal 0.8V reference. If the feedback voltage is below the reference, the main MOSFET is turned on for a fixed on-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that on-time is reduced with increasing input supply voltage. Following this on-time, the main MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the on-time cycle is repeated. Regulation is achieved in this manner.

Design Steps for the LMZ14202EXT Application

The LMZ14202EXT is fully supported by Webench® and offers the following: Component selection, electrical and thermal simulations as well as the build-it board for a reduction in design time. The following list of steps can be used to manually design the LMZ14202EXT application.

- Select minimum operating V_{IN} with enable divider resistors
- Program V_O with divider resistor selection
- Program turn-on time with soft-start capacitor selection
- Select C_O
- Select C_{IN}
- Set operating frequency with R_{ON}
- Determine module dissipation
- Layout PCB for required thermal performance

ENABLE DIVIDER, R_{ENT} AND R_{ENB} SELECTION

The enable input provides a precise 1.18V band-gap rising threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typ) of hysteresis resulting in a falling threshold of 1.09V. The maximum recommended voltage into the EN pin is 6.5V. For applications where the midpoint of the enable divider exceeds 6.5V, a small zener can be added to limit this voltage.

The function of this resistive divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14202EXT output rail. The two resistors should be chosen based on the following ratio:

$R_{ENT} / R_{ENB} = (V_{IN\ UVLO}/ 1.18V) – 1$ ***(1)***

The LMZ14202EXT demonstration and evaluation boards use 11.8kΩ for R_{ENB} and 68.1kΩ for R_{ENT} resulting in a rising UVLO of 8V. This divider presents 6.25V to the EN input when the divider input is raised to 42V.

OUTPUT VOLTAGE SELECTION

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation an on-time cycle is initiated when the voltage on the FB pin falls below 0.8V. The main MOSFET on-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8V. As long as the voltage at FB is above 0.8V, on-time cycles will not occur.

The regulated output voltage determined by the external divider resistors RFBT and RFBB is:

$V_O = 0.8V * (1 + R_{FBT} / R_{FBB})$ ***(2)***

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$R_{FBT} / R_{FBB} = (V_O / 0.8V) - 1$ ***(3)***

These resistors should be chosen from values in the range of 1.0 kohm to 10.0 kohm.

For V_O = 0.8V the FB pin can be connected to the output directly so long as an output preload resistor remains that draws more than 20uA. Converter operation requires this minimum load to create a small inductor ripple current and maintain proper regulation when no load is present.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , C_{FF} and R_{ON} is included in the applications schematic.

SOFT-START CAPACITOR SELECTION

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turn-on, after all UVLO conditions have been passed, an internal 8uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady state operation is given by the formula:

$t_{SS} = V_{REF} * C_{SS} / Iss = 0.8V * C_{SS} / 8uA$ ***(4)***

This equation can be rearranged as follows:

$C_{SS} = t_{SS} * 8\ \mu A / 0.8V$ ***(5)***

Use of a 0.022µF capacitor results in 2.2msec soft-start duration which is recommended as a minimum value.

As the soft-start input exceeds 0.8V the output of the power stage will be in regulation. The soft-start capacitor continues charging until it reaches approximately 3.8V on the SS pin. Voltage levels between 0.8V and 3.8V have no effect on other circuit operation. Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200 µA current sink.

- The enable input being “pulled low”
- Thermal shutdown condition
- Over-current fault
- Internal Vcc UVLO (Approx 4V input to V_{IN})

C_O SELECTION

None of the required C_O output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst case minimum ripple current rating of $0.5 * I_{LR\ P-P}$, as calculated in equation (19) below. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Ceramic capacitors or other low ESR types are recommended. See AN-2024 for more detail.

The following equation provides a good first pass approximation of C_O for load transient requirements:

$C_O \geq I_{STEP} * V_{FB} * L * V_{IN} / (4 * V_O * (V_{IN} — V_O) * V_{OUT-TRAN})$ ***(6)***

Solving:

$C_O \geq 2A*0.8V*10\mu H*24V / (4*3.3V*(24V — 3.3V)*33mV)$
$\geq 43\mu F$ ***(7)***

The LMZ14202EXT demonstration and evaluation boards are populated with a 100 uF 6.3V X5R output capacitor. Locations for extra output capacitors are provided. See AN-2024 for locations.

C_{IN} SELECTION

The LMZ14202EXT module contains an internal 0.47 µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst case input ripple current rating is dictated by the equation:

$I(C_{IN(RMS)}) \cong 1/2 * I_O * \sqrt{}\,(D / 1-D)$ ***(8)***

where $D \cong V_O / V_{IN}$

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 * V_O$).

Recommended minimum input capacitance is 10uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of input ripple voltage ΔV_{IN} be maintained then the following equation may be used.

$C_{IN} \geq I_O * D * (1–D) / f_{SW-CCM} * \Delta V_{IN}$ ***(9)***

If ΔV_{IN} is 1% of V_{IN} for a 24V input to 3.3V output application this equals 240 mV and f_{SW} = 400 kHz.

$C_{IN} \geq 2A * 3.3V/24V * (1– 3.3V/24V) / (400000 * 0.240\ V)$
$\geq 2.5\mu F$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

R_{ON} RESISTOR SELECTION

Many designs will begin with a desired switching frequency in mind. For that purpose the following equation can be used.

$f_{SW(CCM)} \cong V_O / (1.3 * 10^{-10} * R_{ON})$ ***(10)***

This can be rearranged as

$R_{ON} \cong V_O / (1.3 * 10^{-10} * f_{SW(CCM)})$***(11)***

The selection of RON and $f_{SW(CCM)}$ must be confined by limitations in the on-time and off-time for the COT control section.

The on-time of the LMZ14202EXT timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$t_{ON} = (1.3 * 10^{-10} * R_{ON}) / V_{IN}$ ***(12)***

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the on-time at maximum V_{IN} is greater than 150 ns. The on-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by the following equation:

$f_{SW(MAX)} = V_O / (V_{IN(MAX)} * 150\ nsec)$ ***(13)***

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum on-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$R_{ON} \geq V_{IN(MAX)} * 150\ nsec / (1.3 * 10^{-10})$ ***(14)***

If R_{ON} calculated in (11) is less than the minimum value determined in (14) a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

Additionally note, the minimum off-time of 260 ns limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

Discontinuous Conduction and Continuous Conduction Modes

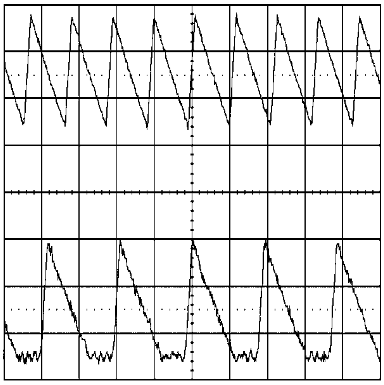
At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the off-time. Note that during the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next on-time period starts when the voltage on the at the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained since conduction and switching losses are reduced with the smaller load and lower switching frequency. Operating frequency in DCM can be calculated as follows:

$f_{SW(DCM)} \cong V_O*(V_{IN}-1)*10\mu H*1.18*10^{20}*I_O/(V_{IN}–V_O)*R_{ON}^2$ ***(15)***

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using equation 7 above.

Following is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.

CCM and DCM Operating Modes
V_{IN} = 24V, V_O = 3.3V, I_O = 2A/0.32A 2 µsec/div



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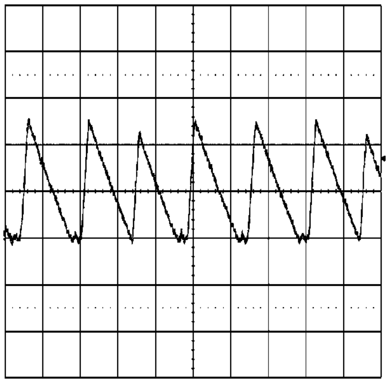
The approximate formula for determining the DCM/CCM boundary is as follows:

$I_{DCB} \cong V_O*(V_{IN}-V_O)/(2*10\ \mu H*f_{SW(CCM)}*V_{IN})$ ***(16)***

Following is a typical waveform showing the boundary condition.

Transition Mode Operation
V_{IN} = 24V, V_O = 3.3V, I_O = 0.35A 2 µsec/div



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The inductor internal to the module is 10 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$I_{LR\ P-P}=V_O*(V_{IN}-V_O)/(10\mu H*f_{SW}*V_{IN})$ ***(17)***

Where V_{IN} is the maximum input voltage and f_{SW} is determined from equation 10.

If the output current I_O is determined by assuming that I_O = I_L, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

POWER DISSIPATION AND BOARD THERMAL REQUIREMENTS

For the design case of V_{IN} = 24V, V_O = 3.3V, I_O = 2A, $T_{AMB\ (MAX)}$ = 85°C , and $T_{JUNCTION}$ = 125°C, the device must see a thermal resistance from case to ambient of:

$\theta_{CA} < (T_{J\text{-}MAX} — T_{AMB(MAX)}) / P_{IC\text{-}LOSS} - \theta_{JC}$ ***(18)***

Given the typical thermal resistance from junction to case to be 1.9 °C/W. Use the 85°C power dissipation curves in the Typical Performance Characteristics section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 1.5W.

θ_{CA} = (125 — 85) / 1.5W — 1.9) = 24.8

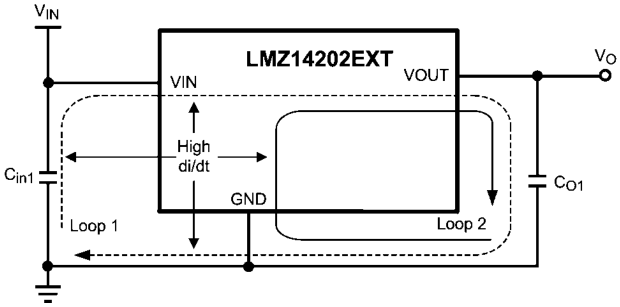
To reach θ_{CA} = 24.8, the PCB is required to dissipate heat effectively. With no airflow and no external heat, a good estimate of the required board area covered by 1 oz. copper on both the top and bottom metal layers is:

Board Area_cm^2 = 500°C x cm^2/W / θ_{JC} ***(19)***

As a result, approximately 20.2 square cm of 1 oz copper on top and bottom layers is required for the PCB design. The PCB copper heat sink must be connected to the exposed pad. Approximately thirty six, 10mils (254 µm) thermal vias spaced 59mils (1.5 mm) apart must connect the top copper to the bottom copper. For an example of a high thermal performance PCB layout, refer to the Evaluation Board application note AN-2024.

PC BOARD LAYOUT GUIDELINES

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.



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1. Minimize area of switched current loops.

From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14202EXT. Therefore place C_{IN1} as close as possible to the LMZ14202EXT VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. Have a single point ground.

The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. Minimize trace length to the FB pin.

Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The trace are from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14202EXT to minimize noise.

4. Make input and output bus connections as wide as possible.

This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with minimum via diameter of 10mils (254 µm) thermal vias spaced 59mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

Additional Features

OUTPUT OVER-VOLTAGE COMPARATOR

The voltage at FB is compared to a 0.92V internal reference. If FB rises above 0.92V the on-time is immediately terminated. This condition is known as over-voltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET on-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

CURRENT LIMIT

Current limit detection is carried out during the off-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 2.6 A (typical) the current limit comparator disables the start of the next on-time period. The next switching cycle will occur only if the FB input is less than 0.8V and the inductor current has decreased below 2.6 A. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds 2.6A, further on-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer off-time. It should also be noted that current limit is dependent on both duty cycle and temperature as illustrated in the graphs in the typical performance section.

THERMAL PROTECTION

The junction temperature of the LMZ14202EXT should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145 °C (typ Hyst = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require application derating at elevated temperatures.

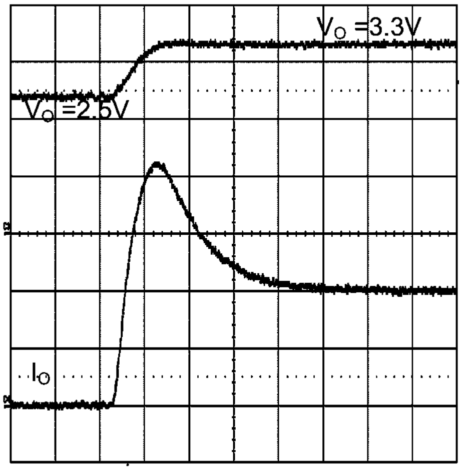
ZERO COIL CURRENT DETECTION

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next on-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

PRE-BIASED STARTUP

The LMZ14202EXT will properly start up into a pre-biased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The following scope capture shows proper behavior during this event.

Pre-Biased Startup



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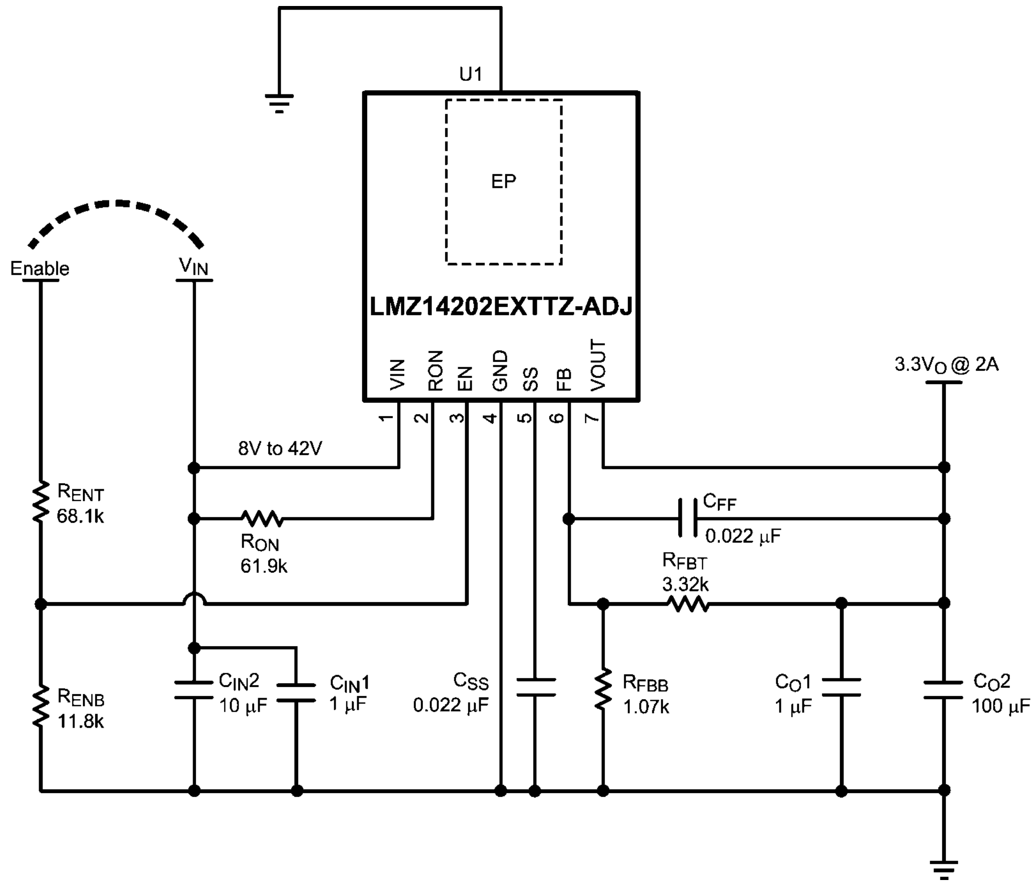
Evaluation Board Schematic Diagram



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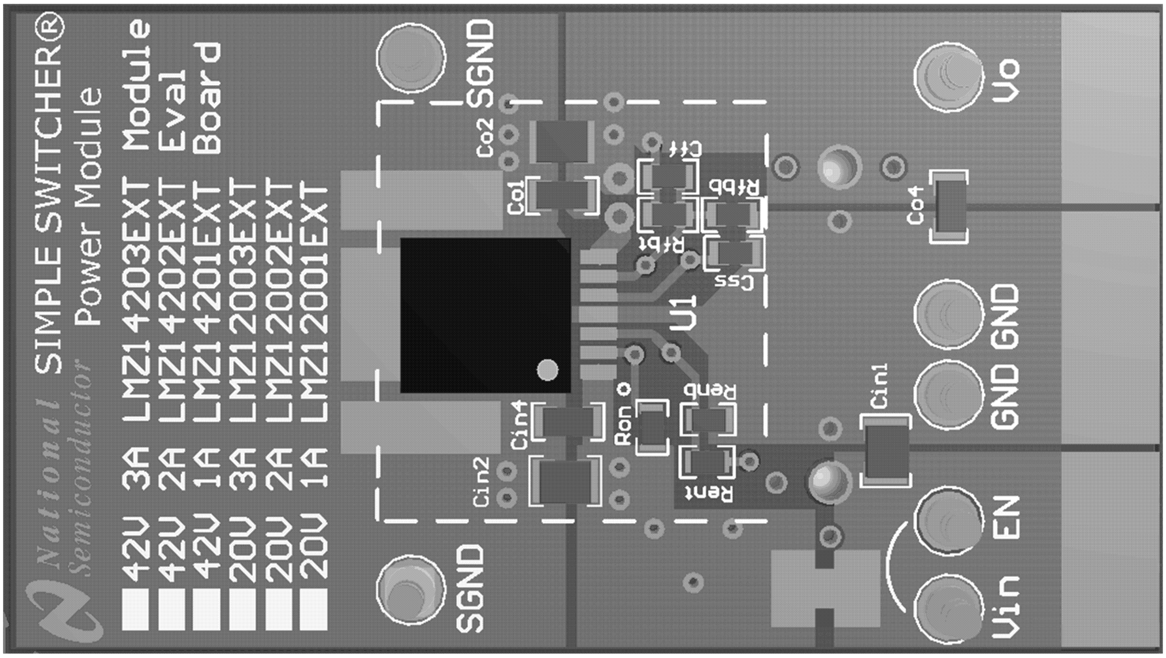
Ref Des	Description	Case Size	Case Size	Manufacturer P/N
U1	SIMPLE SWITCHER ®	TO-PMOD-7	National Semiconductor	LMZ14202EXTTZ-ADJ
C_{in1}	1 µF, 50V, X7R	1206	Taiyo Yuden	UMK316B7105KL-T
C_{in2}	10 µF, 50V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{O1}	1 µF, 50V, X7R	1206	Taiyo Yuden	UMK316B7105KL-T
C_{O2}	100 µF, 6.3V, X7R	1210	Taiyo Yuden	JMK325BJ107MM-T
R_{FBT}	3.32 kΩ	0603	Vishay Dale	CRCW06033K32FKEA
R_{FBB}	1.07 kΩ	0603	Vishay Dale	CRCW06031K07FKEA
R_{ON}	61.9 kΩ	0603	Vishay Dale	CRCW060361k9FKEA
R_{ENT}	68.1 kΩ	0603	Vishay Dale	CRCW060368k1FKEA
R_{ENB}	11.8 kΩ	0603	Vishay Dale	CRCW060311k8FKEA
C_{FF}	22 nF, ±10%, X7R, 16V	0603	TDK	C1608X7R1H223K
C_{SS}	22 nF, ±10%, X7R, 16V	0603	TDK	C1608X7R1H223K



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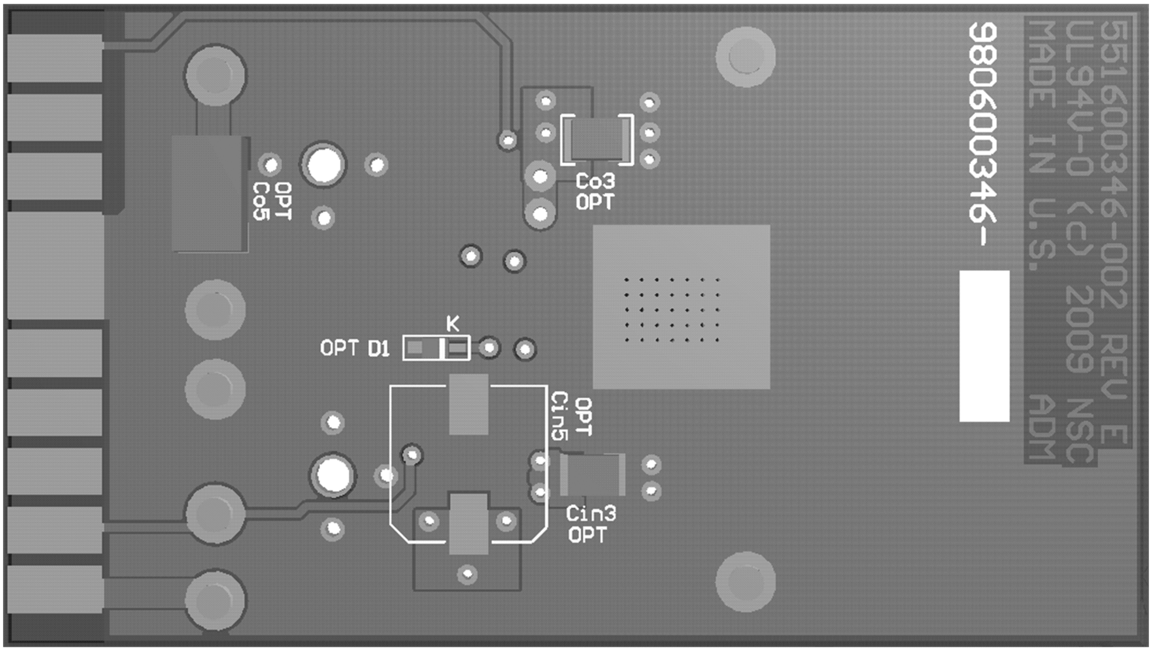

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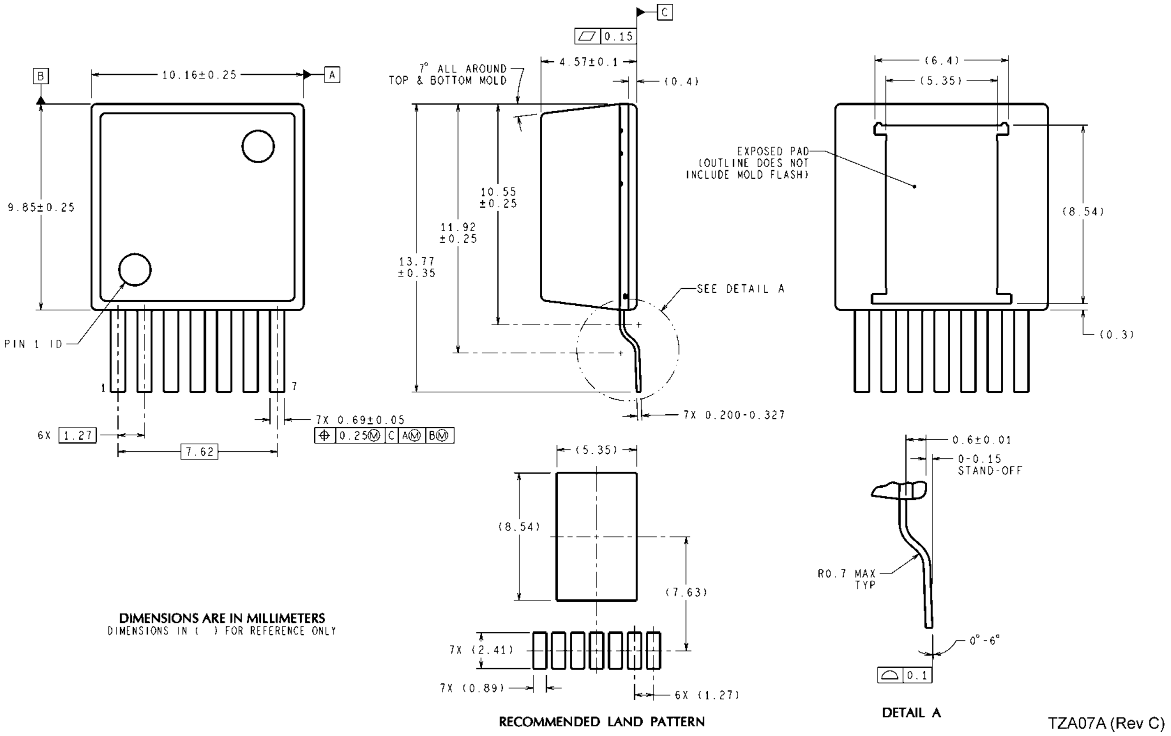
Physical Dimensions inches (millimeters) unless otherwise noted



7-Lead TZA Package
NS Package Number TZA07A

Notes

Notes

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