EL4583C

Sync Separator, 50% Slice, S-H, Filter, H_{OUT}

Features

- NTSC, PAL and SECAM sync separation
- Single supply, +5V operation
- Precision 50% slicing, internal caps
- Built in programmable color burst filter
- Decodes non-standard verticals
- Horizontal sync output
- Sync. pulse amplitude output
- Same socket can be used for 8-pin EL4581
- Low power CMOS
- Detects loss of signal
- Resistor programmable scan rate
- Few external components
- Available in 16-Pin DIP and SO-16 pkg.

Applications

- Video special effects
- Video test equipment
- Video distribution
- Multimedia
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4583CN	−40°C to +85°C	16-Pin DIP	MDP0031
EL4583CS	−40°C to +85°C	16-Lead SO	MDP0027

General Description

The EL4583C extracts timing from video sync in NTSC, PAL, and SECAM systems, and non standard formats, or from computer graphics operating at higher scan rates. Timing adjustment is via an external resistor. Input without valid vertical interval (no serration pulses) produces a default vertical output.

A larger package (16-pin) is used for greater flexibility. The "core" pins match the same pin functions of the 8-pin (EL4581C etc.) for substitution in applications not requiring these features.

Outputs are: **composite sync, vertical sync, filter, burst/back porch, horizontal, no signal detect, level,** and **odd/even output** (in interlaced scan formats only).

The EL4583C sync slice level is set to a mid-point halfway between sync tip and the blanking level. This 50% point is determined by two internal sample and hold circuits that track sync tip and back porch levels. It provides hum and noise rejection and compensates for input levels of 0.5V to $2.0V_{p\text{-}p}$.

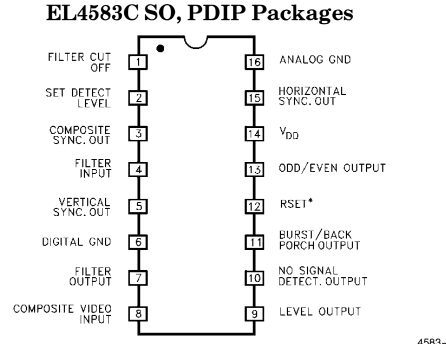
A built in filter attenuates the chroma signal to prevent color burst from disturbing the 50% sync slice. Cut off frequency is set by a resistor to ground from the **Filter Cut Off** pin. The filter can be by-passed, the video signal is fed to the **Video Input**.

A DC voltage, twice the sync amplitude, from the **Level Output** pin drives AGC circuits. A TTL/CMOS compatible **No Signal Detect Output** signals a loss or reduction in input signal level. A resistor sets the **Set Detect Level**.

The EL4583C is manufactured using Elantec's high performance analog CMOS process.

Connection Diagram

EL4583C SO, PDIP Packages



Top View

*Note: RSET must be a 1% resistor.

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Pin Voltages	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C	Operating Temperature Range	−40°C to +85°C
Lead Temperature	260°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, RSET = 681k, RF = 22k, RLV = 82k)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2.5	4	I	mA
Clamp Voltage	Pins 4, 8, unloaded	25°C	1.3	1.55	1.8	I	V
Discharge Current	Pins 4, 8, with Signal (Note 2) No Signal	25°C	3	1 6	12	I I	µA
Clamp Charge Current	Pins 4, 8, V_{IN} = IV	25°C	2	3	4	I	mA
Ref. Voltage V_{REF}	Pin 12, V_{DD} = 5V (Note 3)	25°C	1.5	1.75	2	I	V
Filter Reference Voltage, VRF	Pin 1	25°C	0.35	0.5	0.65	I	V
Level Reference Current	Pin 2 (Note 4)	25°C	1.5	2.5	3.5	I	µA
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA	25°C		350	800	I	mV
V_{OH} Output High Voltage	I_{OH} = −40 µA I_{OH} = −1.6 mA	25°C	4 2.4	 4		IV I	V

Note 1: No video signal, outputs unloaded.
Note 2: At loss of signal (pin 10 high) the pull down current source switches to a value of 10 µA.
Note 3: Tested for V_{DD} 5V ±5%.
Note 4: Current sourced from pin 2 is V_{REF}/RSET.

TD is 2.3in

Dynamic Characteristics

RF = 22 kΩ, RSET = 681 kΩ, V_{DD} = 5V, 1 V_{p-p} VIDEO, T_A = 25°C, C_L = 15 pF, I_{OH} = −1.6 mA, I_{OL} = 1.6 mA

Parameter	Description	Min	Typ	Max	Test Level	Units
Horizontal Pulse Width, Pin 15, t_H	(Note 5)	3.8	5	6.2	I	µs
Vertical Sync Width, Pin 5, t_{VS}	(Note 6)		195		I	µs
Burst/Back Porch Width, Pin 11, t_B	(Note 5)	2.7	3.7	4.7	I	µs
Filter Attenuation	F_{IN} = 3.6 MHz (Note 7)		12		IV	dB
Comp. Sync Prop. Delay, t_{CS}	V_{IN} (Pin 4)—Comp Sync		250	400	I	ns
Input Dynamic Range	p-p NTSC Signal	0.4		2	I	V
Slice Level	Input Voltage = 1 V_{p-p} V_{SLICE}/V_{BLANK}	40% 40%	50% 50%	60% 60%	I IV	
Level Out, Pin 9	Input Voltage = 1 V_{p-p} Pin 4	555	620	685	I	mV
Vertical Sync Default Time, t_{VSD}	(Note 8)	27	36	45	I	µs
Loss of Signal Time-Out	Pin 10	400	600	800	I	µs
Burst/Back Porch Delay, t_{BD}	See Figure 4		250	400	V	µs

Note 5: Width is a function of RSET.
Note 6: c/s, Vertical, Back porch and H are all active low, V_{OH} = 0.8V. Vertical is 3H lines wide of NTSC signal.
Note 7: Attenuation is a function of RF. See filter typical characteristics.
Note 8: Vertical pulse width in absence of serrations on input signal.

Pin Description

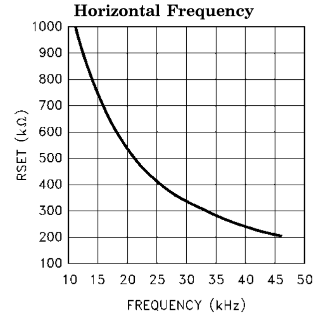
Pin No.	Pin Name	Function
1	Filter Cut-Off	A resistor RF connected between this input and ground determines the input filter characteristic. Increasing RF increases the filter 3.58 MHz color burst attenuation. See the graph showing filter characteristics.
2	Set Detect Level	A resistor RLV connected between pin 2 and ground determines the value of the minimum signal which will trigger the loss of signal output on pin 10. The relationship is V_PMIN = 0.75 RLV/RSET, where V_PMIN is the minimum detected sync pulse amplitude applied to pin 4. See characterization curve.
3	Composite Sync Output	This output replicates all the sync inputs on the input video.
4	Filter Input	The filter is a 3 pole active filter with a gain of 2, designed to produce a constant phase delay of nominally 260 ns with signal amplitude. Resistor RF on pin 1 controls the filter cut-off. An internal clamp sets the minimum voltage on pin 4 at 1.55V when the input becomes low impedance. Above the clamp voltage, an input current of 1 µA charges the input coupling capacitor. With loss of signal, the current source switches to a value of 10 µA, for faster signal recovery.
5	Vertical Sync Output	The vertical sync output is synchronous with the first serration pulse rising edge in the vertical interval of the input signal and ends on the trailing edge of the first equalizing Output pulse after the vertical interval. It will therefore be slightly more than 3H lines wide.

Pin Description — Contd.

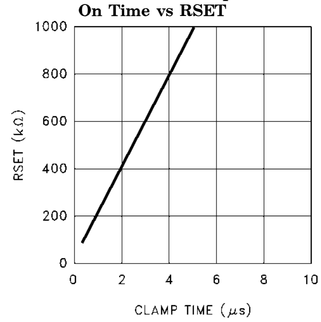
Pin No.	Pin Name	Function
6	Digital Ground	This is the ground return for digital buffer outputs.
7	Filter Output	Output of the active 3 pole filter which has its input on pin 4. It is recommended to ac couple the output to pin 8.
8	Video Input	This input can be directly driven by the signal if it is desired to bypass the filter, for example, in the case of strong clean signals. This input is 6 dB less sensitive than the filter input.
9	Level Output	This pin provides an analog voltage which is nominally equal to twice the sync pulse amplitude of the video input signal applied to pin 4. It therefore provides an indication of signal strength.
10	No Signal Detect Output	This is a digital output which goes high when either a) loss of input signal or b) the input signal level falls below a predetermined amplitude as set by RLV on pin 2. There will be several horizontal lines delay before the output is initiated.
11	Burst/Back Porch Output	The start of back porch output is triggered on the trailing edge of normal H sync, and on the rising edge of serration pulses in the vertical interval. The pulse is timed out internally to produce a one-shot output. The pulse width is a function of RSET. This output can be used for d.c. restore functions where the back porch level is a known reference.
12	RSET	The current through the resistor RSET determines the timing of the functions within the I.C. These functions include the sampling of the sync pulse 50% point, back porch output and the 2H eliminator. For faster scan rates, the resistor needs to be reduced inversely. For NTSC 15.7 kHz scan rate RSET is 681k 1%. RSET must be a 1% resistor.
13	Odd/Even Output	Odd-even output is low for even field and high for odd field. The operation of this circuit has been improved for rejecting spurious noise pulses such as those present in VCR signals.
14	V_{DD} 5V	The internal circuits are designed to have a high immunity to supply variations, although as with most I.C.s a 0.1 μF decoupling capacitor is advisable.
15	Horizontal Sync Output	This output produces only true H pulses of nominal width 5 μs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2H eliminator circuit.
16	Analog Ground	This is the ground return for the signal paths in the chips, RSET, RF and RLV.

Typical Performance Characteristics

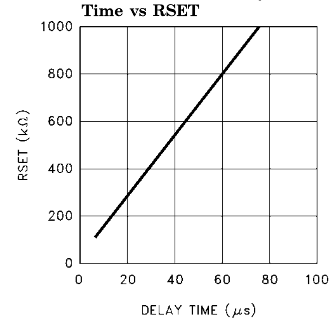
RSET vs Horizontal Frequency



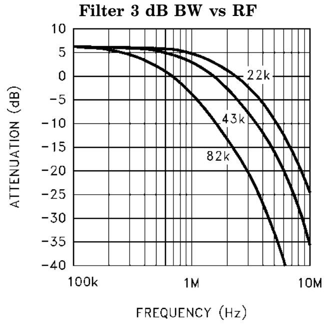
Back Porch Clamp On Time vs RSET



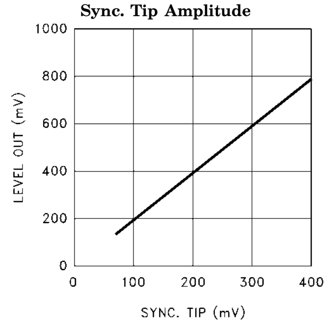
Vertical Default Delay Time vs RSET



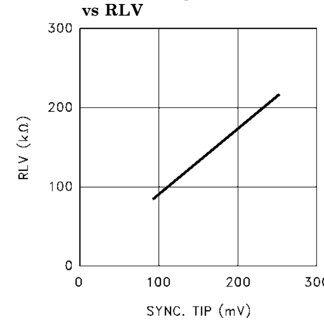
Filter 3 dB BW vs RF



Level Out (Pin 9) vs Sync. Tip Amplitude



Minimum Signal Detect vs RLV



*Note 1

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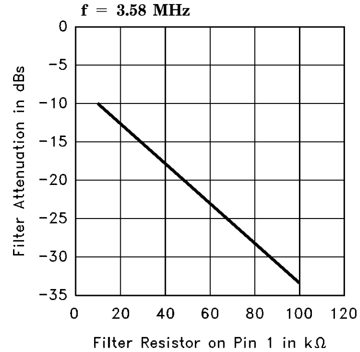
Filter Attenuation vs RF @ f = 3.58 MHz



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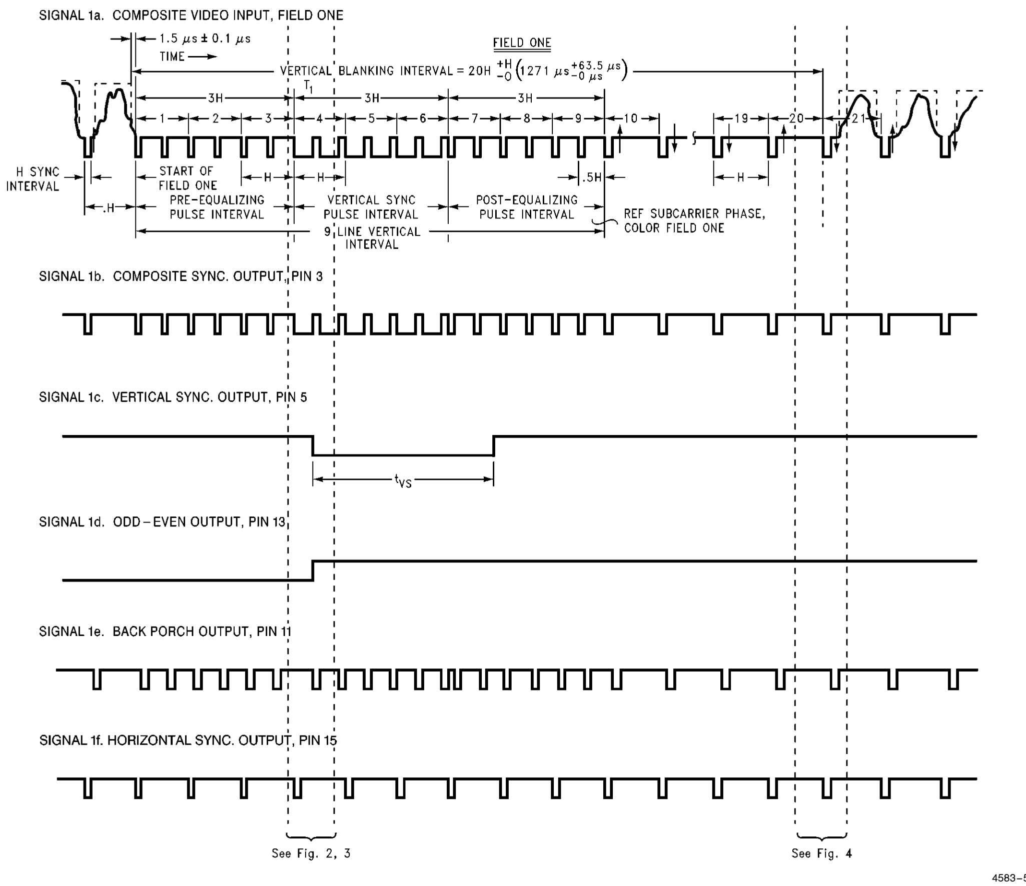
Note 1: For RLV < 100 kΩ, no signal detect output (pin 10) will default high at minimum signal sensitivity specification, or at complete loss of signal.

Timing Diagram



Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

f. Horizontal sync output produces the true "H" pulses of nominal width of 5μs. It has the same delay as the composite sync.

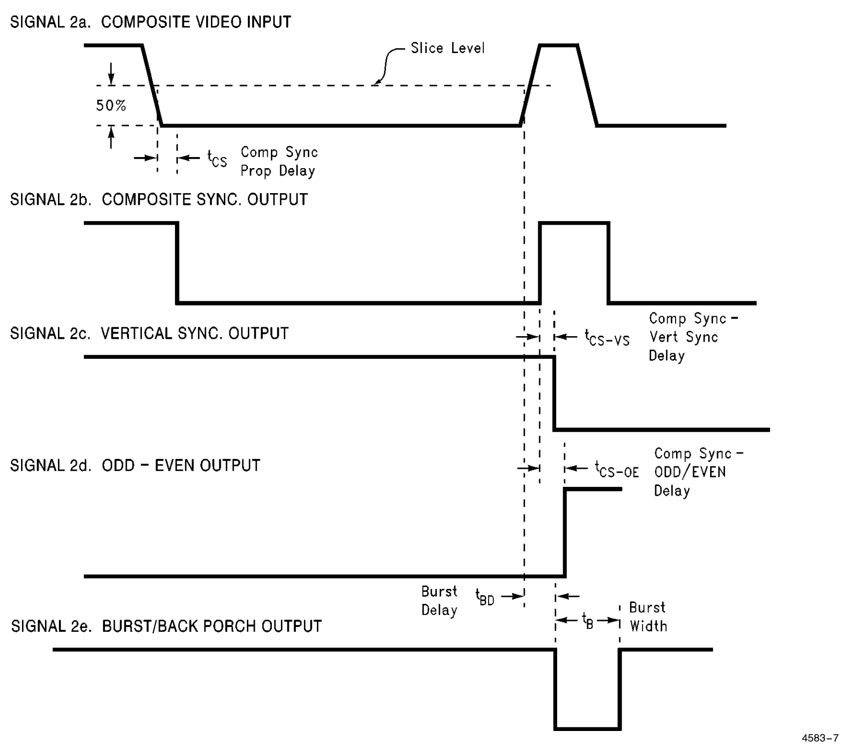


Figure 2

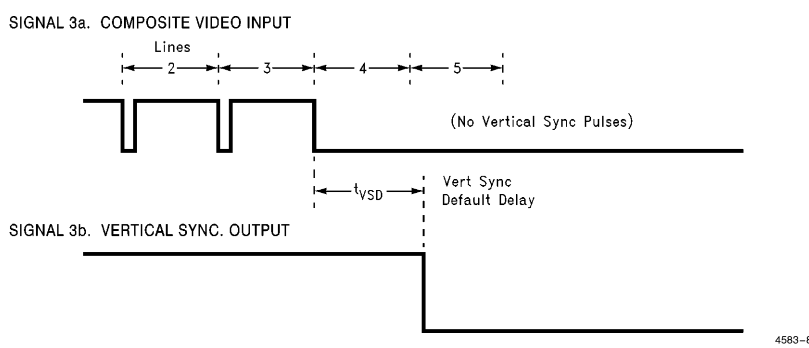


Figure 3

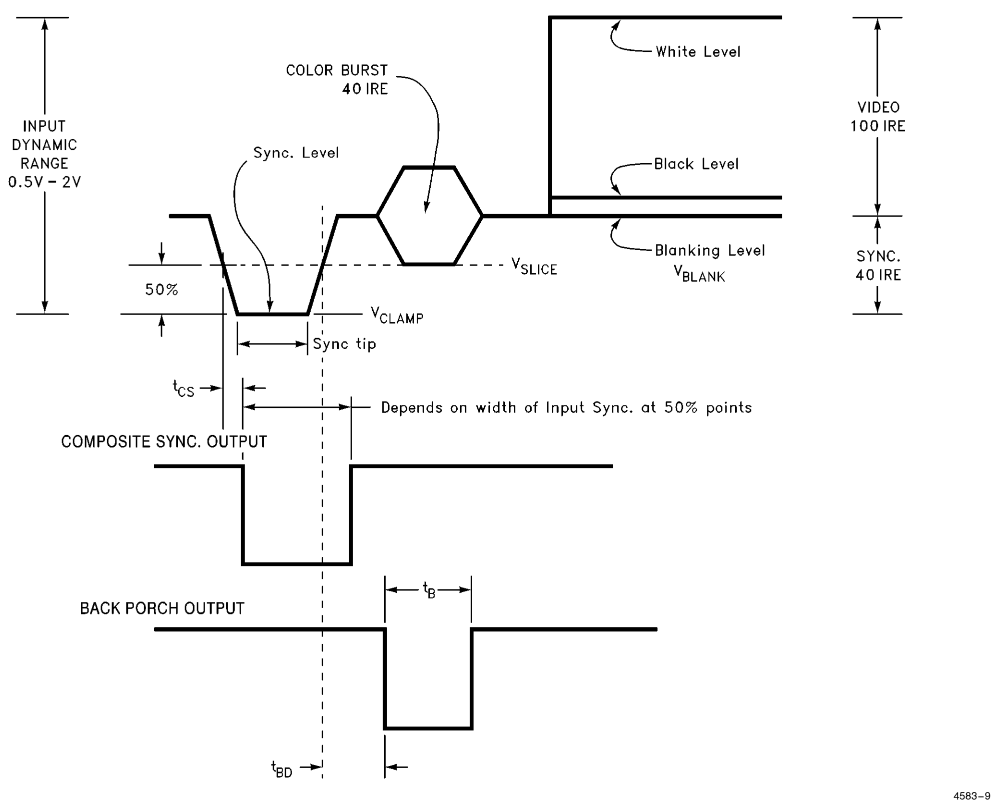


Figure 4. Standard (NTSC Input) H. Sync Detail

Description of Operation

A simplified block schematic is shown in Figure 1. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC compuled to pin 4 via the capacitor C_1, nominally 0.1 μF. The clamp circcuit A1 will prevent the input signal on pin 4 going any more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 10 μA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 μs for a 15.75 kHz timebase. From I • t = C • V, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_I will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. The filter cut-off frequency is controlled by an external resistor from pin 1 to ground.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op-amp A2 forces pin 12 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance RSET will determine the value of the reference current I_{TR}. The internal resistance R3 is only about 6 kΩ, much less than RSET. All the internal timing functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

To improve noise immunity, the output of the 3 pole filter is brought out to pin 7. It is recommended to AC couple the output to pin 8, the video input pin. In case of strong clean video signal, the video input pin, pin 8, can be driven by the signal directly.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync. pulse with a threshold voltage V_{R2} which is referenced at a fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 μs to enable the actual sample of 2 μs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through I_{OT}.

The 50% level of the sync tip is derived, through the resistor divided R1 and R2, from the sample and held voltages V_{TIP} and V_{BP}, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S output buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.

Description of Operation — Contd.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer vertical sync. pulse widths. The internal timing circuits are referenced to I_{OT} and V_{R3}, the timout period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absence of a serration pulse, an internal timer will default the start of vertical.

The Horizontal circuit senses the C/S edges and produces the true horizontal pulses of nominal width 5 µs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2 H eliminator circuit. The 2 H eliminator circuit initiates a time out period after a horizontal pulse if generated. The time out period is a function of I_{OT} which is set by RSET.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by RESET.

The odd/even circuit circuit (O/E) is comprised of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 13 is high during the odd field.

Loss of video signal can be detected by monitoring the No Signal Detect Output pin 10. The VTIP voltage held by the sample and hold is compared with a voltage level set by RLV on pin 2. Pin 10 output goes high when the VTIP falls below RLV set value.

VTIP voltage is also passed through an amplifier with gain of 2 and buffed to pin 9. This is done to provide an indication of signal strength. The Level Output signal can be used for AGC applications.

Block Diagram

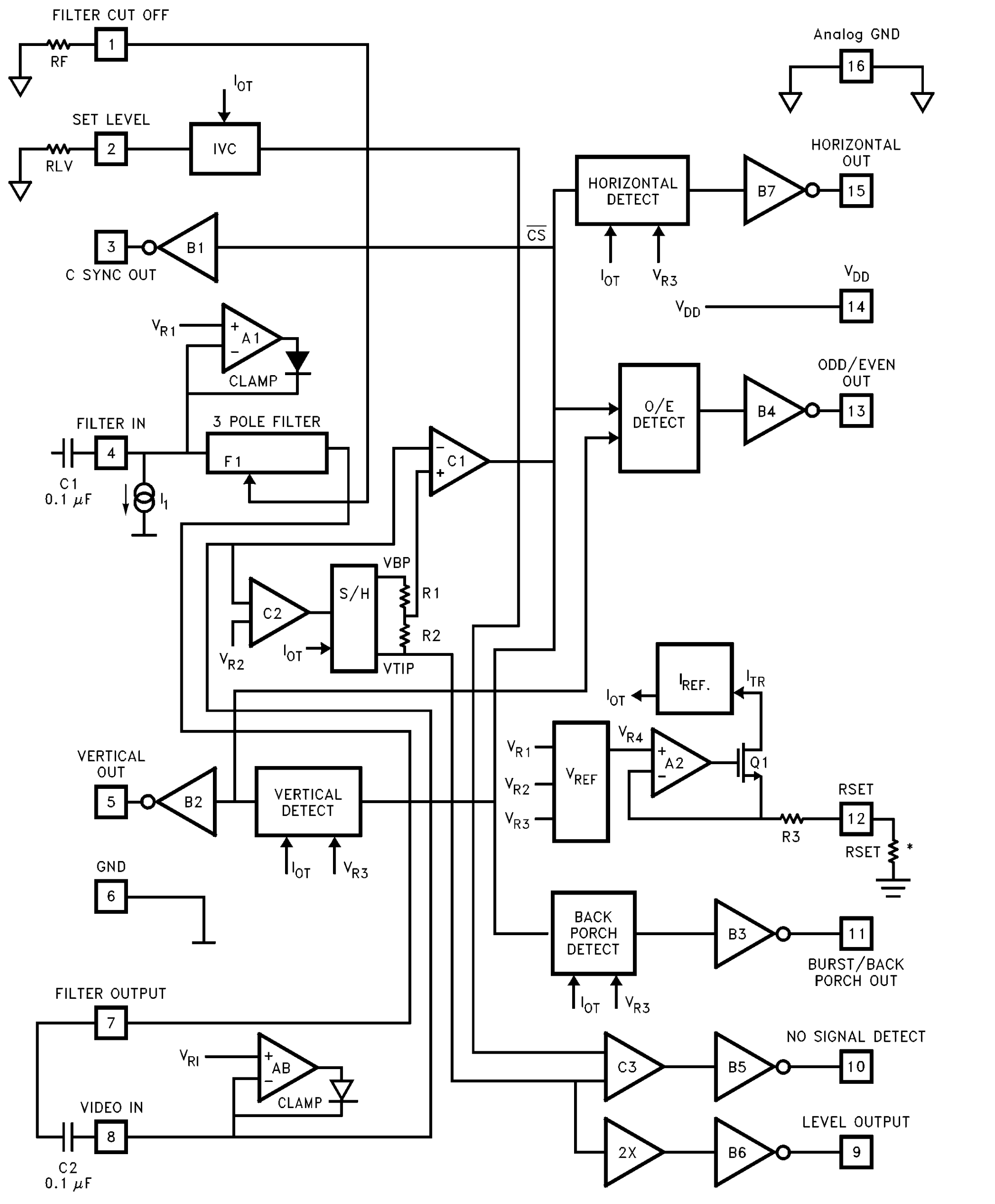


Figure 5

* Note: RSET must be a 1% resistor

EL4583C

Sync Separator, 50% Slice, S-H, Filter, H_{OUT}

General Disclaimer

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec, Inc.
1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
(800) 333-6314
Fax: (408) 945-9305
European Office: 44-71-482-4596

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