WT12

Data Sheet

Version 1.6

Tuesday, January 24, 2006

blue giga
TECHNOLOGIES

Contents:

List of Tables:

List of Figures:

VERSION HISTORY

Version:	Date:	Author:	Comments:
0.1	11.5.2005	*MS*	*Preliminary version*
0.2	15.5.2005	*TR*	*Reviewed*
0.3	31.5.2005	*TL*	*Reviewed*
0.5	2.6.2005	*MS*	*Added PCM documentation*
0.7	3.6.2005	*MS*	*Preliminary phase*
0.9	6.6.2005	*MS*	*Public preliminary version*
1.0	8.6.2005	*MS*	*Review round corrections*
1.1	13.6.2005	*MS*	*Preliminary power consumption added, PIN description corrected*
1.2	12.8.2005	*MS*	*Images added*
1.3	24.1.2006	*MS*	*Pins updated*
1.4	23.9.2005	*MS*	*Minor updates*
1.5	14.12.2005	*MS*	*Dimensions updated*
1.6	24.1.2006	*MS*	*Minor fixes*

TERMS & ABBREVIATIONS

Term or Abbreviation:	Explanation:
Bluetooth	Set of technologies providing audio and data transfer over short-range radio connections
CE	Conformité Européene
EDR	Enhanced Data Rate
FCC	Federal Communications Commission
HCI	Host Controller Interface
HID	Human Interface Device
iWRAP	Interface for WRAP
PCB	Printed Circuit Board
RoHS	The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Transmitter Receiver
USB	Universal Serial Bus
VM	Virtual Machine
WRAP	Wireless Remote Access Platform

1. DEVICE FEATURES OVERVIEW

- Fully Qualified Bluetooth system v2.0 + EDR, CE and FCC
- Integrated chip antenna
- Industrial temperature range from -40^{o}C to +85^{o}C
- Enhanced Data Rate (EDR) compliant with v2.0.E.2 of specification for both 2Mbps and 3Mbps modulation modes
- RoHS Compliant
- Full Speed Bluetooth Operation with Full Piconet
- Scatternet Support
- USB version 2.0 compatible
- UART with bypass mode
- Support for 802.11 Coexistence
- 8Mbits Flash Memory

2. GENERAL DESCRIPTION

2.1 Physical Outlook

Figure 1: Physical outlook of WT12

2.2 Block Diagram and Descriptions

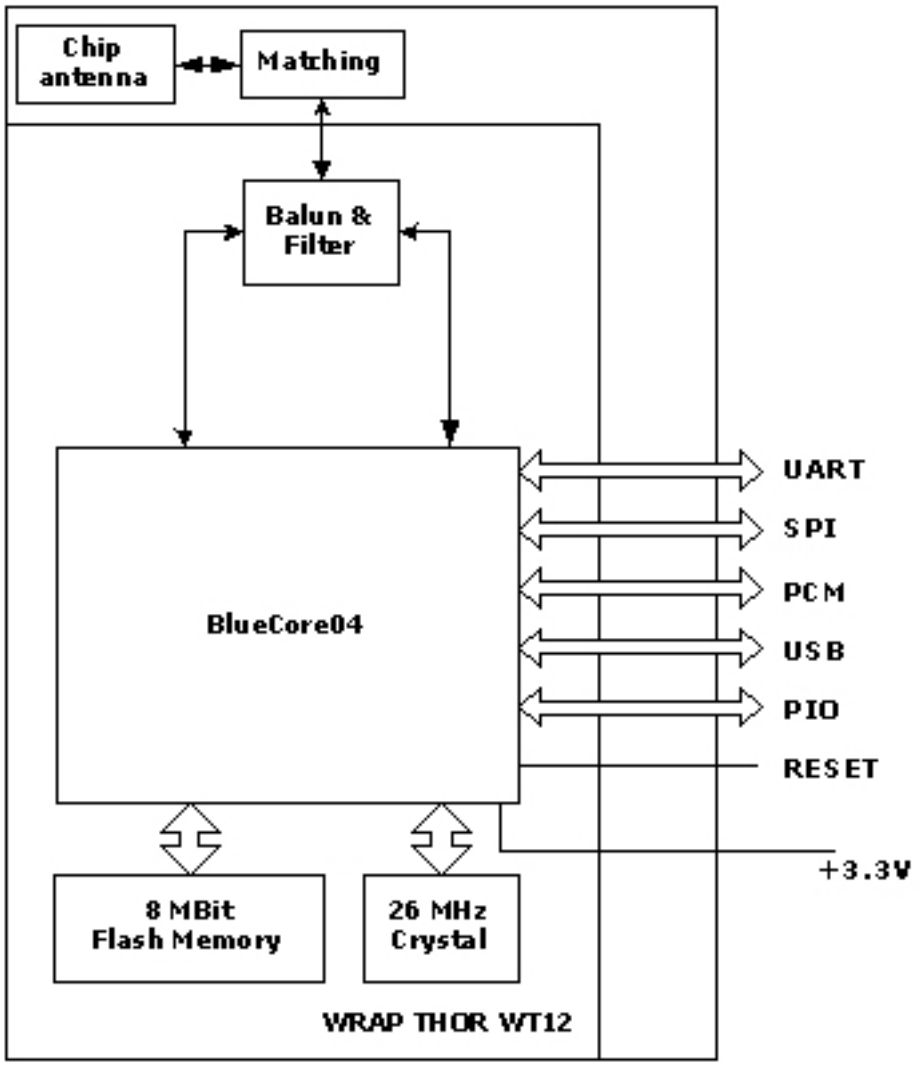

Figure 2: Block Diagram of WT12

2.2.1 BlueCore04

BlueCore4 is a single chip Bluetooth solution which implements the Bluetooth radio transceiver and also an on chip microcontroller. BlueCore4 implements Bluetooth® 2.0+EDR (Enhanced Data Rate) and it can deliver data rates up to 3 Mbps.

The microcontroller (MCU) on BlueCore04 acts as interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

BlueCore04 has 48Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

2.2.2 Crystal

The crystal oscillates at 26MHz.

2.2.3 Flash

Flash memory is used for storing the Bluetooth protocol stack and Virtual Machine applications. It can also to the optional external RAM for memory intensive applications.

2.2.4 Balun/Filter

Combined balun and filter changes the balanced input/output signal of the module to unbalanced signal of the monopole antenna. The filter is a band pass filter (ISM band).

2.2.5 Matching

Antenna matching components match the antenna to 50 Ohms.

2.2.6 Antenna

The antenna is ACX AT3216 chip antenna.

2.2.7 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. WT12 acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

2.2.8 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

2.2.9 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

2.2.10 Audio PCM Interface

The audio pulse code modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

2.2.11 Programmable I/O

WT12 has a total of 6 digital programmable I/O terminals. These are controlled by firmware running on the device.

2.2.12 Reset

This can be used to reset WT12.

2.2.13 802.11 Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH (Adaptive Frequency Hopping), priority signaling, channel signaling and host passing of channel instructions are all supported. The features are configured in firmware.

Since the details of some methods are proprietary (e.g. Intel WCS) please contact Bluegiga for details.

2.3 Applications

WT12 Bluetooth module is designed for:

- Hand held terminals
- Industrial devices
- Point-of-Sale systems
- PCs
- Personal Digital Assistants (PDAs)
- Computer Accessories
- Access Points
- Automotive Diagnostics Units

2.4 Product names and codes

iWRAP firmware:

- WT12 with internal chip antenna, iWRAP firmware: WT12-A-AI
- WT12 without antenna, iWRAP firmware: WT12-N-AI

HCI firmware:

- WT12 with internal chip antenna, HCI firmware: WT12-A-HCI
- WT12 without antenna, HCI firmware: WT12-N-HCI

Notes:

HCI firmware is delivered with USB as host interface!

Custom firmware:

- WT12 with internal chip antenna, custom firmware: WT12-A-C
- WT12 without antenna, custom firmware: WT12-N-C

Notes:

Custom firmware requires properly filled custom firmware document or custom firmware ID.

3. PHYSICAL LAYER SPECIFICATIONS

The common physical layer specifications are shown in the table below.

Item	Specification
Operating Frequency	2400 MHz to 2483.5 MHz (ISM-Band)
Carrier Spacing	1.0 MHz
Channels	79
Duplexing	TDD
Symbol Rate	1 Msymbol/s
TX Modulation Polarity	Binary one: Positive frequency deviation
	Binary zero: Negative frequency deviation
RX Data Out Polarity	F_C + dF: "H"
	F_C - dF: "L"

Table 1: Common physical layer specifications

4. GENERAL SPECIFICATIONS

Item	Specification
Supply voltage	3.3 V ± 0.1 V regulated voltage. (Noise < 10 mV_{P-P})
Supply current	Maximum current in TX mode: 70.0mA Maximum current in RX mode: 70.0mA
Frequency range	2400 MHz … 2483.5 MHz (ISM-Band)
Guard band	2 MHz < F < 3.5 MHz (Europe, Japan, USA)
Carrier frequency	2402 MHz … 2480 MHz, F = 2402 + k MHz, k = 0 … 78
Modulation method	GFSK (1 Mbps), Π/4 DQPSK (2Mbps) and 8DQPSK (3Mbps)
Hopping	1600 hops/s, 1 MHz channel space
Maximum data rate	**GFSK:** Asynchronous, 723.2 kbps / 57.6 kbps Synchronous: 433.9 kbps / 433.9 kbps **Π/4 DQPSK:** Asynchronous, 1448.5 kbps / 115.2 kbps Synchronous: 869.7 kbps / 869.7 kbps **8DQPSK:** Asynchronous, 2178.1 kbps / 177.2 kbps Synchronous: 1306.9 kbps / 1306.9 kbps
Receiving signal range	-82 to -20 dBm (Typical)
Receiver IF frequency	1.5 MHz (Center frequency)

Transmission power	Minimum: -11 …-9 dBm Maximum +1 … +3 dBm
RF input impedance	50 Ω
Baseband crystal OSC	26 MHz
Output interfaces	6 GPIO, PCM, SPI, UART, USB
Operation temperature	-40ºC … +85ºC
Storage temperature	-40ºC … +105ºC
Compliance	Bluetooth specification, version 2.0 + EDR
USB specification	USB specification, version 1.2

Table 2: General specifications

5. ELECTRICAL CHARASTERISTICS

Rating	Min	Max
Storage temperature	-40°C	+150°C
Supply Voltage: VDD	3.2V	3.4V

Table 3: Absolute Maximum Ratings

Operating conditions	Min	Max
Operating Temperature Range:	-40°C	+85°C
Supply Voltage: VDD	3.2V	3.4V

Table 4: Recommended Operating Conditions

Digital terminals	Min	Typ	Max	Unit
Input voltage				
V_{IL} input logic level low (VDD=3.3V)	-0.4		+0.8	V
V_{IH} input logic level high	0.7VDD		VDD+0.1	V
Output voltage				
V_{OL} output logic level low (VDD=3.3V) (I_o = 3.0mA)			0.2	V
V_{OL} output logic level high (VDD=3.3V) (I_o = -3.0mA)	VDD-0.2			V

Table 5: Input/Output Terminal Characteristics

6. CURRENT CONSUMPTION

See *WT12 Current Consumption* document for details. The document can be found from www.bluegiga.com/techforum/.

7. WT12 PIN DESCRIPTION

The PIN description of WT12 is shown in the table below.

No.	Pin name	I/O	Description
1	GND	GND	Ground
2	3V3	VDD	Power supply connection
3	PIO2	I/O	Programmable I/O lines
4	PIO3	I/O	Programmable I/O lines
5	NRTS	O	UART RTS (internal pull-up, active low)
6	RXD	I	UART RX (internal pull down)
7	PCMO	O	Synchronous 8 kbps data out (internal Pull down)
8	USB_D+	A	USB data plus (Internal 22 ohm serial resistor)
9	USB_D-	A	USB data minus (Internal 22 ohm serial resistor)
10	NCTS	I	UART CTS (internal pull down, active low)
11	PCMI	I	Synchronous 8 kbps data in (internal pull-down)
12	PCMC	I/O	Synchronous data clock (internal pull-down)
13	PCMS	I/O	Synchronous data strobe (internal pull-down)
14	GND	GND	Ground
15	GND	GND	Ground
16	3V3	VDD	Power supply connection
17	RES	I	Reset input (active high)

18	PIO6	I/O	Programmable I/O lines
19	PIO7	I/O	Programmable I/O lines
20	PIO4	I/O	Programmable I/O lines
21	NCSB	I	Chip selection for SPI (internal pull up, active low)
22	SCLK	I/O	SPI Clock (internal pull down)
23	MISO	O	SPI data output (pull down)
24	MOSI	I	SPI data input (pull down)
25	PIO5	I/O	Programmable I/O lines
26	TXD	O	UART TX (internal pull up)
27	NC	-	NC, not used in WT12 module.
28	GND	GND	Ground
29	GND	GND	Ground
30	RF	RF	RF-transceiver antenna (when chip antenna not in use!)
31	GND	GND	Ground

Table 6: WT12 PIN configuration

Notes: Voltage level of input (I), output (O) and input/output (I/O) pins is 3.3V.

Pin 30 is used only with WT12-N i.e. WT12 is used with external antenna.

8. FOOT PRINT

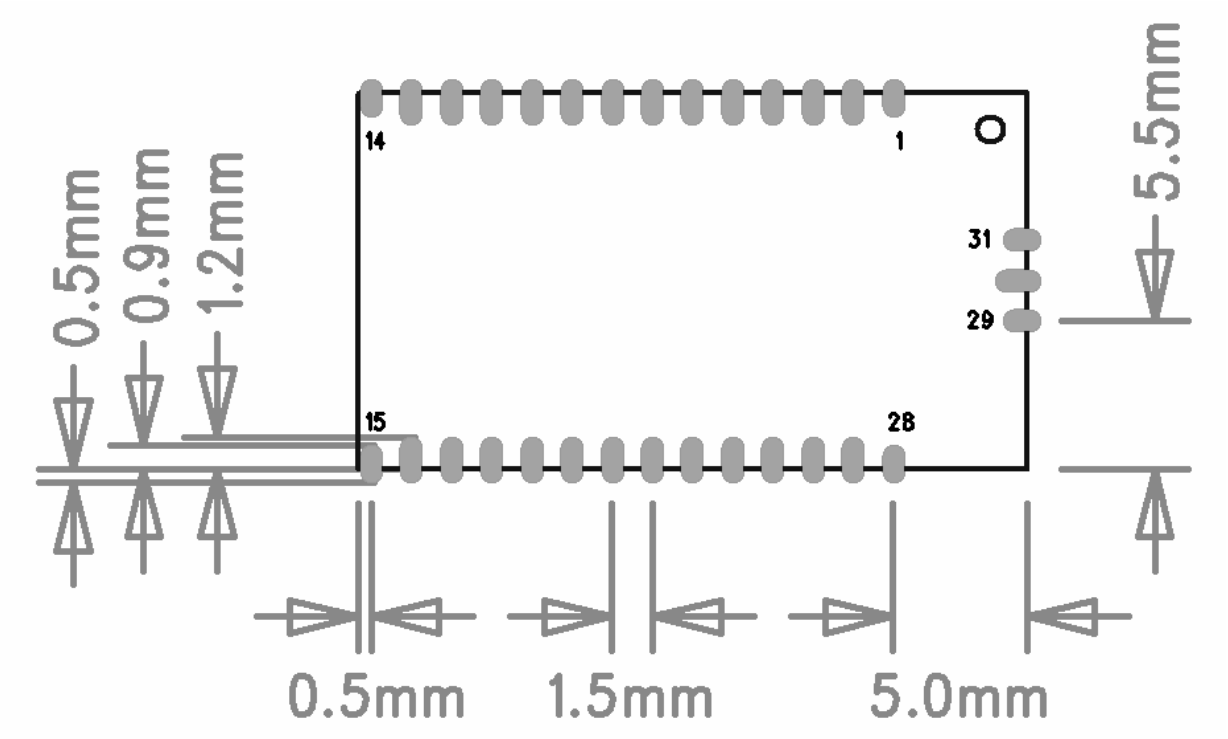

Figure 3: WT12 foot print and dimension

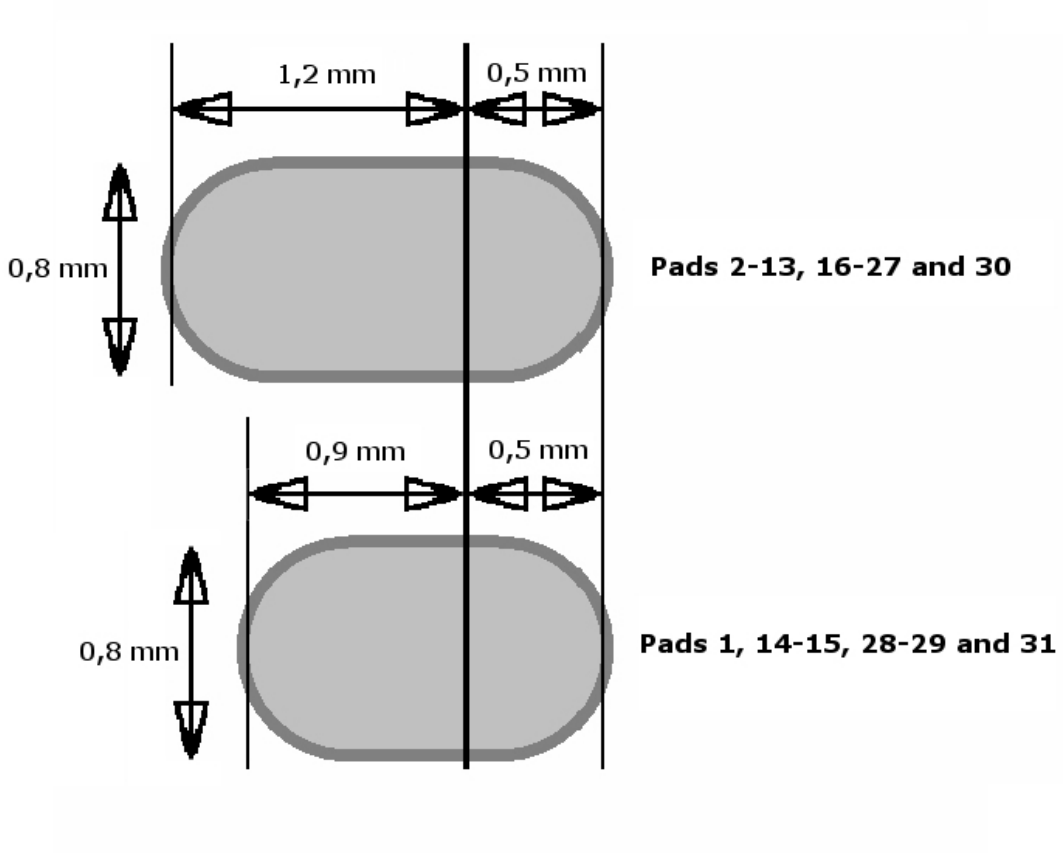

Figure 4: WT12 pad dimensions

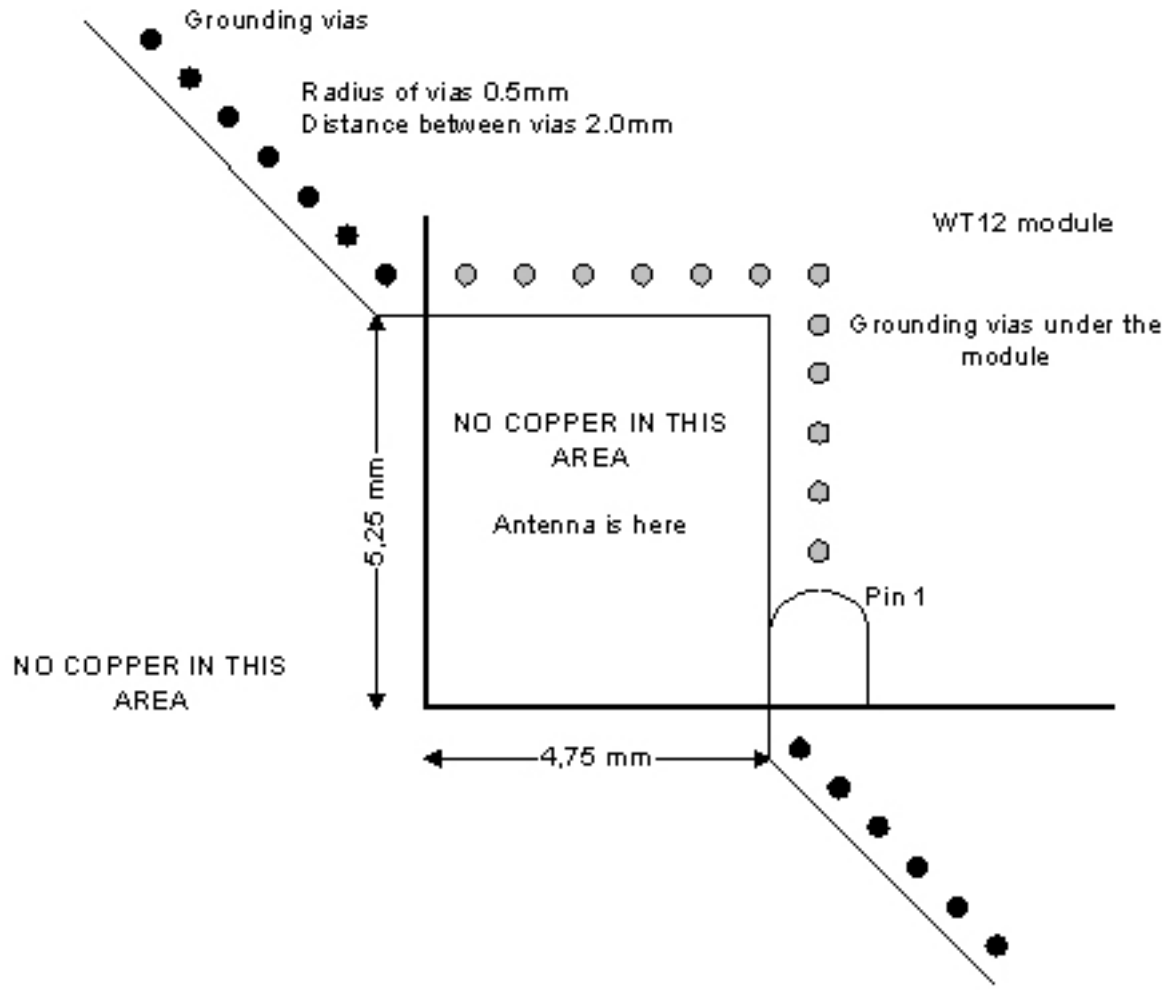

Figure 5: PCB design around ACX antenna

Figure four above illustrates how PCB design around the antenna of WT12 should be made. The most important thing is that there is no copper (ground plane or traces) underneath or in the close proximity of the ACX antenna.

It's also very important to have grounding vias all the way in the border between ground plane and free space, as illustrated with black and gray dots in figure 4. This prevents the RF signal for reflecting back to the PCB and signal lines over there.

For more information, please refer to the WT12 design guide and design references.

9. PHYSICAL DIMENSIONS

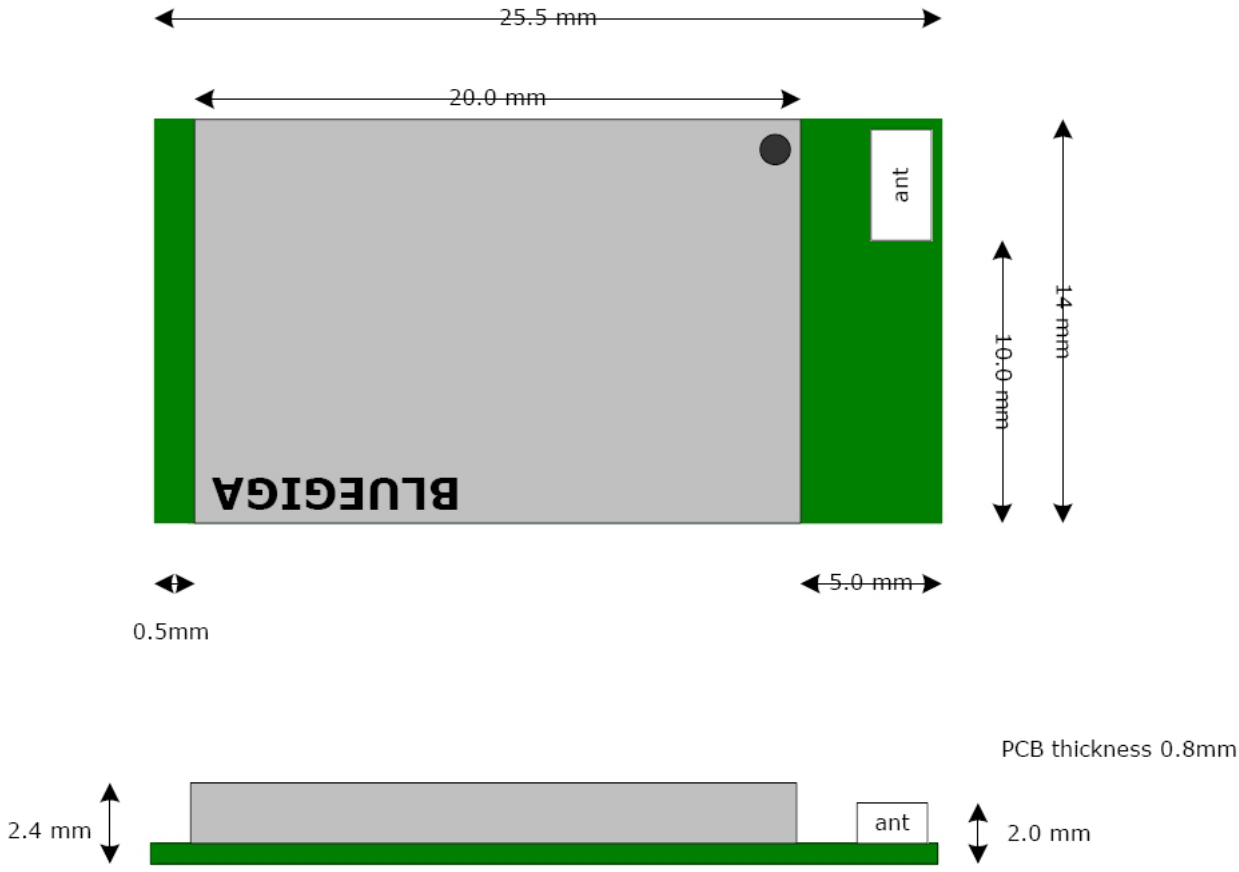

Figure 6: WT12 Dimensions

10. RADIO CHARASTERISTICS

WT12 meets the Bluetooth v2.0+EDR specification between -40°C and +85°C.

TX output is guaranteed to be unconditionally stable over the guaranteed temperature range.

VDD = 3.3V

10.1 Temperature 20°C

10.1.1 Transmitter

Item	Min	Typ	Max	Unit	Bluetooth specification
Maximum output power[1,2]	-	+2.5	-	dBm	-6 to 4[3]
Variation in RF power over temperature range with compensation enabled[4]	-	1.5	-	dB	-
Variation in RF power over temperature range with compensation disabled[4]	-	2.0	-	dB	-
RF power control range	-	35	-	dB	t16
RF power range control resolution[5]	-	0.5	-	dB	-
20dB bandwidth for modulated carrier	-	780	-	kHz	d1000
Adjacent channel transmit power F=F r2MHz(6)(7)	-	-40	-	dBm	d-20
Adjacent channel transmit power F=F r3MHz(6)(7)	-	-45	-	dBm	d-40
Adjacent channel transmit power F=F !r3MHz(6)(7)	-	-50	-	dBm	d-40
'f1avg "Maximum Modulation"	-	165	-	kHz	140<f1avg<175

‘f2max “Minimum Modulation”	-	150	-	kHz	t115
’ f2avg / ’ f1avg	-	0.97	-	-	t0.8
Initial carrier frequency tolerance	-	6	-	kHz	r75
Drift Rate	-	8	-	kHz/50 Ps	d20
Drift (single slot packet)	-	7	-	kHz	d25
Drift (five slot packet)	-	9	-	kHz	d40
2nd Harmonic content	-	-65	-	dBm	d-30
3rd Harmonic content	-	-45	-	dBm	d-30

Table 7: Transmitter characteristics +20°C

Notes:

1 WT12 firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits.

2 Measurement made using a PSKEY_LC_MAX_TX_POWER setting corresponds to a PSKEY_LC_POWER_TABLE power table entry of 63.

3 Class 2 RF-transmit power range, Bluetooth v2.0+EDR specification.

4 To some extent these parameters are dependent on the matching circuit used, and its behavior over temperature. Therefore these parameters may be beyond CSR’s direct control.

5 Resolution guaranteed over the range -5dB to -25dB relative to maximum power for TX Level >20.

6 Measured at F0= 2441MHz.

7 Up to three exceptions are allowed in the Bluetooth v2.0+EDR specification. WT12s guaranteed to meet the ACP performance as specified by the Bluetooth v2.0+EDR specification.

	Frequency (GHz)	Min	Typ	Max	Unit	Cellular band
Emitted power in cellular bands measured at the unbalanced port of the balun. Output power 4dBm	0.869 – 0.894[1]	-	-145	-	dBm/kHz	GSM 850
	0.869 – 0.894[2]	-	-145	-		CDMA 850
	0.925 – 0.960[1]	-	-145	-		GSM 900
	1.570 – 1.580[3]	-	-145	-		GPS
	1.805 – 1.880[1]	-	-145	-		GSM 1800 / DCS 1800
	1.930 – 1.990[4]	-	-145	-		PSC 1900
	1.930 – 1.990[1]	-	-145	-		GSM 1900
	1.930 – 1.990[2]	-	-145	-		CDMA 1900
	2.110 – 2.170[2]	-	-142	-		W-CDMA 2000
	2.110 – 2.170[2]	-	-144	-		W-CDMA 2000

Table 8: Transmitter characteristics +20°C continued

Notes:

1 Integrated in 200kHz bandwidth and then normalized to a 1Hz bandwidth.

2 Integrated in 1.2MHz bandwidth and then normalized to a 1Hz bandwidth.

3 Integrated in 1MHz bandwidth. and then normalized to a 1Hz bandwidth.

4 Integrated in 30kHz bandwidth and then normalized to a 1Hz bandwidth.

5 Integrated in 5MHz bandwidth and then normalized to a 1Hz bandwidth.

10.1.2 Receiver

Item	Frequency (GHz)	Min	Typ	Max	Unit	Bluetooth specification
Sensitivity at 0.1% BER for all packet types	2.402	-	-84	-	dBm	d-70
	2.441	-	-84	-		
	2.480	-	-84	-		
Maximum received signal at 0.1% BER		-	10	-	dBm	d-20

Table 9: Receiver characteristics +20°C

Item	Frequency (GHz)	Min	Typ	Max	Unit	Bluetooth specification
Continuous power required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30-2000	-	TBD	-	dBm	d-10
	2000-2400	-	TBD	-		d-27
	2500-3000	-	TBD	-		d-27
	3000-3300	-	TBD	-		d-10
C/I co-channel		-	6	-	dB	d11
Adjacent channel selectivity C/I F=F 1MHz[1,2]		-	-5	-	dB	d0
Adjacent channel selectivity C/I F=F 1MHz[1,2]		-	-4	-	dB	d0
Adjacent channel selectivity C/I F=F2 MHz[1,2]		-	-38	-	dB	d-30
Adjacent channel selectivity C/I F=F2 MHz[1,2]		-	-23	-	dB	d-20

Adjacent channel selectivity C/I FtF +3MHz[1,2]	-	-45	-	dB	d-40
Adjacent channel selectivity C/I FdF5MHz[1,2]	-	-44	-	dB	d-40
Adjacent channel selectivity C/I F=FImage[1,2]	-	-22	-	dB	d-9
Maximum level of intermodulation interferers[3]	-	-30	-	dBm	t-39
Spurious output level[4]	-	TBD	-	dBm/ Hz	-

Table 10: Receiver characteristics +20°C continued

Notes:

1 Up to five exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4 is guaranteed to meet the C/I performance as specified by the Bluetooth v2.0 + EDR specification.

2 Measured at F = 2441MHz

3 Measured at f1-f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c. i.e. wanted signal at -64dBm

4 Measured at the unbalanced port of the balun. Integrated in 100kHz bandwidth and then normalized to 1Hz. Actual figure is typically below TBD dBm/Hz except for peaks of -52dBm in band at 2.4GHz and d80dBm at 3.2GHz

	Frequency (GHz)	Min	Typ	Max	Unit	Cellular band
Emitted power in cellular bands required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	2.0	-	dBm	GSM 850
	0.824 – 0.849	-	TBD	-		CDMA
	0.880 – 0.915	-	5.0	-		GSM 900
	1.710 – 1.785	-	4.0	-		GSM 1800 / DCS 1800

	1.710 – 1.785	-	3.0	-		GSM 1900 / PCS 1900
	1.850 – 1.910	-	TBD	-		CDMA 1900
	1.920 – 1.980	-	TBD	-		W-CDMA 2000
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of-72dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	-10.0	-	dBm	GSM 850
	0.824 – 0.849	-	TDB	-		CDMA
	0.880 – 0.915	-	-10.0	-		GSM 900
	1.710 – 1.785	-	-9.0	-		GSM 1800 / DCS 1800
	1.850 – 1.910	-	-9.0	-		GSM 1900 / PCS 1900
	1.850 – 1.910	-	TDB	-		CDMA 1900
	1.920 – 1.980	-	TDB	-		W-CDMA 2000

Table 11: Receiver characteristics +20^{o}C continued

11. RADIO CHARACTERISTICS - ENHANCED DATA RATE

11.1 Temperature 20°C

11.1.1 Transmitter

Item		Min	Typ	Max	Unit	Bluetooth specification
Maximum output power[1]		-	+1	-	dBm	-6 to 4[2]
Relative transmit power[3]		-	-1	-	dB	-
Carrier frequency stability[3]		-	3	-	kHz	d10
Modulation accuracy[3,4]	RMS DEV	-	-	-	%	d13[5]
	99% DEV	-	-	-	%	d20[5]
	Peak DEVM	-	-	-	%	d25[5]

Table 12: Transmitter characteristics +20°C EDR

Notes:

Results shown are referenced to input of the RF balun.

1. WT12 firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits
2. Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification
3. Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2
4. Modulation accuracy utilizes differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
5. The Bluetooth specification values are for 8DPSK modulation (values for the S/4 DQPSK modulation are less stringent)

11.1.2 Receiver

Item	Modulation	Min	Typ	Max	Unit	Bluetooth specification
Sensitivity at 0.1% BER for all packet	Π/4 DQPSK	-	-87	-	dBm	d-70

	8DQPSK	-	-79	-		d-70
Maximum received signal at 0.1% BER[1]	Π/4 DQPSK	-	-7	-		t-20
	8DQPSK	-	-7	-		t-20
C/I co-channel at 0.1% BER[1]	Π/4 DQPSK	-	+11	-		d+13
	8DQPSK	-	+19	-		d+21
Adjacent channel selectivity C/I F=F0 +1MHz[1,2,3]	Π/4 DQPSK	-	-8	-		d0
	8DQPSK	-	-2	-		d+5
Adjacent channel selectivity C/I F=F0 -1MHz[1,2,3]	Π/4 DQPSK	-	-8	-	dB	d0
	8DQPSK	-	-2	-		d+5
Adjacent channel selectivity C/I F=F0 - +2MHz[1,2,3]	Π/4 DQPSK	-	-35	-		d-30
	8DQPSK	-	-35	-		d-25
Adjacent channel selectivity C/I F=F0 -2MHz[1,2,3]	Π/4 DQPSK	-	-23	-		d-20
	8DQPSK	-	-19	-		d-13
Adjacent channel selectivity C/I F*F0 +3MHz[1,2,3]	Π/4 DQPSK	-	-43	-		d-40
	8DQPSK	-	-40	-		d-33
Adjacent channel selectivity C/I F*F0 -5MHz[1,2,3]	Π/4 DQPSK	-	-43	-	dB	d-40
	8DQPSK	-	-38	-		d-33
Adjacent channel selectivity C/I F=FImage[1,2,3]	Π/4 DQPSK	-	-17	-		d-7
	8DQPSK	-	-11	-		d0

Table 13: Receiver characteristics +20°C EDR

Notes:

Results shown are referenced to input of the RF balun

1. Measurements methods are in accordance with the EDR RF Test Specification v2.0.E.2

2. Up to five exceptions are allowed in EDR RF Test Specification v2.0.E.2. WT12 is guaranteed to meet the C/I performance as specified by the EDR RF Test Specification v2.0.E.2.

3. Measured at F0 = 2405MHz, 2441MHz, 2477MHz

12. PHYSICAL INTERFACES

12.1 UART Interface

WT12 Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard[1].

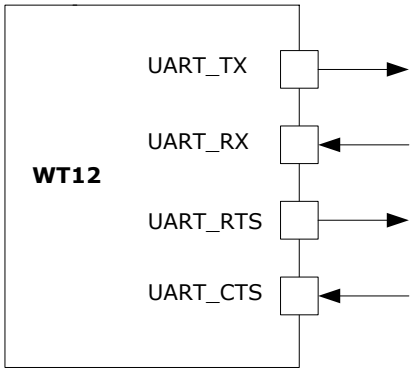

Figure 7: WT12 UART interface

Four signals are used to implement the UART function, as shown in Figure 11.12. When WT12 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signaling levels of 0V and VDD_PADS.

UART configuration parameters, such as Baud rate and packet format, are set using iWRAP software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

1. Uses RS232 protocol but voltage levels are 0V to VDD_USB, (requires external RS232 transceiver chip)

Parameter		Possible values
Baud rate	Minimum	1200 baud (d2%Error)
		9600 baud (d1%Error)
	Maximum	3.0Mbaud (d1%Error)
Flow control		RTS/CTS, none

Parity	None, Odd, Even
Number of stop bits	1 or 2
Bits per channel	8

Figure 8: Possible UART settings

The UART interface is capable of resetting WT12 upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure below If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialize the system to a known state. Also, WT12 can emit a Break character that may be used to wake the Host.

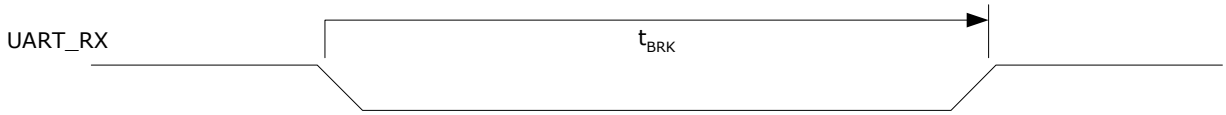

Figure 9: Break signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 15 shows a list of commonly used Baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the Persistent Store Key according to the formula in Equation below.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Figure 10: Baud rate calculation formula

Baud rate	Persistent store value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2765800	0x2c3d	11325	0.00%

Table 14: UART baud rates and error values

12.1.1 UART Configuration While RESET is Active

The UART interface for WT12 while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when WT12reset is de-asserted and the firmware begins to run.

12.1.2 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on WT12 can be used. The default state of WT12 after reset is de-asserted, this is for the host UART bus to be connected to the WT12 UART, thereby allowing communication to WT12 via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to WT12 upon this, it will switch the bypass to PIO[7:4] as shown in Figure 6. Once the bypass mode has been invoked, WT12 will enter the deep sleep state indefinitely.

In order to re-establish communication with WT12, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

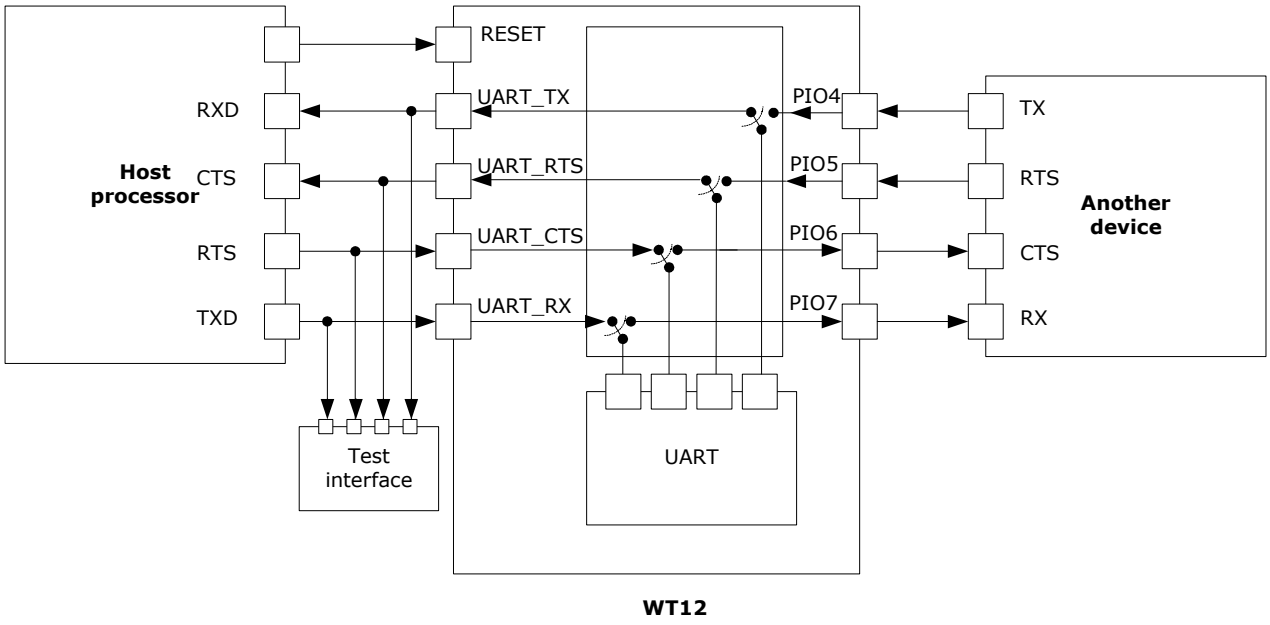

Figure 11: UART bypass mode

12.1.3 Current Consumption in UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

12.2 USB Interface

WT12 USB devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth v2.0 + EDR specification or alternatively can appear as a set of endpoint appropriate to USB audio devices such as speakers.

As USB is a Master/Slave oriented system (in common with other USB peripherals), WT12 only supports USB Slave operation.

12.2.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the WT12 and therefore have low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors are included with USB_DP / USB_DN and the cable.

12.2.2 USB Pull-Up Resistor

WT12 features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when

WT12 is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device. The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15k: r5% pull-down resistor (in the hub/host) when VDD =3.3V. This presents a Therein resistance to the host of at least 900Ohms. Alternatively, an external 1.5k: pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

12.2.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

12.2.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to WT12 via a resistor network (Rvb1 and Rvb2), so WT12 can detect when VBUS is powered up. WT12 will not pull USB_DP high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5K 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in WT12 is only suitable for bus powered USB devices i.e. dongles.

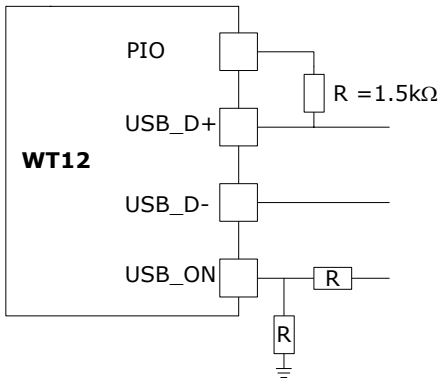

Figure 12: USB in self powered mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

In self powered mode PSKEY_USB_PIO_PULLUP must be set to match with the PIO selected.

Note:

USB_ON is shared with WT12 PIO terminals (PIO2-PIO7).

12.2.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. WT12 negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For WT12 Bluetooth applications, it is recommended that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without fold back or limiting. In bus powered mode, WT12 requests 100mA during enumeration.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10pF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of WT12 will result in reduced receive sensitivity and a distorted RF transmit signal.

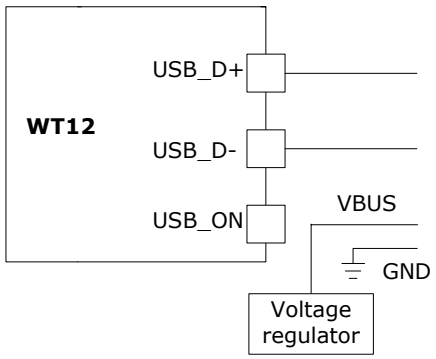

Figure 13: USB in bus powered mode

In bus powered mode PSKEY_USB_PIO_PULLUP must be set to 16 for internal pull-up (default configuration in WT12).

12.2.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB Suspend mode. While in USB Suspend, bus powered devices must not draw more than 0.5mA from USB VBUS (self powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100uA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by WT12. The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see separate CSR documentation).

12.2.7 Detach and Wake-Up Signaling

WT12 can provide out-of-band signaling to a host controller by using the control lines called 'USB_DETACH' and 'USB_WAKE_UP'. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding WT12 into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes WT12 to put USB_DN and USB_DP in high impedance state and turned off the pull-up resistor on D+. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, WT12 will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while WT12 is effectively disconnected from the bus.

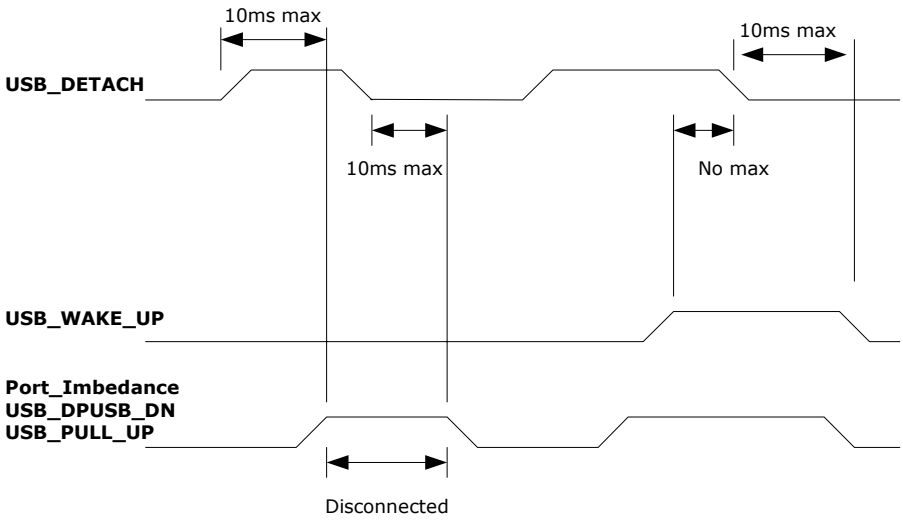

Figure 14: USB_DETACH and USB_WAKE_UP Signal

12.2.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between WT12 and Bluetooth software running on the host computer. Suitable drivers are available from www.bluegiga.com/techforum/.

12.2.9 USB 1.1 Compliance

WT12 is qualified to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labeling.

Although WT12 meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed

USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plug fest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

12.2.10 USB 2.0 Compatibility

WT12 is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

12.3 SPI Interface

The synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory. SPI interface is connected using the MOSI, MISO, CSB and CLK pins.

12.4 PCM Interface

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, BlueCore4-External has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. WT12 offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on WT12 allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time[1].

WT12 can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. WT12 is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

WT12 interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-External is also compatible with the Motorola SSI™ interface

12.4.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, WT12 generates PCM_CLK and PCM_SYNC.

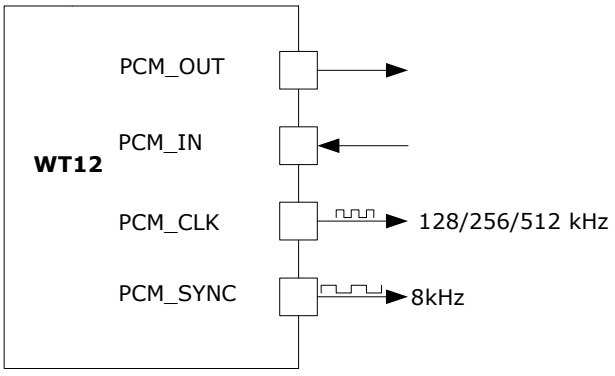

Figure 15: WT12 as PCM master

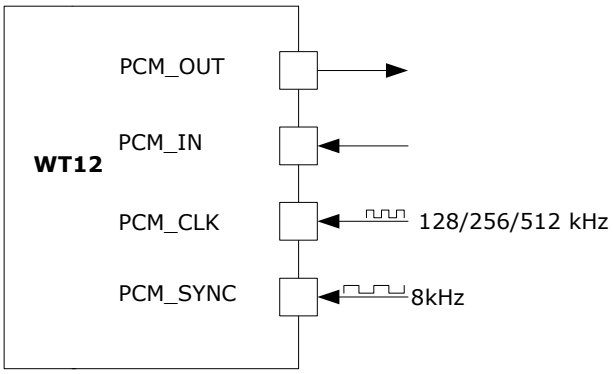

Figure 16: WT12 as PCM slave

12.4.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-External is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-External is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5μs long.

BlueCore4-External samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

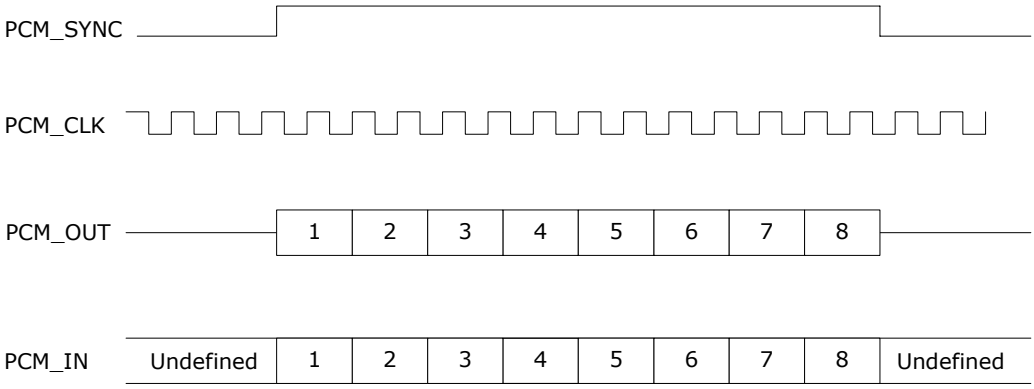

Figure 17: Long frame sync (shown with 8-bit Companded Sample)

12.4.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

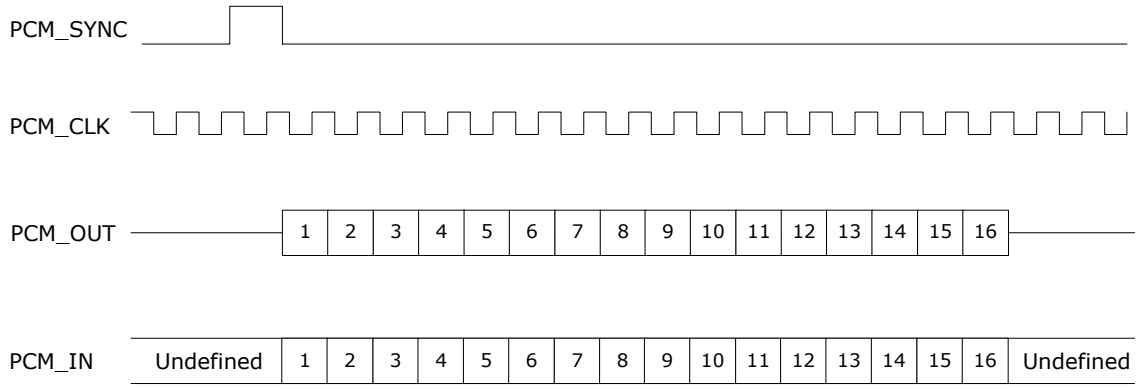

Figure 18: Short frame sync (shown with 16-bit Companded Sample)

As with Long Frame Sync, WT12 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

12.4.4 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

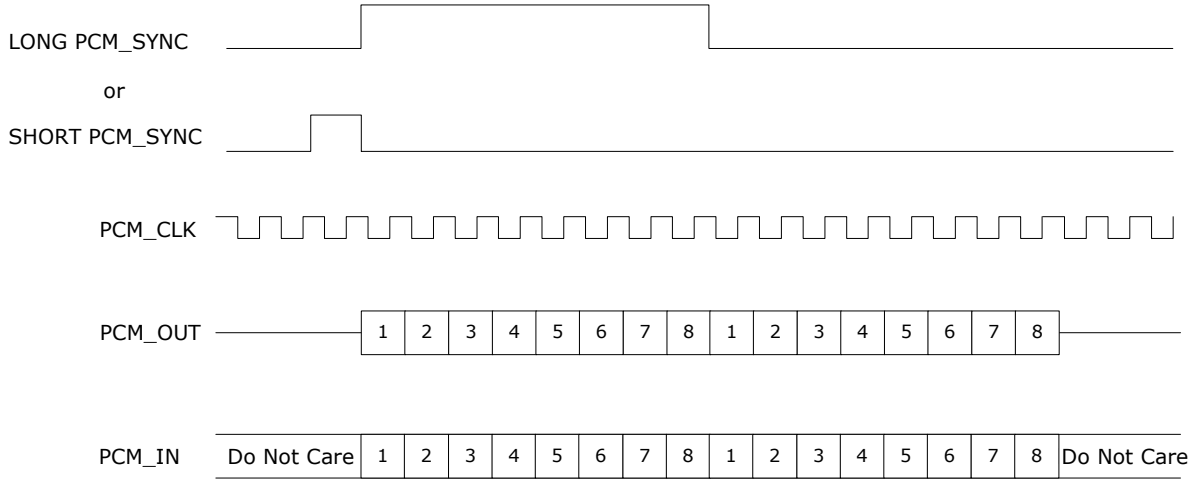

Figure 19: Multi Slot Operation with Two Slots and 8-bit Companded Samples

12.4.5 GCI Interface

WT12 is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

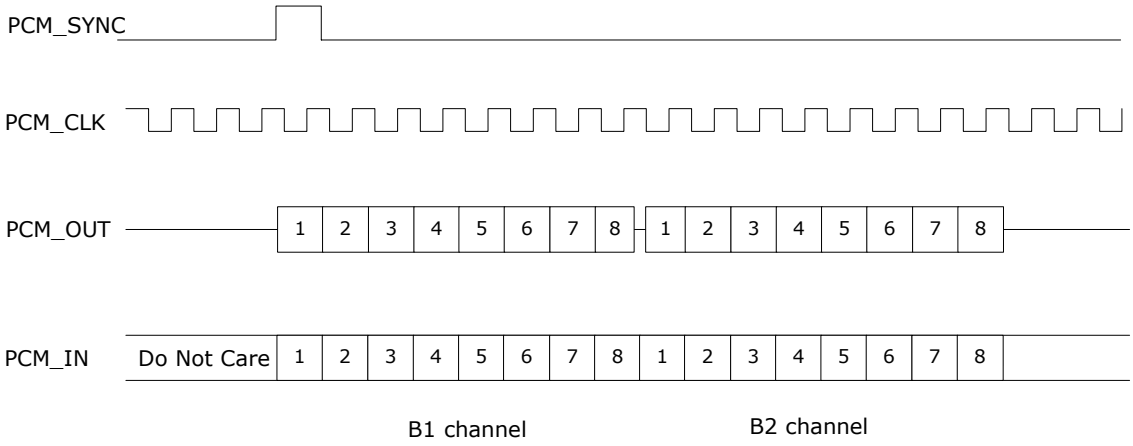

Figure 20: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With WT12 in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

12.4.6 Slots and Sample Formats

WT12 can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Duration's of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

WT12 supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big Endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

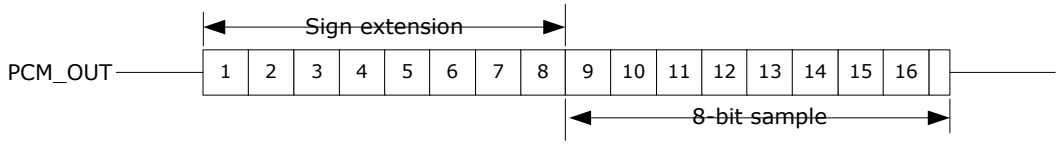

Figure 21: 16-bit slot with 8-bit companded sample and sign extension selected

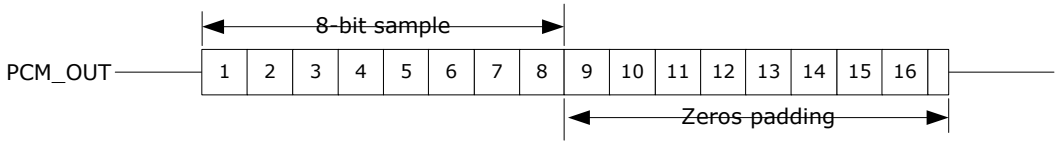

Figure 22: 16-bit slot with 8-bit companded sample and zeros padding selected

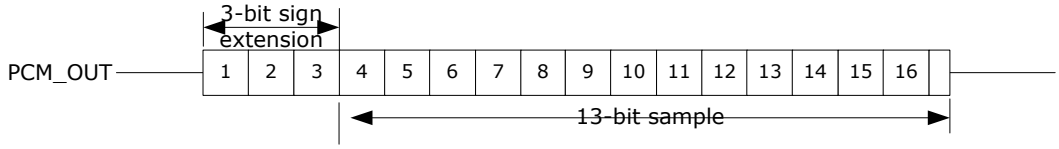

Figure 23: 16-bit slot with 13-bit linear sample and sign extension selected

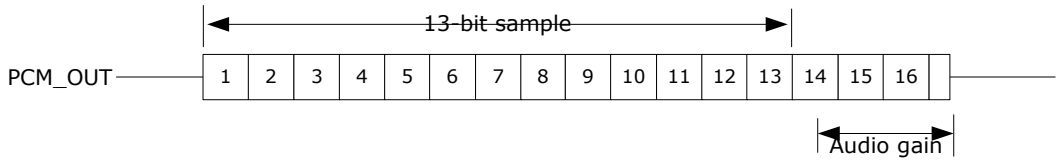

Figure 24: 16-bit slot with 13-bit linear sample and audio gain selected

12.4.7 Additional Features

WT12 has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

12.4.8 PCM timing information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable.	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable.	2.9		-	kHz
.	PCM_SYNC frequency		-	8		kHz
f_{mclkh} (1)	PCM_CLK high, 4MHz DDS generation		980	-	-	ns
f_{mclkl} (1)	PCM_CLK low, 4MHz DDS generation		730	-	-	ns
-	PCM_CLK jitter, 48MHz DDS generation				21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns pk-pk
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long frame sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_SYNC high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_SYNC high impedance		30	-	-	ns
$t_{hpinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		10	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 15: PCM Master timing

1. Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

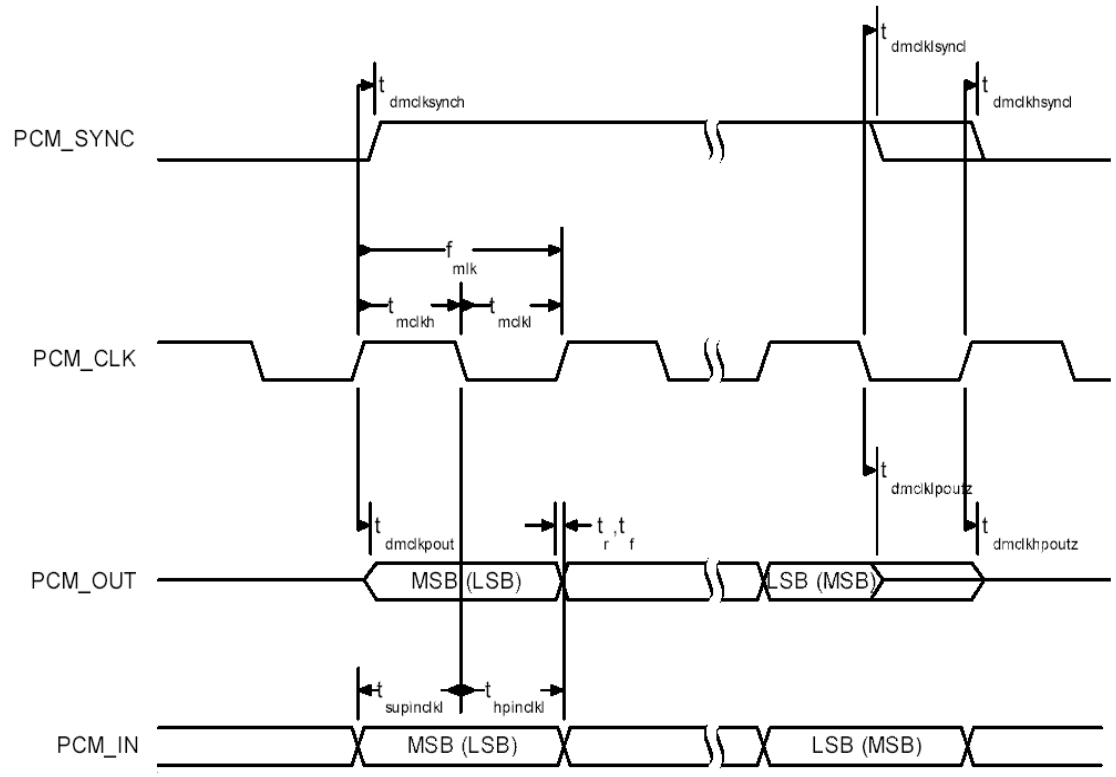

Figure 25: PCM master timing long frame sync

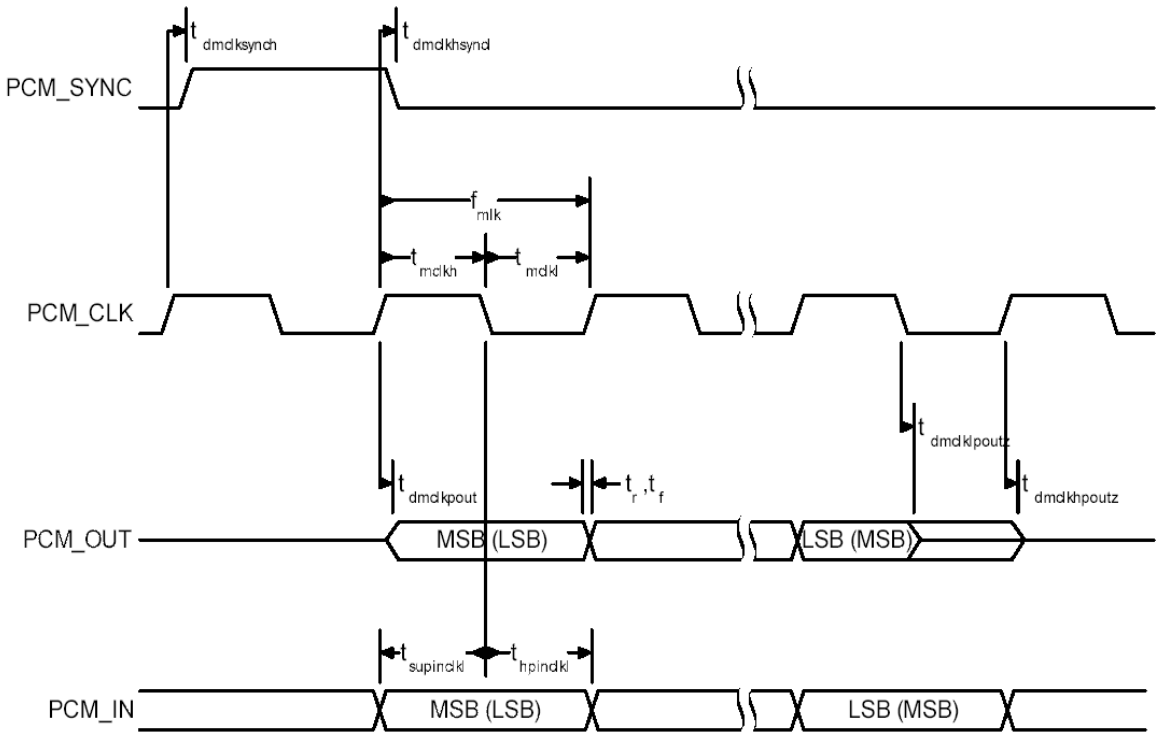

Figure 26: PCM master timing short frame sync

12.4.9 PCM slave timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64		2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	ns
f_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time for PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_ SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (Long frame sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_ SYNC or PCM_CLK low, whichever is later, to valid PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low valid to PCM_IN invalid	30	-	-	ns

Table 16: PCM slave timing

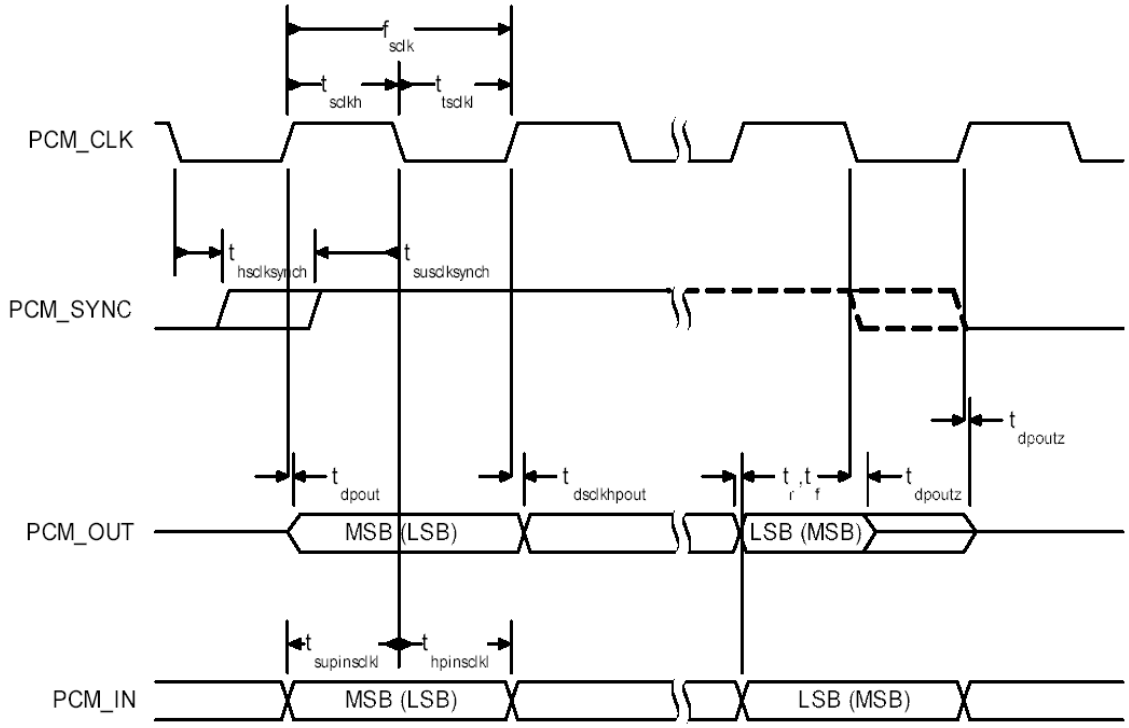

Figure 27: PCM slave timing long frame sync

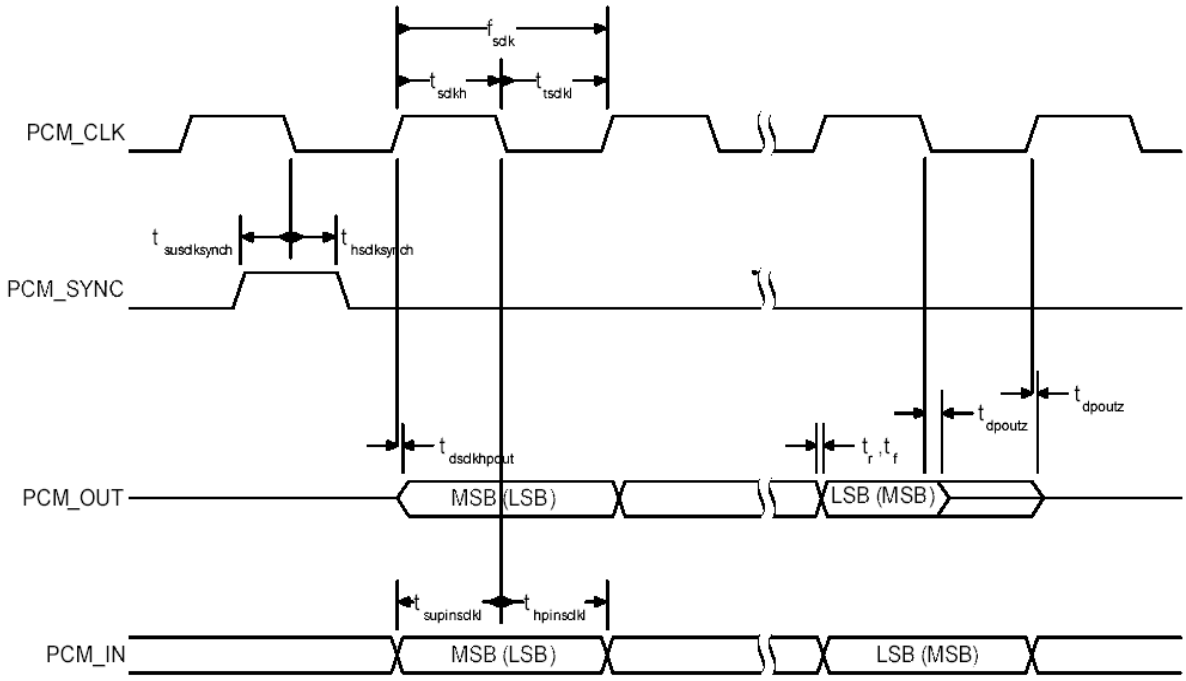

Figure 28: PCM slave timing short frame sync

12.4.10 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables detail these PS Keys. PSKEY_PCM_CONFIG32. The default for this key is 0x00800000 i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-stating of PCM_OUT.

PSKEY_PCM_LOW_JITTER_CONFIG is described in Table below.

Name	Bit position	Description
-	0	Set to 0.
SLAVE MODE EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT SYNC EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0
SIGN EXTENDED EN	4	0 selects padding of 8 or 13-bit voice sample into a 16- bit slot by inserting extra LSBs, 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB FIRST EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB first.
TX TRISTATE EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX TRISTATE RISING EDGE EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.

SYNC SUPPRESS EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilize this to enter a low power state.
GCI MODE EN	9	1 enables GCI mode.
MUTE EN	10	1 forces PCM_OUT to 0.
48M PCM CLK GEN EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore4-External. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG LENGTH SYNC EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER CLK RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE SLOT	[26:23]	Default is '0001'. Ignored by firmware.
SAMPLE FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 17: PSKEY_PCM_CONFIG32 description

Name	Bit position	Description
CNT LIMIT	[12:0]	Sets PCM_CLK counter limit.

CNT RATE	[23:16]	Sets PCM_CLK count rate.
SYNC LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 18: PSKEY_PCM_LOW_JITTER_CONFIG Description

12.5 I/O Parallel Ports

The Parallel Input Output (PIO) Port is a general-purpose I/O interface to WT12. The port consists of six programmable, bi-directional I/O lines, PIO[2:7].

Programmable I/O lines can be accessed either via an embedded application running on WT12 or via private channel or manufacturer-specific HCI commands.

All PIO lines are configured as inputs with weak pull downs at reset.

PIO[2] / USB_PULL_UP (1)

This is a multifunction terminal. The function depends on whether WT12 is a USB or UART capable version. On UART versions, this terminal is a programmable I/O. On USB versions, it can drive a pull-up resistor on USB_D+. For application using external RAM this terminal may be programmed for chip select.

PIO[3] / USB_WAKE_UP (1)

This is a multifunction terminal. On UART versions of WT12 this terminal is a programmable I/O. On USB versions, its function is selected by setting the Persistent Store Key PSKEY_USB_PIO_WAKEUP (0x2cf) either as a programmable I/O or as a USB_WAKE_UP function.

PIO[4] / USB_ON (1)

This is a multifunction terminal. On UART versions of WT12 this terminal is a programmable I/O. On USB versions, the USB_ON function is also selectable.

PIO[5] / USB_DETACH (1)

This is a multifunction terminal. On UART versions of WT12 this terminal is a programmable I/O. On USB versions, the USB_DETACH function is also selectable.

PIO[6] / CLK_REQ

This is multifunction terminal, its function is determined by Persistent Store Keys. Using PSKEY_CLOCK_REQUEST_ENABLE, (0x246) this terminal can be configured to be low when WT12 is in deep sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] to avoid losing timing accuracy in certain Bluetooth operating modes.

PIO[7]

Programmable I/O terminal.

13. RESET

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period **greater than 5ms**.

14. SOFTWARE STACKS

WT12 is supplied with Bluetooth v2.0 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

The WT12 software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

14.1 iWRAP Stack

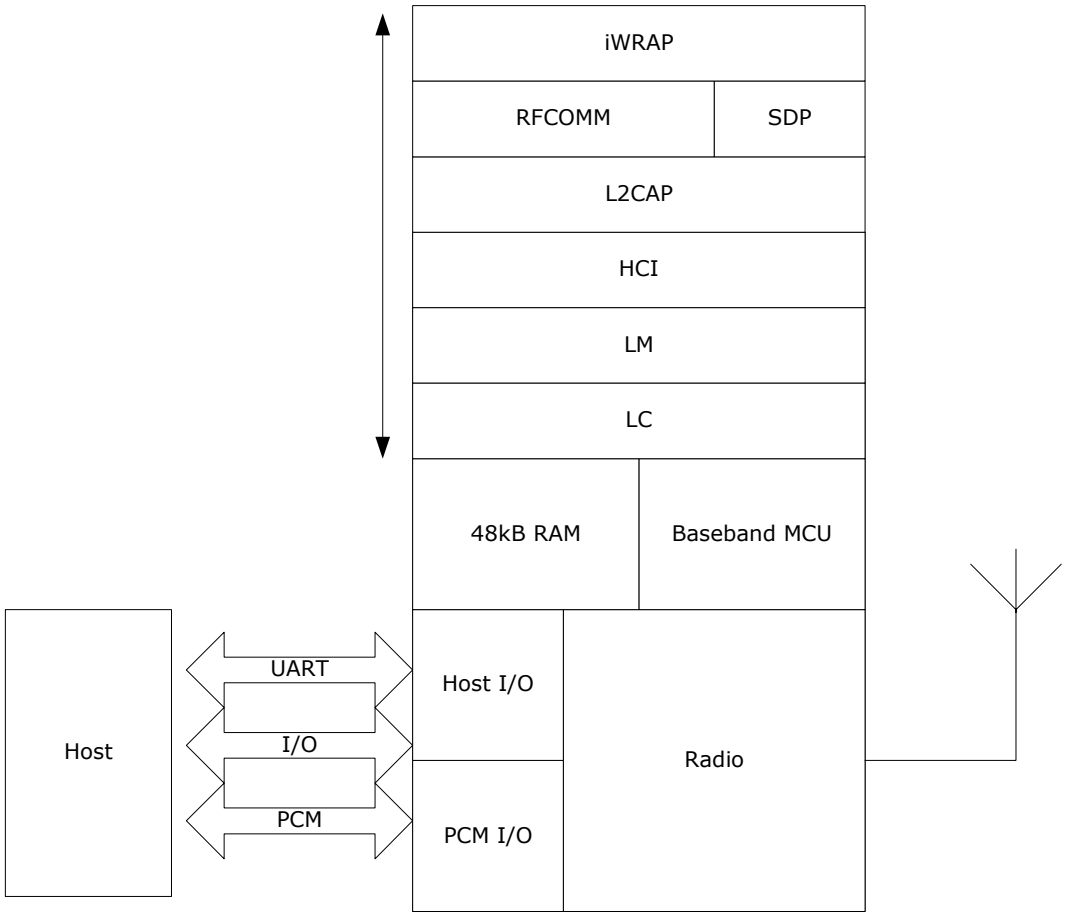

Figure 29: WRAP THOR VM Stack

In figure above, the iWRAP software solution is described. In this version of the stack firmware shown no host processor is required to run the Bluetooth protocol stack. All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The host processor interfaces to iWRAP software via one or more of the physical interfaces which are also shown in the figure above. The most common interfacing is done via UART interface using the ASCII commands supported by the iWRAP software. With these ASCII commands the user can access Bluetooth functionality without paying any attention to the complexity which lies in the Bluetooth protocol stack.

The user may write applications code to run on the host processor to control iWRAP software with ASCII commands and to develop Bluetooth powered applications.

Notes:

More details of iWRAP software and it's features can be found from *iWRAP User Guide* which can be downloaded from www.bluegiga.com.

14.2 HCI Stack

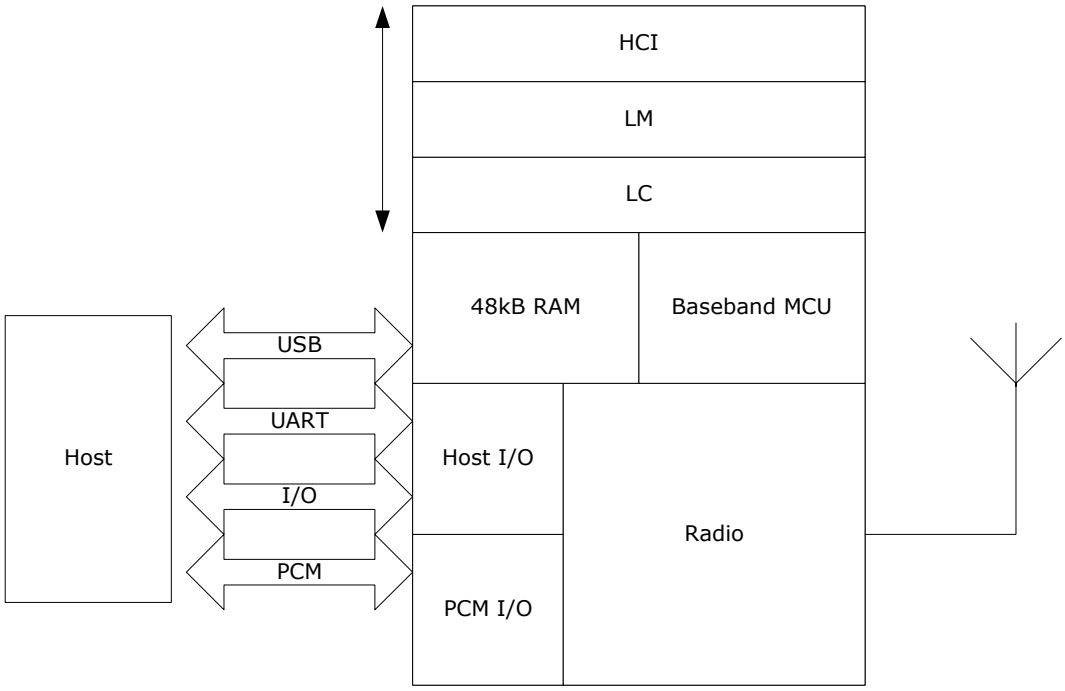

Figure 30: WRAP THOR HCI Stack

In the implementation shown in figure above the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

14.2.1 Features of HCI Stack

1. New Bluetooth v2.0 + EDR Mandatory Functionality:
    - (AFH), including classifier
    - Faster connection – enhanced inquiry scan (immediate FHS response)
    - LMP improvements
    - Parameter ranges
2. Optional v2.0 functionality supported:
    - Adaptive Frequency Hopping (AFH) as Master and Automatic Channel Classification
    - Fast Connect – Interlaced Inquiry and Page Scan plus RSSI during Inquiry
    - Extended SCO (eSCO), eV3 +CRC, eV4, eV5
    - SCO handle
    - Synchronization

The firmware has been written against the Bluetooth v2.0 + EDR Specification.

- Bluetooth components:
    - Baseband (including LC)
    - LM
    - HCI
- Standard USB v2.0 (full speed) and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps(1)
- Operation with up to seven active slaves(1)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus "transparent SCO"
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold"
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance (PICS) documents. They can be asked separately form support@bluegiga.com.

Extra functionality:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth UART Host Transport

- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command"), provides:

- Access to the chip's general-purpose PIO port

- The negotiated effective encryption key length on established Bluetooth links

- Access to the firmware's random number generator

- Controls to set the default and maximum transmit powers – these can help minimize interference between overlapping, fixed-location piconets

- Dynamic UART configuration

- Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit

- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code

- A block of BCCMD commands provides access to the chip's "persistent store" configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.

- A UART "break" condition can be used in three ways:

- Presenting a UART break condition to the chip can force the chip to perform a hardware reboot

- Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialization while the condition exists

- With BCSP, the firmware can be configured to send a break to the host before sending data – normally used to wake the host from a deep sleep state

- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules

- A modified version of the DFU protocol allows firmware upgrade via the chip's UART

- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.

- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LED's via the chip's PIO port.

- Hardware low power modes: shallow sleep and deep sleep. The chip drops into

modes that significantly reduce power consumption when the software goes idle.

- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

- Co-operative existence with 802.11b/g chipsets. The device can be optionally configured to support a number of different co-existence schemes including:

    - TDMA - Bluetooth and WLAN avoid transmitting at the same time.

    - FDMA - Bluetooth avoids transmitting within the WLAN channel

    - Combination TDMA & FDMA - Bluetooth avoids transmitting in the WLAN channel only when WLAN is active.

- Please refer to separate documentation for full details of the co-existence schemes that CSR supports.

Notes:

1. Supports basic data rate up to 723.2kbps asymmetric, maximum allowed by Bluetooth v2.0 + EDR specification

2. WT12 supports all combinations of active ACL and SCO channels for both Master and

3. Always refer to the Firmware Release Note for the specific functionality of a particular build.

14.3 RFCOMM Stack

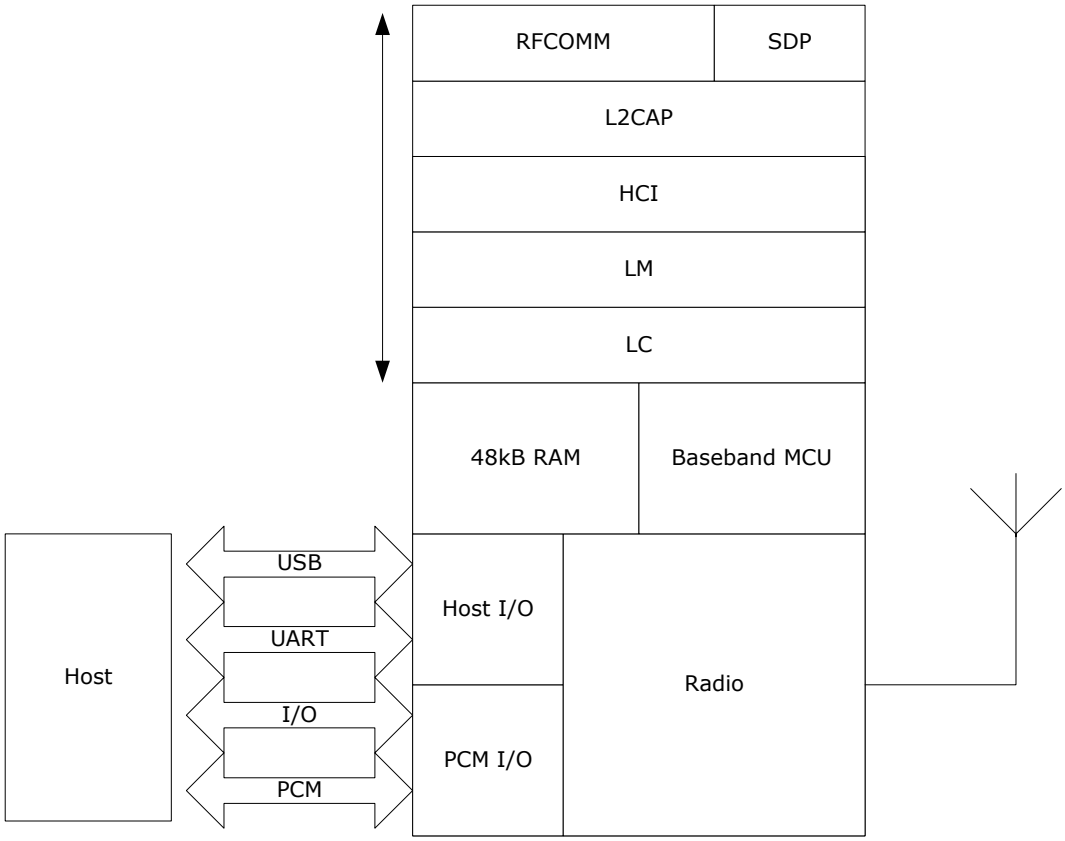

Figure 31: WRAP THOR RFCOMM stack

In the version of the firmware, shown in Figure 9.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

14.3.1 Features of RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350kbps[1]

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimize interference to other radio devices using the ISM band.

Notes:

1. The data rate is with respect to WT12 with basic data rate packets.

14.4 VM Stack

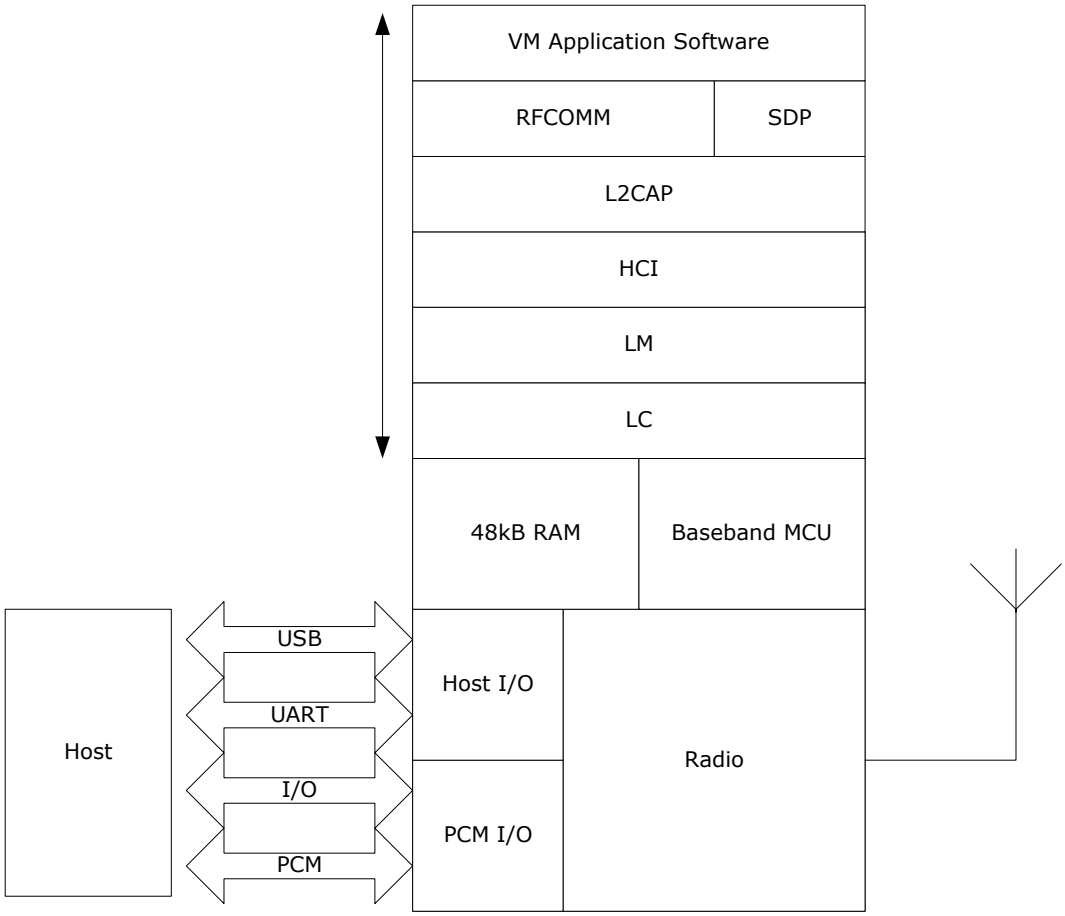

Figure 32: WRAP THOR VM Stack

In figure above, this version of the stack firmware shown requires no host processor (but can use a host processor for debugging etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab™ software development kit (SDK) supplied with the Casira development kit, available separately from Bluegiga or directly form CSR. This code will then execute alongside the main WRAP THOR firmware. The user is able to make calls to the WRAP THOR firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

Notes:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

14.5 HID Stack

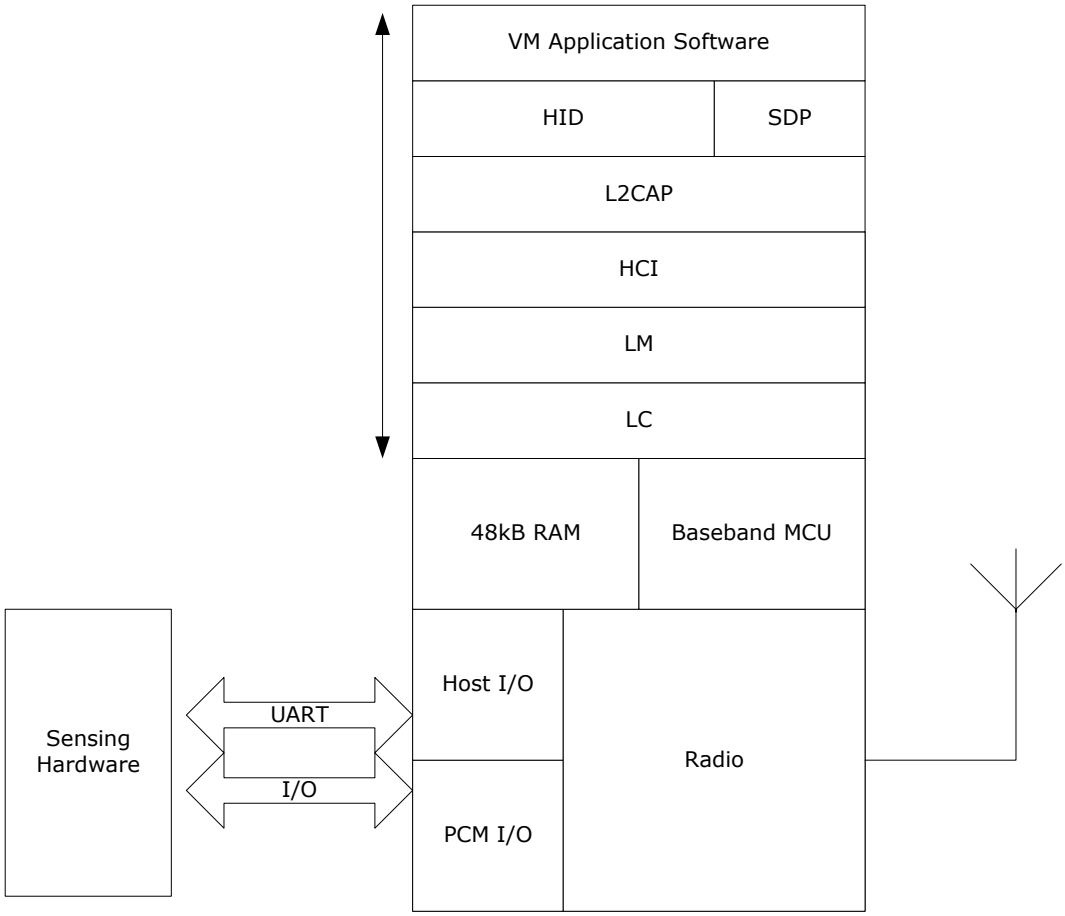

Figure 33: WRAP THOR HID stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional software development kit (SDK) supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customize features such as power management and connect/reconnect behavior.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include 5 mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available separately.

14.5.1 Software Development

CSR's BlueLab and Casira development kits are available to allow the evaluation of the WT12 hardware and software, and as toolkits for developing on-chip and host software.

15. SOLDERING

15.1 Manual Soldering

TBA

15.2 Reflow Soldering

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.

2. Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimize the out gassing of the flux.

3. Reflow Zone - The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.

4. Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

5. Solder Re-Flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

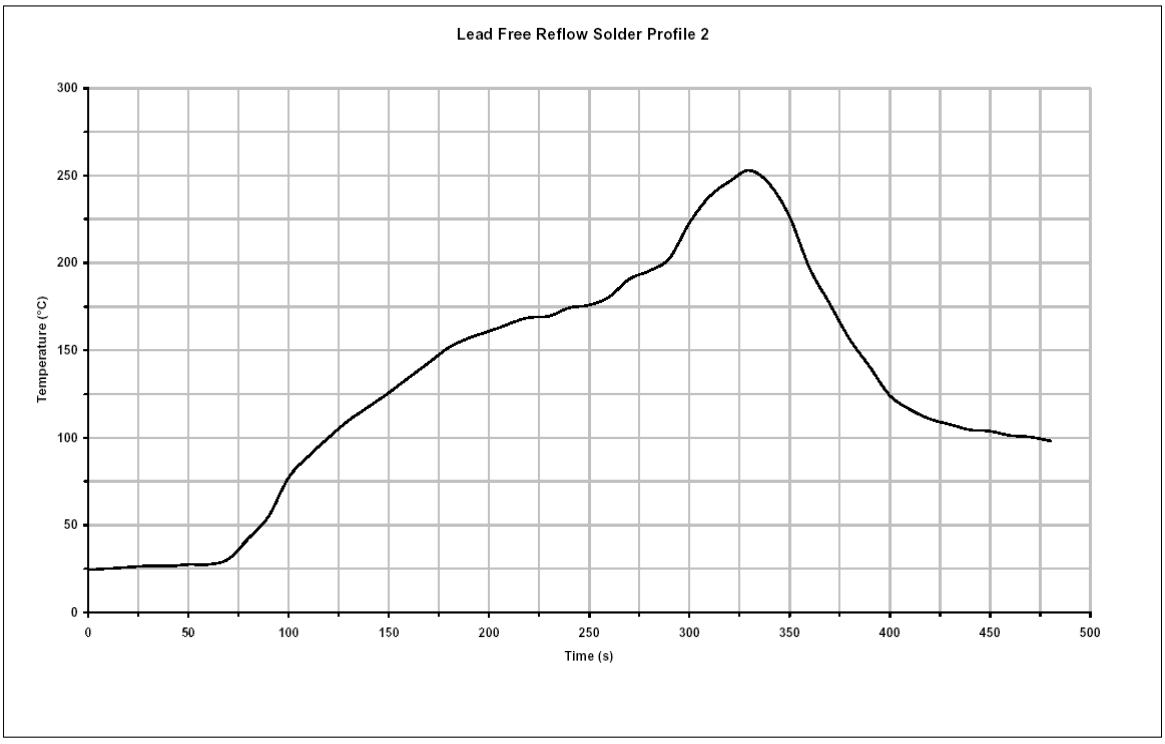

Figure 34: Reflow solder profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260°C.

16. PACKAGE

TBA

17. CERTIFICATIONS

TBA

18. ENHANCED DATA RATE

EDR has been introduced to provide 2x and optionally 3x data rates with minimal disruption to higher layers of the Bluetooth stack. CSR supports both of the new data rates, with WT12. WT12 is compliant with revision v2.0.E.2 of the specification.

18.1 Enhanced Data Rate Baseband

At the baseband level EDR uses the same 1.6kHz slot rate as basic data rate and therefore the packets can be 1, 3, or 5 slots long as per the basic data rate. Where EDR differs from the basic data rate is that in the same 1MHz symbol rate 2 or 3bits are used per symbol, compared to 1bit per symbol used by the basic data rate. To achieve the increase in number of bits symbol, two new modulation schemes have been introduced as summarized in Table presented below and the modulation schemes are explained in the further sections.

Scheme	Bits per symbol	Modulation
Basic Data Rate	1	GFSK
Enhanced Data Rate	2	Π/4 DQPSK
Enhanced Data Rate	3	8DPSK (optional)

Figure 35: Data rate schemes

Although the EDR uses new packets Link establishment and management are unchanged and still use Basic Rate packets.

18.2 Enhanced Data Rate Π/4 DQPSK

4-state Differential Phase Shift Keying

2 bits determine phase shift between consecutive symbols

2 bits determine phase shift between consecutive symbols

S/4 rotation avoids phase shift of S, which would cause large amplitude variation

Raised Cosine pulse shaping filter to further reduce side band emissions

Bit pattern	Phase shift
00	Π/4
01	3 Π/4
10	-3 Π/4
11	- Π/4

Figure 36: 2 bits determine phase shift between consecutive symbols

18.3 8DQPSK

8-state Differential Phase-Shift Keying

Three bits determine phase shift between consecutive symbols.

Bit pattern	Phase shift
000	0
001	Π/4
011	Π/2
010	3 Π/4
110	Π
111	-3 Π/4
101	- Π/2
100	- Π/4

Figure 37: 3 bits determine phase shift between consecutive symbols

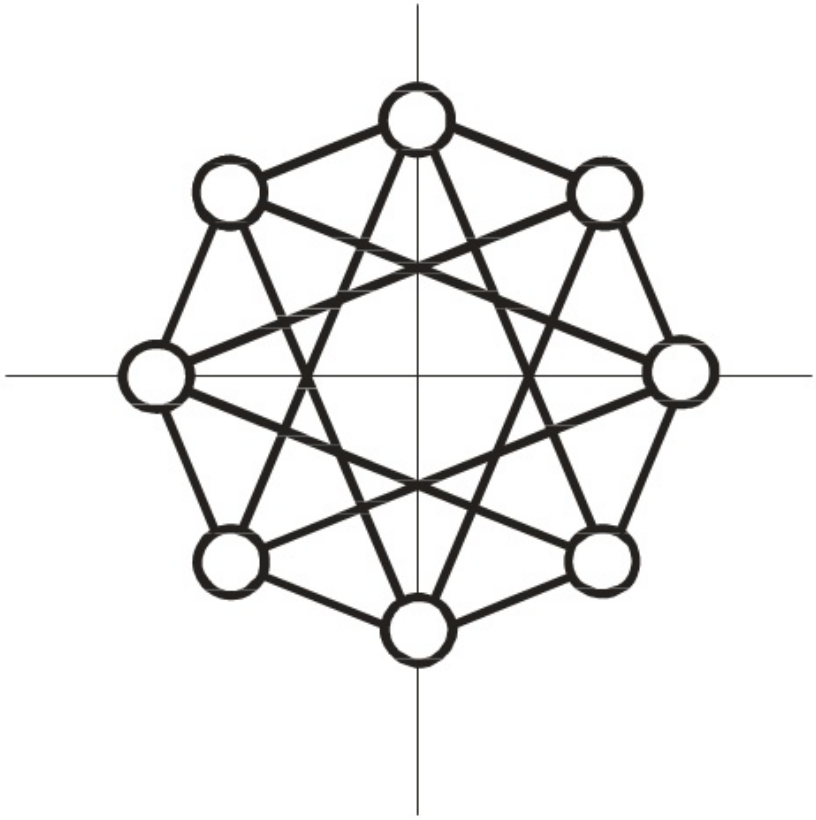

Figure 38: 8DQPSK

19. CONTACT INFORMATION

Sales: sales@bluegiga.com

Technical support: support@bluegiga.com
http://www.bluegiga.com/techforum/

Orders: orders@bluegiga.com

Head Office / Finland

Phone: +358-9-4355 060
Fax: +358-9-4355 0660

Street Address:
Sinikalliontie 11
02630 ESPOO
FINLAND

Postal address:
P.O. BOX 120
02631 ESPOO, FINLAND

Sales Office / USA
Phone: (781) 556-1039

Bluegiga Technologies, Inc.
99 Derby Street, Suite 200
Hingham, MA 02043